SAMSUNG

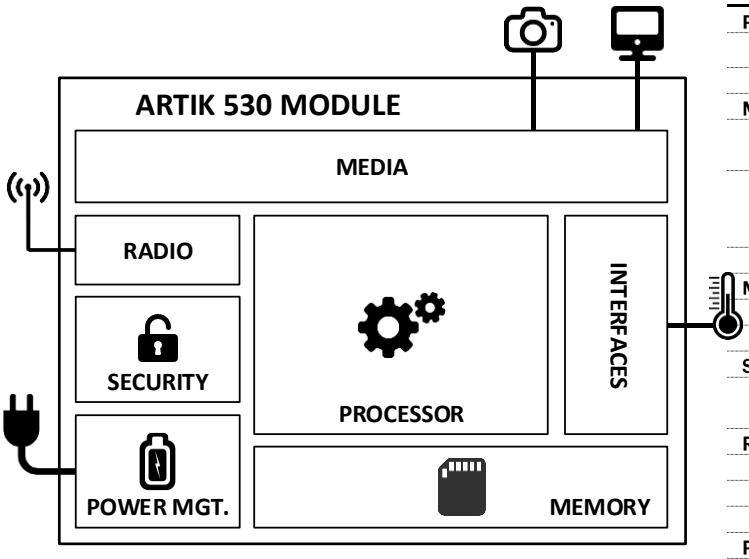
ARTIK™ Modules

5

530 Datasheet

ARTIK 530 Module Top View

The Samsung ARTIK™ 530 Module is a highly-integrated System-in-Module that combines a quad core ARM® Cortex®-A9 processor packaged DRAM and Flash memories; a Secure Element; and a wide range of wireless communication options such as 802.11a/b/g/n, Bluetooth® 4.2 (BLE+Classic), and 802.15.4 for ZigBee®/Thread; all into one 49x36mm footprint. The many standard digital control interfaces support external sensors and higher-performance peripherals to expand the module's capabilities. With the combination of 802.11, Bluetooth® and ZigBee or Thread, the ARTIK 530 Module is the perfect choice for home automation and home hub devices, while also supporting a rich UI/UX capability for camera and display requirements. The inclusion of a hardware-based Secure Element provides end-to-end security.



ARTIK 530 Module Block Diagram

Processor	
CPU	Quad core ARM® Cortex®-A9@1.2GHz
GPU	3D graphics accelerator
Media	
Camera I/F	4-lane MIPI CSI up to 5M (1920x1080@30fps)
Display	4-lane MIPI DSI and HDMI1.4a (1920x1080p@60fps) or LVDS (1280x720p@60fps)
Audio	Two I²S audio input/output
Memory	
DRAM	512MB DDR3
FLASH	4GB eMMC v4.5
Security	
Secure Element	Secure point to point authentication and data transfer
Radio	
WLAN	IEEE 802.11a/b/g/n, dual band SISO
Bluetooth®	4.2 (BLE+Classic)
802.15.4	ZigBee/Thread
Power Management	
PMIC	Provides all power of the ARTIK 530 Module using on board bucks and LDOs
Interfaces	
Ethernet	10/100/1000Base-T MAC (External PHY required)
Analog and Digital I/O	GPIO, UART, I²C, SPI, USB Host, USB OTG, HSIC, ADC, PWM, I²S, JTAG

ARTIK 530 Module Table of Contents

List of Figures

List of Tables

VERSION HISTORY

Revision	Date	Description	Maturity
V1.0	January 20, 2017	ARTIK 530 datasheet.	Release
V1.01	February 07, 2017	Updated Module PAD's section. Updated look and feel.	Release Update
V1.02	April 12, 2017	Updated default behavior of GPIO pins to latest software release.	Release Update
V1.02a	May 2, 2017	Updated Booting Sequence section. 802.15.4 RF Specifications section. Updated Table 35-36. Updated SD/MMC AC Electrical Characteristics section. Updated Recommended Operating Conditions section. Updated ESD section. Updated Table 34. Updated Power management section. Updated Table3-4. Updated Table 31-32.	Release Update
V1.02b	May 8, 2017	Updated Table 1.	Release Update
V1.02c	May 15-16, 2017	Updated Table 1-Table 33.	Release Update
V1.02d	May 24, 2017	Updated Table 2-6. Updated Table 21. Updated Table 30. Created KCC certification section. Created SRRC certification section.	Release Update
	May 30, 2017	Updated Table 1, 7-9. Updated Table 10-16, 19, 20. Updated Table 26-28.	

Block Diagram and Module Features

Figure 1 shows the functional block diagram of the ARTIK 530 Module. It consists of a quad-core ARM® Cortex®-A9 application processor with 512MB of DDR3 and 4GB eMMC, PMIC power management, Secure Element, 802.11/Bluetooth®, 802.15.4 and RF connectors.

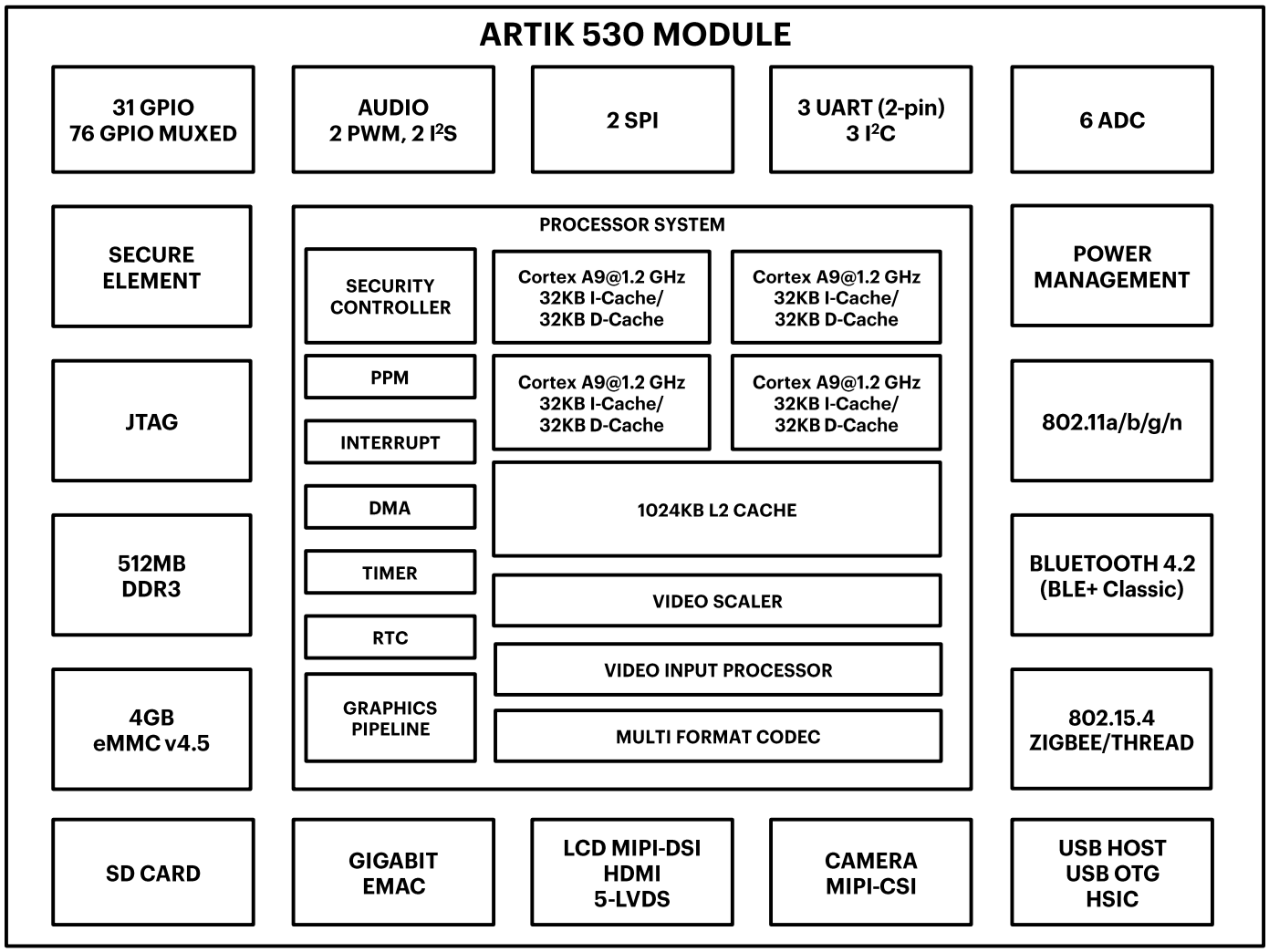


Figure 1. ARTIK 530 Module Functional Block Diagram

Warning : Do not apply power to the ARTIK 530 Module before connecting antennas or damage to the Module may result!

ARTIK 530 MODULE FEATURES

The sub-sections that will follow describe the functions of the various blocks depicted in *Figure 1* that are present on the ARTIK 530 Module.

GPIO

The ARTIK 530 Module provides a GPIO system with up to 107 GPIOs (76 multiplexed, 31 dedicated) to allow for a wide variety of use cases to be supported. The key features of the GPIO system are:

- Programmable pull-up control
- Both edge detect and level detect functionality
- Support for programmable pull-up resistors
- Support for fast or normal slew operation
- Support for default Drive Strength or High Drive Strength
- Support for interrupt generation that can be triggered on:
  - Rising edge
  - Falling edge
  - High level detection
  - Low level detection
- The I/O data is clocked up to 50MHz

I²S

The ARTIK 530 Module provides two 5-line Inter-IC Sound (I^2S) channel. I^2S is one of the most popular digital audio interfaces. The I^2S bus handles audio data and other signals, such as sub-coding and control. It is possible to transmit data between two I^2S buses. The key features of the I^2S sub-system are:

- Supports 1-port stereo (1 channel) I^2S-bus for audio with DMA based operation
- Supports serial data transfer of 16/24-bit per channel in Master and Slave mode
- Supports a variety of interface modes:
  - I^2S, Left justified, Right justified, DSP mode

PWM

The ARTIK 530 Module provides two pulse width modulation (PWM) modules. The key features of the PWM modules are:

- Two individual PWM channels with independent duty control and polarity
- Two 32-bit PWM timers, one per channel
- Support for static as well as dynamic setup
- Support for auto-reload and one shot pulse mode
- Dead zone generator
- Level interrupt generation

SPI

The ARTIK 530 Module provides two, Serial Peripheral Interfaces (SPI) that transfers serial data. SPI support includes 8-bit/16-bit shift registers to transmit and receive data. During an SPI transfer, data is simultaneously transmitted (shifted out serially) and received (shifted in serially). The SPI implementation adheres to the protocols described by Texas Instruments Synchronous Serial, National Semiconductor's Microwire and Motorola's Serial Peripheral Interface. The key features of the SPI sub-system are:

- Support for full-duplex
- 8-bit/16-bit shift register for Tx and Rx
- Complies with the SPI protocol described by Texas Instruments, National Semiconductor and Motorola
- Support for independent 16-bit wide transmit and receive FIFOs 8 locations deep
- Supports for master mode and slave mode
- Supports for receive-without-transmit operation
- Max operating frequency :
  - Master Mode : Support Tx up to 50MHz, Rx up to 20MHz

- Slave Mode : Support Tx up to 8MHz, Rx up to 8MHz

UART

The ARTIK 530 Module provides three 2-pin universal asynchronous receiver transmitters (UARTs). The key features of the UART sub-system are:

- Separate 32x8 Tx and 32x12 Rx FIFO memory buffers
- Support for DMA mode (UART0 : [AP_UART_RX0, AP_UART_TX0] only) and interrupt based mode of operation
- All independent channels support IrDA 1.0
- Support for modem control functions CTS, DCD, DSR, RTS, DTR and RI
- Each UART channel contains:
  - Programmable baud-rates
  - 1 or 2 stop bit insertion
  - 5-bit, 6-bit, 7-bit, or 8-bit data width
  - Parity checking

I^2C

The ARTIK 530 Module provides three generic I^2C blocks supporting both 100kb/s and 400kb/s speed modes.
The key features of the I^2C sub-system are:

- Supporting multi-master and slave mode
- 7-bit addressing mode only
- Supports serial, 8-bit oriented and bi-directional data transfer
- Supports up to 100 kb/s in the standard mode
- Supports up to 400 kb/s in the fast mode
- Supports master transmit, master receive, slave transmit, and slave receive operation
- Supports both interrupt and polling events

ADC

The ADC interface controls one 28nm low power CMOS 1.8V 12-bit ADC. The key features of the ADC sub-system are:

- Up to six channels of analog input can be selected
- Converts analog input into 12-bit binary code up to 1MSPS
- Power consumption 1.0mW when running 1MSPS
- Input frequency up to 100kHz

POWER MANAGEMENT

The ARTIK 530 Module power requirements are managed using a power management integrated circuit (PMIC). This PMIC device has four fully-integrated fixed-frequency current-mode synchronous PWM step-down converters that can achieve peak efficiencies of up to 97%. In addition it provides seven low-noise LDOs with currents up to 300mA, one always-on LDO and an integrated backup battery charger that will provide all power requirements for the ARTIK 530 Module.

The four DC-DC regulators operate at a fixed high frequency of 2.25MHz, minimizing noise in sensitive applications and allowing the use of small form factor components. These four buck regulators supply up to 3A of output current and can fully satisfy the power and control requirements of the ARTIK 530 Module. Dynamic Voltage Scaling (DVS) of the various core voltages is supported using I^2C control.

For a detailed description see the section on *Power Supply Requirements*.

802.11

The ARTIK 530 Module has a fully-integrated WLAN block covering IEEE 802.11 a/b/g/n. The most important hardware features of the 802.11 module are:

- 802.11 a/b/g/n dual band SISO, 2.4GHz/5GHz compliant
  - 1T1R 2.4GHz/5GHz band

  - Support for 20 and 40MHz bandwidth (72.2/150Mbps PHY rate)
- Enhanced 802.11/Bluetooth® Coexistence control to improve transmission quality in different profiles

BLUETOOTH®

The ARTIK 530 Module has a fully-integrated Bluetooth® block 4.2 (BLE+Classic). The most important hardware features of the Bluetooth® module are:

- Bluetooth® 4.2 (BLE+Classic)
- Enhanced 802.11/Bluetooth® Coexistence control to improve transmission quality in different profiles

802.15.4

The ARTIK 530 Module carries fully-integrated 802.15.4 functionality. The most important hardware features are:

- Fully integrated 2.4 GHz, IEEE 802.15.4 compliant transceiver
- Complete system-on-chip using 32-bit ARM® Cortex®-M4 processor
- Flash and RAM memory and peripherals.
- Extremely low power consumption.
- Excellent RF performance.
- Single-voltage operation.
- Supported Protocols:
  - ZigBee
  - Thread

USB OTG

The ARTIK 530 Module provides one USB2.0 OTG interface supporting both device and host functionality. The key features of the USB2.0 OTG sub-system are:

- In compliance with the USB 2.0 on-the-go specification revision 1.3a and 2.0
- Operates in high speed (480Mbps) mode
- Operates in full speed (12Mbps) mode
- Operates in low speed (1.5Mbps, host only) mode
- Supports session request protocol (SRP) and host negotiation protocol (HNP)
- One control endpoint 0 for control transfer
- Supports up to 15 device-programmable endpoints:
  - Programmable endpoint type: Bulk, Isochronous, Interrupt
  - Programmable In/Out direction
- Supports 16 host channels

USB HOST

The ARTIK 530 Module provides one USB2.0 Host controller that is fully compliant with the USB 2.0 specifications, and the enhanced host controller Interface (EHCI) specification. The key features of the USB2.0 OTG sub-system are:

- Detecting the attachment and removal of USB devices
- Collecting status and activity statistics
- Controlling power supply to attached USB devices
- In compliance with the UTMI+ Level 3 revision 1.0
- Controlling the association to either the open host controller interface (OHCI) or the EHCI via a port router
- Root Hub functionality to support up/down stream port

HSIC

The ARTIK 530 Module provides one high speed inter chip (HSIC) version 1.0 module. The key features of the HSIC sub-system are:

- Support for ping and split transactions
- Up to 30MHz operation for a 16-bit interface
- Up to 60MHz operation for a 8-bit interface

- Support for HSIC version 1.0

MIPI CSI

The ARTIK 530 Module provides one 4-lane mobile industry processor interface (MIPI) interface that complies with the MIPI camera serial interface (CSI) standard specification V1.01r06 and D-PHY standard specification v1.0. The key features of the MIPI CSI sub-system are:

- Supports 1, 2, 3 or 4 data lanes
- Supported image formats are:
  - YUV420, YUV420 (Legacy), YUV420 (CSPS), 8-bit YUV422, 10-bit YUV422
  - User defined Byte based data packet
  - Compatible to PPI (Protocol to PHY interface)

MIPI DSI

The ARTIK 530 Module provides one 4-lane MIPI interface that complies with the MIPI DSI standard specification V1.01r11. The key features of the MIPI DSI sub-system are:

- Maximum resolution ranges up to 1920x1080
- Supports 1, 2, 3 or 4 data lanes
- Supports pixel format:
  - 16bpp, 18bpp packed, 18bpp loosely packed (3 byte), 24bpp
- Supported interfaces are:
  - Protocol-to-PHY Interface (PPI) up to 1.5Gbps, in MIPI D-PHY
  - RGB Interface for video image input from display controller
  - PMS control interface for PLL to configure byte clock frequency
  - Pre-scaler to generate escape clock from byte clock

HDMI

The ARTIK 530 Module provides one HDMI v1.4a interface. The key features of the HDMI sub-system are:

- Support for v1.4a spec
- Up to 1080p video resolution
- HDMI Link + HDMI PHY
- Support for the following video formats:
  - 480p@59.94/60Hz
  - 576p@50Hz
  - 720p@50/59.94/60Hz
  - 1080p@50/59.94/60Hz (No support for interlaced format)
- Support for 4:4:4 RGB
- Support for up to 8-bits per color

LVDS

The ARTIK 530 Module provides five low voltage differential signaling (LVDS) output channels with one clock channel. The key features of the LVDS channel system are:

- Output clock range 30-125MHz
- Support for 630 Mbps per channel
- Up to 393.75MB/s data transport
- Support for power down mode

GIGABIT EMAC

The ARTIK 530 Module provides one Gigabit EMAC interface. The most important features of the Ethernet MAC module are:

- Standard compliance
  - IEEE 802.3az-2010: energy efficient Ethernet (EEE)
  - RGMII v2.6

- MAC supports the following features:
  - 10/100/1000 Mbps data transfer rates with an RGMII interface to communicate with external Gigabit PHY
  - Full duplex operation
  - Half duplex operation
  - Flexible address filtering
  - Additional frame filtering

SD-CARD

The ARTIK 530 Module provides one shared SD-card/MMC interface. The Mobile Storage Host is an interface between the system and the SD-card. The key features of mobile storage host sub-system are:

- Support for Secure Digital I/O (SDIO – version 3.0)
- Support for Secure Digital Memory (SDMEM – version 3.0)
- Support for Consumer Electronics Advanced Transport Architecture (CE-ATA-version 1.1)
- Support 4-bit SDR mode up to 50MHz
- Supports PIO and DMA mode data transfer
- Supports ¼- bit data bus width

MMC

The ARTIK 530 Module provides one shared SD-card/MMC interface. The Mobile Storage Host is an interface between the system and MMC card. The key features of mobile storage host sub-system are:

- Support for Embedded Multimedia Cards (MMC – version 4.41)
- Support for Embedded Multimedia Cards (eMMC – version 4.5)
- Support 4-bit SDR mode up to 50MHz
- Supports PIO and DMA mode data transfer
- Supports ¼- bit data bus width

DDR

The ARTIK 530 Module has DDR memory. The key features of the DDR memory present on the ARTIK 530 Module are:

- One 32-bit DDR3 memory interface
- Two 256MB DDR3 16-bit memory chips, for a total of 512MB
- Up to 800MHz DDR3 speed with a maximum throughput of 6.4GB/s

JTAG

Our JTAG core that is part of the ARTIK 530 Module provides debug capabilities for the developer. The main features of the JTAG module are:

- Compliant with the IEEE 1149 standard
- Can only be used together with the ARTIK 530 Module.

SECURE ELEMENT

The ARTIK 530 Module has a dedicated Secure Element to assure end-to-end authentication and communication between nodes in an IoT setting. The Secure Element provides an ISO/IEC 7816 14443 compliant interface. The most important hardware features of the Secure Element are:

- Dedicated 16-bit SecuCalm CPU core
- Crypto co-processor
  - Modular exponential accelerator
  - RSA 2080 bits
  - ECC 512 bits
- Data security
  - Memory encryption for all memory
  - 256B read only and 256B non erasable flash area
  - Selective reset operation if abnormal voltages/frequencies are detected

- Embedded tamper-free memory
  - 32KB ROM
  - 264KB FLASH
  - (6+2.5)KB Static RAM including 2.5KB crypto memory
- Serial interfaces:
  - ISO 7816-3 compliant interface
  - Asynchronous half-duplex character receive/transmit serial interface

Quad Core Processor System

The processor system architecture that resides on the ARTIK 530 Module is a system-on-a-chip (SoC) based on a 32-bit RISC architecture. Designed using the 28nm low power process, the processor system architecture provides superior performance using a quad-core CPU. The key features of the ARTIK 530 Module are:

- Quad-core ARM® Cortex®-A9, 32-bit RISC architecture
- Maximum core speed 1.2GHz
- 32KB I-Cache per core
- 32KB D-Cache per core
- 1024KB L2-Cache shared between four cores
- Support for dynamic virtual-address mapping

PPM

The ARTIK 530 Module has one pulse period measurement (PPM) IP-block that can measure the duration of a high level or low level from a GPIO pin. The most important features of the PPM block are:

- One 16-bit counter tied to a clock that can vary between 843.75kHz and 13.50MHz

For more details on how to relate a PPM to a GPIO please refer to the ARTIK 530 Module software developer's guide.

Timer

The ARTIK 530 Module has four dedicated timer channels. The most important features of the Timer module are:

- Timer or watchdog timer modes
- Four dedicated Timer channels with watchdog timer
- Normal interval timer mode with interrupt request
- Reset on timer countdown
- Level-triggered interrupt mechanism

Interrupt

The ARTIK 530 Module has one interrupt module. The most important features of the interrupt module are:

- Vectored Interrupt Controller
- Support 64x channel interrupt sources
- For each interrupt source the following properties are available:
  - Fixed hardware interrupt priority level
  - Programmable interrupt priority level
  - Hardware interrupt priority level masking
  - IRQ and FIQ generation
  - Software interrupt generation
  - Test registers
  - Raw interrupt status
  - Interrupt request status

DMA

The ARTIK 530 Module has one scatter-gather DMA module. The most important features of the DMA module are:

- 16x channels of dedicated DMA

- 16x DMA request lines
- Various operating modes
  - Single DMA mode
  - Burst DMA mode
  - Memory to memory transfer
  - Memory to peripheral transfer
  - Peripheral to memory transfer
  - Peripheral to peripheral transfer
- Support for 8/16/32 bit wide transactions
- Big endian and little endian (default) support

RTC

The ARTIK 530 Module has one real time clock (RTC) module. The most important features of the RTC are:

- Four spread spectrum PLLs
- Two external crystals : one 24MHz crystal for PLL, one 32.768KHz crystal for RTC
- 32-bit RTC counter
- Support for alarm interrupt using RTC

Video Input Processor

The ARTIK 530 Module provides one video input processor (VIP). The key features of the VIP sub-system are:

- Support for external 8-bit and 16-bit MIPI-DSI
- Support for internal MIPI-CSI
- Support of images up to 8192x8192
- Support for clipping and scale-down
- Support for YUV420 memory format

Video Scaler

The ARTIK 530 Module provides one universal scaler. The key features of the scaler are:

- Support for different input formats
  - YUV420, YUV422, YUV444
- Flexible size, from 8x8 up to 1920x1080 with a granularity of 8
- Upscale ratio from 8x8 to 1920x1080
- Downscale ratio from 1920x1080 to 8x8
- Low pass filter available after upscale or before downscale
- Horizontal 5-tab filter with 64 sets of coefficients
- Vertical 3-tab filter with 32 sets of coefficients

Multi Format Codec

The ARTIK 530 Module provides one integrated Multi Format Codec (MFC) module. The key features of the MFC sub-system are:

- Decoder
  - H.264 : BP, MP, HP Level 4.2 up to 1920x1080, up to 50MBps
  - MPEG4 : Advanced Simple Profile (ASP) up to 1920x1080, up to 40Mbps
  - H.263 : Profile 3 up to 1920x1080, up to 20Mbps
  - MPEG 1,2 : Main Profile, High Level up to 1920x1080, up to 80MBps
- Encoder
  - H.264 : Baseline profile, Level 4.0 up to 1080p, up to 20Mbps
  - MPEG4 : Simple profile, Level 5.6 up to 1080p, up to 20Mbps
  - H.263 : Profile 3, Level 70 up to 1080p, up to 20Mbps

Graphics Pipeline

The ARTIK 530 Module provides one 2D and 3D graphics pipeline module. The key features of the graphics pipeline are:

- Two pixel processors
  - Tile oriented processing
  - Alpha blending
  - Texture support, non-power-of-2
  - Cube mapping
  - Fast dynamic branching
  - Trigonometric acceleration
  - Full floating point arithmetic
  - Line, quad, triangle and point sprites
  - Perspective correct texturing
  - Point sampling, bilinear and trilinear filtering
  - 8-bit stencil buffering
  - 4-level hierarchical Z and stencil operation
- Geometry processor
  - Programmable vertex shader
  - Flexible input and output formats
  - Autonomous operation tile list generation
  - Indexed and non-indexed geometry input
  - Primitive constructions with points, lines, triangles and quads
- Support for OpenGL ES 1.0 and 2.0

MODULE PADS

The ARTIK 530 Module utilizes 292 signal and ground BALLs providing all the relevant signaling. *Figure 2* shows how the BALLs are oriented and how signal coordinates are assigned to the PADs of the ARTIK 530 Module. *Table 2* - *Table 6* describe the relation between the BALL coordinates and the BALL signal names. These tables also provide detailed characteristics for each BALL signal name.

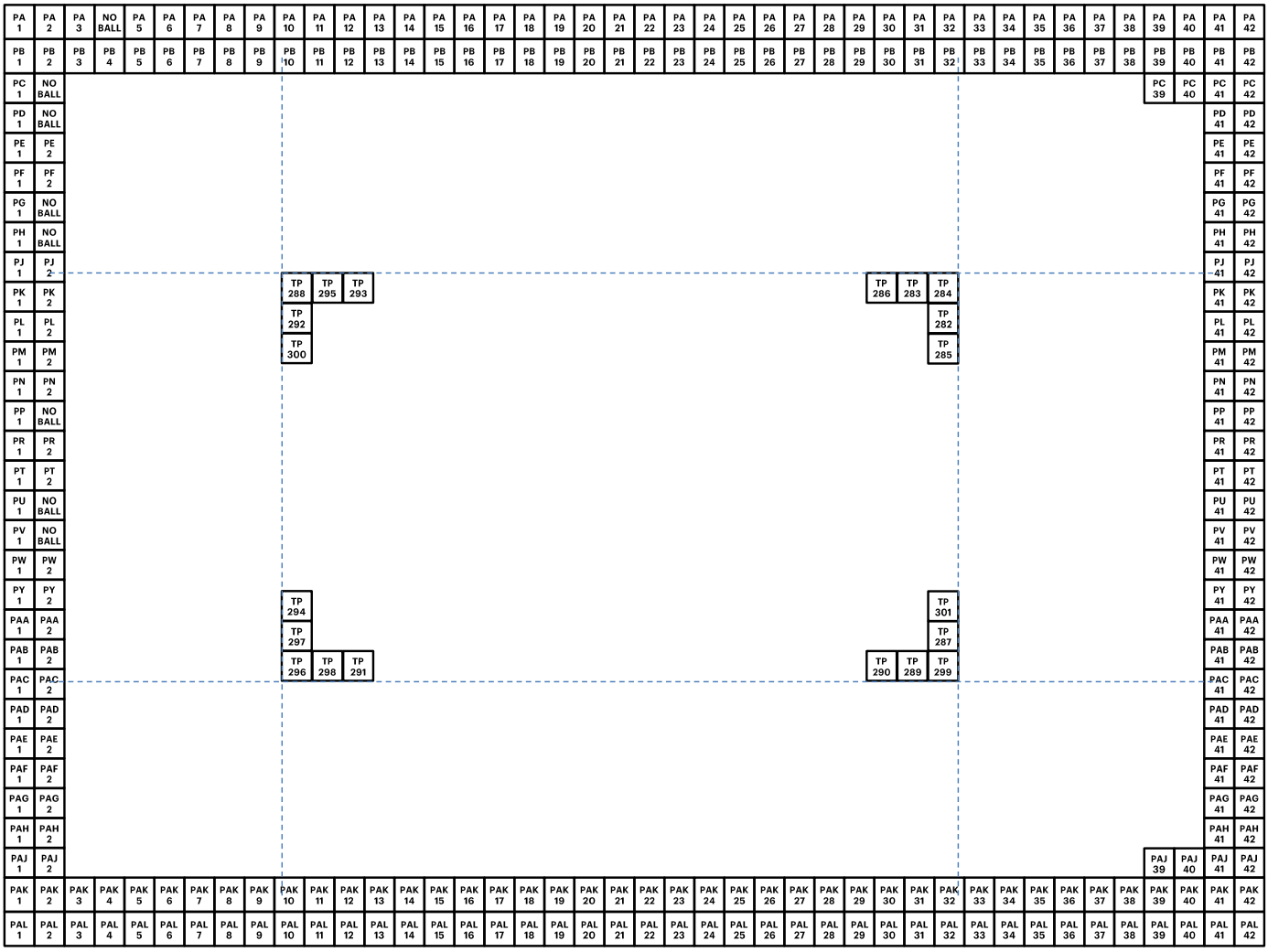


Figure 2. ARTIK 530 Module Top View BALL Organization

BALL TABLE COLUMN DEFINITIONS

The meaning of the various columns used in *Table 2* - *Table 6* is explained in *Table 1*.

Table 1. Ball Table Column Definition

Column Name	Column Definition
Ball	Identifier of the Ball on the ARTIK 530 Module
Ball Name	Nominal function of the ARTIK 530 Module
Power	Voltage level on the Ball
Default	Default function of the main SoC initialized by software
Type	S:Signal Ball, P:Power Ball, G:GND Ball
I/O	I:Input, O:Output, IO:Input/Output
PU/PD	PU:Pull-Up, PD:Pull-Down, N:No Pull-Up/Pull-Down
Group	Nominal function group set according to pad name. For more information see ARTIK 530 Module Hardware User Guide. Usually the function of the pin can be reprogrammed
Function	Explanation on the function of the ball

NORTH BALL ARRAY

Table 2. NORTH BALL ARRAY

BALL	BALL Name	Power	Default	Type	I/O	PU/PD	Group	Function
PA1	GMAC_TXEN	3V3	GMAC_TXEN	S	IO	N	GMAC	GMAC Transmit Enable
PA2	GMAC_TXD1	3V3	GMAC_TXD1	S	IO	N	GMAC	GMAC Transmit Data 1
PA3	GMAC_TXD3	3V3	GMAC_TXD3	S	IO	N	GMAC	GMAC Transmit Data 3
PA4	NO BALL	-	-	-	-	-	NO BALL	-
PA5	GMAC_GTXCLK	3V3	GMAC_GTXCLK	S	IO	N	GMAC	GMAC Transmit Clock
PA6	GMAC_RXDV	3V3	GMAC_RXDV	S	IO	N	GMAC	GMAC Receive Enable
PA7	GMAC_RXD2	3V3	GMAC_RXD2	S	IO	N	GMAC	GMAC Receive Data 2
PA8	GMAC_RXD0	3V3	GMAC_RXD0	S	IO	N	GMAC	GMAC Receive Data 0
PA9	GND	0V0	GND	G	-	-	GND	Ground
PA10	AP_MIPICSI_DNCLK	1V8	MIPICSI_DNCLK	S	IO	N	CSI	MIPI CSI Data Negative Clock
PA11	AP_MIPICSI_DN0	1V8	MIPICSI_DN0	S	IO	N	CSI	MIPI CSI Data Negative 0
PA12	AP_MIPICSI_DN1	1V8	MIPICSI_DN1	S	IO	N	CSI	MIPI CSI Data Negative 1
PA13	AP_MIPICSI_DN2	1V8	MIPICSI_DN2	S	IO	N	CSI	MIPI CSI Data Negative 2
PA14	AP_MIPICSI_DN3	1V8	MIPICSI_DN3	S	IO	N	CSI	MIPI CSI Data Negative 3
PA15	GND	0V0	GND	G	-	-	GND	Ground
PA16	AP_MIPIDSI_DNCLK	1V8	MIPIDSI_DNCLK	S	IO	N	DSI	MIPI DSI Data Negative Clock
PA17	AP_MIPIDSI_DN0	1V8	MIPIDSI_DN0	S	IO	N	DSI	MIPI DSI Data Negative 0
PA18	AP_MIPIDSI_DN1	1V8	MIPIDSI_DN1	S	IO	N	DSI	MIPI DSI Data Negative 1
PA19	AP_MIPIDSI_DN2	1V8	MIPIDSI_DN2	S	IO	N	DSI	MIPI DSI Data Negative 2
PA20	AP_MIPIDSI_DN3	1V8	MIPIDSI_DN3	S	IO	N	DSI	MIPI DSI Data Negative 3
PA21	GND	0V0	GND	G	0V0	-	GND	Ground
PA22	AP_LVDS_TN0	1V8	LVDS_TN0	S	IO	N	LVDS	LVDS Transmit Channel 0 Negative
PA23	AP_LVDS_TN1	1V8	LVDS_TN1	S	IO	N	LVDS	LVDS Transmit Channel 1 Negative
PA24	AP_LVDS_TN2	1V8	LVDS_TN2	S	IO	N	LVDS	LVDS Transmit Channel 2 Negative
PA25	AP_LVDS_TNCLK	1V8	LVDS_TNCLK	S	IO	N	LVDS	LVDS Transmit Negative Clock
PA26	AP_LVDS_TN3	1V8	LVDS_TN3	S	IO	N	LVDS	LVDS Transmit Channel 3 Negative
PA27	AP_LVDS_TN4	1V8	LVDS_TN4	S	IO	N	LVDS	LVDS Transmit Channel 4 Negative
PA28	GND	0V0	GND	G	-	-	GND	Ground
PA29	AP_HDMI_CEC	3V3	SA3	S	IO	N	HDMI	HDMI Consumer Electronics Control
PA30	AP_HDMI_TX2N	1V8	HDMI_TXN2	S	O	N	HDMI	HDMI Transmit Channel 1 Negative
PA31	AP_HDMI_TX1N	1V8	HDMI_TXN1	S	O	N	HDMI	HDMI Transmit Channel 0 Negative
PA32	AP_HDMI_TX0N	1V8	HDMI_TXN0	S	O	N	HDMI	HDMI Transmit Channel 2 Negative
PA33	AP_HDMI_TXCN	1V8	HDMI_TXNCLK	S	O	N	HDMI	HDMI Transmit Negative Clock
PA34	GND	0V0	GND	G	-	-	GND	Ground
PA35	AP_OTG_DM	3V3	USB2.0OTG_DM	S	IO	N	USB OTG	USB OTG Data Minus
PA36	AP_USBH_DM	3V3	USB2.0HOST_DM	S	IO	N	USB HOST	USB HOST Data Plus
PA37	AP_GPA13	3V3	GPIOA13	S	IO	N	GPIO	Generic GPIO
PA38	AP_HSIC_STROBE	1V2	USBHSIC_STROBE	S	IO	N	HSIC	HSIC Strobe
PA39	AP_GPA14	3V3	GPIOA14	S	IO	N	GPIO	Generic GPIO
PA40	AP_GPA9	3V3	GPIOA9	S	IO	N	GPIO	Generic GPIO
PA41	AP_GPA15	3V3	GPIOA15	S	IO	N	GPIO	Generic GPIO
PA42	AP_GPA12	3V3	GPIOA12	S	IO	N	GPIO	Generic GPIO
PB1	GND	0V0	GND	G	-	-	GND	Ground
PB2	GMAC_TXD0	3V3	GMAC_TXD0	S	IO	N	GMAC	GMAC Transmit Data 0
PB3	GMAC_TXD2	3V3	GMAC_TXD2	S	IO	N	GMAC	GMAC Transmit Data 2

BALL	BALL Name	Power	Default	Type	I/O	PU/PD	Group	Function
PB4	GMAC_MDC	3V3	GMAC_MDC	S	IO	N	GMAC	GMAC MDC
PB5	GMAC_RXCLK	3V3	GMAC_RXCLK	S	IO	N	GMAC	GMAX Receive Clock
PB6	GMAC_RXD3	3V3	GMAC_RXD3	S	IO	N	GMAC	GMAC Receive Data 3
PB7	GMAC_RXD1	3V3	GMAC_RXD1	S	IO	N	GMAC	GMAC Receive Data 1
PB8	GMAC_MDIO	3V3	GMAC_MDIO	S	IO	N	GMAC	GMAC MDIO
PB9	GND	0V0	GND	G	-	-	GND	Ground
PB10	AP_MIPICSI_DPCLK	1V8	MIPICSI_DPCLK	S	IO	N	CSI	MIPI CSI Data Positive Clock
PB11	AP_MIPICSI_DP0	1V8	MIPICSI_DP0	S	IO	N	CSI	MIPI CSI Data Positive 0
PB12	AP_MIPICSI_DP1	1V8	MIPICSI_DP1	S	IO	N	CSI	MIPI CSI Data Positive 1
PB13	AP_MIPICSI_DP2	1V8	MIPICSI_DP2	S	IO	N	CSI	MIPI CSI Data Positive 2
PB14	AP_MIPICSI_DP3	1V8	MIPICSI_DP3	S	IO	N	CSI	MIPI CSI Data Positive 3
PB15	GND	0V0	GND	G	-	-	GND	Ground
PB16	AP_MIPIDSI_DPCLK	1V8	MIPIDSI_DPCLK	S	IO	N	DSI	MIPI DSI Data Positive Clock
PB17	AP_MIPIDSI_DP0	1V8	MIPIDSI_DP0	S	IO	N	DSI	MIPI DSI Data Positive 0
PB18	AP_MIPIDSI_DP1	1V8	MIPIDSI_DP1	S	IO	N	DSI	MIPI DSI Data Positive 1
PB19	AP_MIPIDSI_DP2	1V8	MIPIDSI_DP2	S	IO	N	DSI	MIPI DSI Data Positive 2
PB20	AP_MIPIDSI_DP3	1V8	MIPIDSI_DP3	S	IO	N	DSI	MIPI DSI Data Positive 3
PB21	GND	0V0	GND	G	-	-	GND	Ground
PB22	AP_LVDS_TP0	1V8	LVDS_TP0	S	IO	N	LVDS	LVDS Transmit Channel 0 Positive
PB23	AP_LVDS_TP1	1V8	LVDS_TP1	S	IO	N	LVDS	LVDS Transmit Channel 1 Positive
PB24	AP_LVDS_TP2	1V8	LVDS_TP2	S	IO	N	LVDS	LVDS Transmit Channel 2 Positive
PB25	AP_LVDS_TPCLK	1V8	LVDS_TPCLK	S	IO	N	LVDS	LVDS Transmit Positive Clock
PB26	AP_LVDS_TP3	1V8	LVDS_TP3	S	IO	N	LVDS	LVDS Transmit Channel 3 Positive
PB27	AP_LVDS_TP4	1V8	LVDS_TP4	S	IO	N	LVDS	LVDS Transmit Channel 4 Positive
PB28	GND	0V0	GND	G	-	-	GND	Ground
PB29	AP_HDMI_HPD	3V3	HDMI_HOT5V	S	I	N	HDMI	HDMI Hot 5V
PB30	AP_HDMI_TX2P	1V8	HDMI_TXP2	S	O	N	HDMI	HDMI Transmit Channel 1 Positive
PB31	AP_HDMI_TX1P	1V8	HDMI_TXP1	S	O	N	HDMI	HDMI Transmit Channel 0 Positive
PB32	AP_HDMI_TX0P	1V8	HDMI_TXP0	S	O	N	HDMI	HDMI Transmit Channel 2 Positive
PB33	AP_HDMI_TXCP	1V8	HDMI_TXPCLK	S	O	N	HDMI	HDMI Transmit Positive Clock
PB34	GND	0V0	GND	G	-	-	GND	Ground
PB35	AP_OTG_DP	3V3	USB2.0OTG_DP	S	IO	N	USB OTG	USB OTG Data Plus
PB36	AP_USBH_DP	3V3	USB2.0HOST_DP	S	IO	N	USB HOST	USB HOST Data Minus
PB37	AP_OTG_ID	-	USB2.0OTG_ID	S	IO	N	USB HOST	USB HOST ID
PB38	AP_HSIC_DATA	1V2	USBHSIC_DATA	S	IO	N	HSIC	HSIC Data
PB39	AP_GPA4	3V3	GPIOA4	S	IO	N	GPIO	Generic GPIO
PB40	AP_GPA5	3V3	GPIOA5	S	IO	N	GPIO	Generic GPIO
PB41	AP_GPA16	3V3	GPIOA16	S	IO	N	GPIO	Generic GPIO
PB42	AP_GPA11	3V3	GPIOA11	S	IO	N	GPIO	Generic GPIO

SOUTH BALL ARRAY

Table 3. SOUTH BALL ARRAY

BALL	BALL Name	Power	Default	Type	I/O	PU/PD	Group	Function
PAK1	AP_I2S0_DOUT	3V3	I2SDOUT0	S	IO	N	I2S0	I2S 0 Data Out
PAK2	AP_I2S0_BCLK	3V3	I2SBCLK0	S	IO	N	I2S0	I2S 0 Bit Clock
PAK3	AP_GPC11_SPI2_MISO	3V3	SPIRXD2	S	IO	N	SPI2	SPI 2 Receive Data
PAK4	AP_GPC9_SPI2_CLK	3V3	SPICLK2	S	IO	N	SPI2	SPI 2 Clock
PAK5	AP_SPI0_MISO	3V3	GPIOD0	S	IO	N	SPI0	SPI 0 Receive Data
PAK6	AP_SPI0_CLK	3V3	GPIOC29	S	IO	N	SPI0	SPI 0 Clock
PAK7	AP_GPC14_PWM2	3V3	PWM2	S	IO	N	PWM	PWM 2
PAK8	AP_GPD6_SCL2	3V3	SCL2	S	IO	PU	I2C	I2C SCL 2
PAK9	AP_GPD4_SCL1	3V3	SCL1	S	IO	PU	I2C	I2C SCL 1
PAK10	AP_GPD2_SCL0	3V3	SCL0	S	IO	PU	I2C	I2C SCL 0
PAK11	AP_GPA23_HDMI_I2C_SCL	3V3	GPIOA23	S	IO	N	I2C	HDMI I2C SCL
PAK12	ZB_DEBUG_TDO_SWO	3V3	-	-	-	-	ZIGBEE	ZIGBEE Debug
PAK13	ZB_PTI_DATA_FRC_DOUT	3V3	-	-	-	-	ZIGBEE	ZIGBEE Debug
PAK14	ZB_DEBUG_TCK_SWCLK	3V3	-	-	-	-	ZIGBEE	ZIGBEE Debug
PAK15	COMBO_ZIG_UART_TXD	3V3	-	S	IO	-	ZIGBEE	ZIGBEE UART
PAK16	GND	0V0	GND	G	-	-	GND	Ground
PAK17	VCC3P3_SYS	3V3	-	P	O	-	POWER	DCDC3, VCC 3V3 Power
PAK18	VCC3P3_SYS	3V3	-	P	O	-	POWER	DCDC3, VCC 3V3 Power
PAK19	AP_GPD28	3V3	GPIOD28	S	IO	N	GPIO	Generic GPIO
PAK20	AP_GPE2	3V3	GPIOE2	S	IO	N	GPIO	Generic GPIO
PAK21	AP_GPE1	3V3	GPIOE1	S	IO	N	GPIO	Generic GPIO
PAK22	AP_UART_TX3	3V3	UARTTXD3	S	IO	N	UART	UART Transmit Data 3
PAK23	AP_UART_TX4	3V3	UARTTXD4	S	IO	N	UART	UART Transmit Data 4
PAK24	AP_UART_TX0	3V3	GPIOD18	S	IO	N	UART	UART Transmit Data 0
PAK25	AP_GPB0_VID1_1_I2SLRCK1	3V3	GPIOB0	S	IO	PU	I2S1	I2S 1 Left Right Clock
PAK26	AP_GPA28_I2SMCLK1	3V3	GPIOA28	S	IO	N	I2S1	I2S 1 Master Clock
PAK27	AP_GPA30_VID1_0_I2SBCLK1	3V3	GPIOA30	S	IO	PU	I2S1	I2S 1 Bit Clock
PAK28	AP_SD0_CMD	3V3	SDCMD0	S	IO	N	SD/MMC	SD Command
PAK29	AP_SD0_D1	3V3	SDDAT0_1	S	IO	N	SD/MMC	SD Data 1
PAK30	AP_SD0_CLK	3V3	SDCLK0	S	IO	N	SD/MMC	SD Clock
PAK31	NC	-	-	-	-	-	NC	NA
PAK32	AP_GPB13_SD0_BOOT	3V3	SD0	S	IO	PU	BOOTING	Select Booting Scenario
PAK33	AP_GPC17	3V3	GPIOC17	S	IO	N	GPIO	Generic GPIO
PAK34	AP_GPC0	3V3	GPIOC0	S	IO	N	GPIO	Generic GPIO
PAK35	AP_GPC26	3V3	GPIOC26	S	IO	PU	GPIO	Generic GPIO
PAK36	AP_GPB8	3V3	GPIOB8	S	IO	N	GPIO	Generic GPIO
PAK37	AP_GPB14	3V3	GPIOB14	S	IO	N	GPIO	Generic GPIO
PAK38	AP_GPA20	3V3	GPIOA20	S	IO	N	GPIO	Generic GPIO
PAK39	AP_GPA18	3V3	GPIOA18	S	IO	N	GPIO	Generic GPIO
PAK40	AP_GPA21	3V3	GPIOA21	S	IO	N	GPIO	Generic GPIO
PAK41	AP_GPA10	3V3	GPIOA10	S	IO	N	GPIO	Generic GPIO
PAK42	AP_GPA6	3V3	GPIOA6	S	IO	N	GPIO	Generic GPIO
PAL1	AP_I2S0_DIN	3V3	I2SDIN0	S	IO	N	I2S0	I2S 0 Data In
PAL2	AP_I2S0_MCLK	3V3	I2SMCLK0	S	IO	N	I2S0	I2S 0 Master Clock
PAL3	AP_GPC12_SPI2_MOSI	3V3	SPITXD2	S	IO	N	SPI2	SPI 2 Transmit Data
PAL4	AP_GPC10_SPI2_CS	3V3	SPIFRM2	S	IO	PU	SPI2	SPI 2 Frame
PAL5	AP_SPI0_MOSI	3V3	GPIOC31	S	IO	N	SPI0	SPI 0 Transmit Data

BALL	BALL Name	Power	Default	Type	I/O	PU/PD	Group	Function
PAL6	AP_SPI0_CS	3V3	GPIOC30	S	IO	N	SPI0	SPI 0 Frame
PAL7	AP_GPD1_PWM0	3V3	PWM0	S	IO	N	PWM	PWM 0
PAL8	AP_GPD7_SDA2	3V3	SDA2	S	IO	PU	I2C	I2C SDA
PAL9	AP_GPD5_SDA1	3V3	SDA1	S	IO	PU	I2C	I2C SDA 1
PAL10	AP_GPD3_SDA0	3V3	SDA0	S	IO	PU	I2C	I2C SDA 0
PAL11	AP_GPA24_HDMI_I2C_SDA	3V3	GPIOA24	S	IO	N	I2C	HDMI I2C SDA
PAL12	ZB_DEBUG_TMS_SWDIO	3V3	-	-	-	-	ZIGBEE	ZIGBEE Debug
PAL13	ZB_PTI_SYNC_FRC_DFRAME	3V3	-	-	-	-	ZIGBEE	ZIGBEE Debug
PAL14	PAD_ZB_RSTn	3V3	-	S	O	N	ZIGBEE	ZIGBEE Debug
PAL15	COMBO_ZIG_UART_RXD	3V3	-	S	IO	PU	ZIGBEE	ZIGBEE UART
PAL16	GND	0V0	GND	G	-	-	GND	Ground
PAL17	VCC3P3_SYS	3V3	-	P	O	-	POWER	DCDC3, VCC 3V3 Power
PAL18	VCC3P3_SYS	3V3	-	P	O	-	POWER	DCDC3, VCC 3V3 Power
PAL19	AP_VDDPWRON	3V3	VDDPWRON	S	O	N	MISC	VDD Power On
PAL20	AP_GPE3	3V3	GPIOE3	S	IO	N	GPIO	Generic GPIO
PAL21	AP_GPE0	3V3	GPIOE0	S	IO	N	GPIO	Generic GPIO
PAL22	AP_UART_RX3	3V3	UARTRXD3	S	IO	N	UART	UART Receive Data 3
PAL23	AP_UART_RX4	3V3	UARTRXD4	S	IO	N	UART	UART Receive Data 4
PAL24	AP_UART_RX0	3V3	GPIOD14	S	IO	N	UART	UART Receive Data 0
PAL25	AP_GPD31	3V3	GPIOD31	S	IO	N	GPIO	Generic GPIO
PAL26	AP_GPB9_I2SDIN1	3V3	GPIOB9	S	IO	N	I2S1	I2S 1 Data In
PAL27	AP_GPB6_VID1_4_I2SDOUT1	3V3	GPIOB6	S	IO	PD	I2S1	I2S 1 Data Out
PAL28	AP_SD0_D3	3V3	SDDAT0_3	S	IO	N	SD/MMC	SD Data 3
PAL29	AP_SD0_D2	3V3	SDDAT0_2	S	IO	N	SD/MMC	SD Data 2
PAL30	AP_SD0_D0	3V3	SDDAT0_0	S	IO	N	SD/MMC	SD Data 0
PAL31	AP_GPB4_VID1_3_BOOT	3V3	VID1_3	S	IO	PU	BOOTING	Select Booting Scenario
PAL32	AP_GPB15_SD1_BOOT	3V3	SD1	S	IO	PD	BOOTING	Select Booting Scenario
PAL33	AP_GPD8	3V3	GPIOD8	S	IO	N	GPIO	Generic GPIO
PAL34	AP_GPE30	3V3	GPIOE30	S	IO	PU	GPIO	Generic GPIO
PAL35	AP_GPC27	3V3	GPIOC27	S	IO	PU	GPIO	Generic GPIO
PAL36	AP_GPB22	3V3	GPIOB22	S	IO	N	GPIO	Generic GPIO
PAL37	AP_GPB16	3V3	GPIOB16	S	IO	N	GPIO	Generic GPIO
PAL38	AP_GPB23	3V3	GPIOB23	S	IO	N	GPIO	Generic GPIO
PAL39	AP_GPA22	3V3	GPIOA22	S	IO	N	GPIO	Generic GPIO
PAL40	AP_GPA19	3V3	GPIOA19	S	IO	N	GPIO	Generic GPIO
PAL41	AP_GPA17	3V3	GPIOA17	S	IO	N	GPIO	Generic GPIO
PAL42	AP_GPA3	3V3	GPIOA3	S	IO	N	GPIO	Generic GPIO

EAST BALL ARRAY

Table 4. EAST BALL ARRAY

BALL	BALL Name	Power	Default	Type	I/O	PU/PD	Group	Function
PC1	GND	0V0	GND	G	-	-	GND	Ground
PC2	NO BALL	-	-	-	-	-	NO BALL	-
PD1	GND	0V0	GND	G	-	-	GND	Ground
PD2	NO BALL	-	-	-	-	-	NO BALL	-
PE1	GND	0V0	GND	G	-	-	GND	Ground
PE2	GND	0V0	GND	G	-	-	GND	Ground
PF1	GND	0V0	GND	G	-	-	GND	Ground
PF2	GND	0V0	GND	G	-	-	GND	Ground
PG1	GND	0V0	GND	G	-	-	GND	Ground
PG2	NO BALL	-	-	-	-	-	NO BALL	-
PH1	GND	0V0	GND	G	-	-	GND	Ground
PH2	NO BALL	-	-	-	-	-	NO BALL	-
PJ1	GND	0V0	GND	G	-	-	GND	Ground
PJ2	GND	0V0	GND	G	-	-	GND	Ground
PK1	GND	0V0	GND	G	-	-	GND	Ground
PK2	GND	0V0	GND	G	-	-	GND	Ground
PL1	GND	0V0	GND	G	-	-	GND	Ground
PL2	GND	0V0	GND	G	-	-	GND	Ground
PM1	GND	0V0	GND	G	-	-	GND	Ground
PM2	GND	0V0	GND	G	-	-	GND	Ground
PN1	GND	0V0	GND	G	-	-	GND	Ground
PN2	GND	0V0	GND	G	-	-	GND	Ground
PP1	GND	0V0	GND	G	-	-	GND	Ground
PP2	NO BALL	-	-	-	-	-	NO BALL	-
PR1	GND	0V0	GND	G	-	-	GND	Ground
PR2	GND	0V0	GND	G	-	-	GND	Ground
PT1	GND	0V0	GND	G	-	-	GND	Ground
PT2	GND	0V0	GND	G	-	-	GND	Ground
PU1	GND	0V0	GND	G	-	-	GND	Ground
PU2	NO BALL	-	-	-	-	-	NO BALL	-
PV1	GND	0V0	GND	G	-	-	GND	Ground
PV2	NO BALL	-	-	-	-	-	NO BALL	-
PW1	AP_ADC4	1V8	ADC4	S	IO	N	ADC	ADC Channel 4
PW2	AP_ADC5	1V8	ADC5	S	IO	N	ADC	ADC Channel 5
PY1	AP_ADC0	1V8	ADC0	S	IO	N	ADC	ADC Channel 0
PY2	AP_ADC1	1V8	ADC1	S	IO	N	ADC	ADC Channel 1
PAA1	AP_ADC2	1V8	ADC2	S	IO	N	ADC	ADC Channel 2
PAA2	AP_ADC3	1V8	ADC3	S	IO	N	ADC	ADC Channel 3
PAB1	GND	0V0	GND	G	-	-	GND	Ground
PAB2	GND	0V0	GND	G	-	-	GND	Ground
PAC1	AP_TCK	3V3	TCLK	S	GPIO	PD	JTAG	JTAG TCK
PAC2	AP_TMS	3V3	TMS	S	GPIO	PU	JTAG	JTAG TMS
PAD1	AP_TDO	3V3	TDO	S	GPIO	N	JTAG	JTAG TDO
PAD2	AP_TDI	3V3	TDI	S	GPIO	PU	JTAG	JTAG TDI
PAE1	AP_NTRST	3V3	NTRST	S	GPIO	PD	JTAG	JTAG NTRST
PAE2	AP_AGP2_RTC_INT_N	3V3	ALIVEGPIO2	S	IO	N	ALIVE	AliveGPIO
PAF1	AP_PWRKEY	3V3	ALIVEGPIO0	S	IO	N	ALIVE	Power Key part of AliveGPIO
PAF2	AP_AGP1	3V3	ALIVEGPIO1	S	IO	N	ALIVE	AliveGPIO

BALL	BALL Name	Power	Default	Type	I/O	PU/PD	Group	Function
PAG1	AP_NRESET	3V3	nRESET	S	I	PU	MISC	Reset
PAG2	AP_GPA25	3V3	GPIOA25	S	IO	N	GPIO	Generic GPIO
PAH1	AP_GPA26	3V3	GPIOA26	S	IO	N	GPIO	Generic GPIO
PAH2	AP_GPA0	3V3	GPIOA0	S	IO	N	GPIO	Generic GPIO
PAJ1	AP_I2S0_LRCLK	3V3	I2SLRCLK0	S	IO	N	I2S0	I2S 0 Left Right Clock
PAJ2	AP_GPA27	3V3	GPIOA27	S	IO	N	I2S0	Generic GPIO

WEST BALL ARRAY

Table 5. RIGHT BALL ARRAY

BALL	BALL Name	Power	Default	Type	I/O	PU/PD	Group	Function
PC39	GND	0V0	GND	G	-	-	GND	Ground
PC40	GND	0V0	GND	G	-	-	GND	Ground
PC41	GND	0V0	GND	G	-	-	GND	Ground
PC42	GND	0V0	GND	G	-	-	GND	Ground
PD41	VCC5P0_OTGVBUS	-	-	P	I	-	POWER	USB2.0 OTG BUS Power
PD42	VCC5P0_OTGVBUS	-	-	P	I	-	POWER	USB2.0 OTG BUS Power
PE41	NC	-	-	-	-	-	NC	NA
PE42	NC	-	-	-	-	-	NC	NA
PF41	NC	-	-	-	-	-	NC	NA
PF42	GND	0V0	GND	G	-	-	GND	Ground
PG41	GND	0V0	GND	G	-	-	GND	Ground
PG42	GND	0V0	GND	G	-	-	GND	Ground
PH41	NC	-	-	-	-	-	NC	NA
PH42	NC	-	-	-	-	-	NC	NA
PJ41	NC	-	-	-	-	-	NC	NA
PJ42	GND	0V0	GND	G	-	-	GND	Ground
PK41	GND	0V0	GND	G	-	-	GND	Ground
PK42	GND	0V0	GND	G	-	-	GND	Ground
PL41	GND	0V0	GND	G	-	-	GND	Ground
PL42	GND	0V0	GND	G	-	-	GND	Ground
PM41	GND	0V0	GND	G	-	-	GND	Ground
PM42	GND	0V0	GND	G	-	-	GND	Ground
PN41	GND	0V0	GND	G	-	-	GND	Ground
PN42	GND	0V0	GND	G	-	-	GND	Ground
PP41	AP_GPB30	3V3	GPIOB30	S	IO	-	GPIO	Generic GPIO
PP42	GND	0V0	GND	G	-	-	GND	Ground
PR41	NC	-	-	-	-	-	NC	NA
PR42	NC	-	-	-	-	-	NC	NA
PT41	GND	0V0	GND	G	-	-	GND	Ground
PT42	GND	0V0	GND	G	-	-	GND	Ground
PU41	GND	0V0	GND	G	-	-	GND	Ground
PU42	GND	0V0	GND	G	-	-	GND	Ground
PV41	VIN	3.7~5.0	-	P	I	-	POWER	Main Power Supply for Module
PV42	VIN	3.7~5.0	-	P	I	-	POWER	Main Power Supply for Module
PW41	VIN	3.7~5.0	-	P	I	-	POWER	Main Power Supply for Module
PW42	VIN	3.7~5.0	-	P	I	-	POWER	Main Power Supply for Module
PY41	VIN	3.7~5.0	-	P	I	-	POWER	Main Power Supply for Module
PY42	VIN	3.7~5.0	-	P	I	-	POWER	Main Power Supply for Module
PAA41	VIN	3.7~5.0	-	P	I	-	POWER	Main Power Supply for Module
PAA42	VIN	3.7~5.0	-	P	I	-	POWER	Main Power Supply for Module
PAB41	VIN	3.7~5.0	-	P	I	-	POWER	Main Power Supply for Module
PAB42	VIN	3.7~5.0	-	P	I	-	POWER	Main Power Supply for Module
PAC41	GND	0V0	GND	G	-	-	GND	Ground
PAC42	GND	0V0	GND	G	-	-	GND	Ground
PAD41	NC	-	-	-	-	-	NC	NA
PAD42	NC	-	-	-	-	-	NC	NA
PAE41	GND	0V0	GND	G	-	-	GND	Ground
PAE42	NC	-	-	-	-	-	NC	NA

BALL	BALL Name	Power	Default	Type	I/O	PU/PD	Group	Function
PAF41	GND	0V0	GND	G	-	-	GND	Ground
PAF42	GND	0V0	GND	G	-	-	GND	Ground
PAG41	AP_GPB11	3V3	CLE0	S	GPIO	N	GPIO	Generic GPIO
PAG42	AP_GPB18	3V3	GPIOB18	S	GPIO	N	GPIO	Generic GPIO
PAH41	AP_GPC25	3V3	GPIOC25	S	GPIO	PU	GPIO	Generic GPIO
PAH42	AP_GPE31	3V3	GPIOE31	S	GPIO	PU	GPIO	Generic GPIO
PAJ39	BT_PCM_CLK	3V3	-	S	IO	N	BT PCM	PCM Clock
PAJ40	BT_PCM_D_IN	3V3	-	S	I	N	BT PCM	PCM Data In
PAJ41	BT_PCM_D_OUT	3V3	-	S	O	N	BT PCM	PCM Data Out
PAJ42	BT_PCM_LRCK	3V3	-	S	IO	N	BT PCM	PCM LR Clock

CENTER BALL ARRAY

Table 6. Center Ball Array

BALL	BALL Name	Power	Default	Type	I/O	PU/PD	Group	Function
TP282	GND	0V0	GND	NA	0V0	-	GND	Ground
TP283	GND	0V0	GND	NA	0V0	-	GND	Ground
TP284	GND	0V0	GND	NA	0V0	-	GND	Ground
TP285	GND	0V0	GND	NA	0V0	-	GND	Ground
TP286	GND	0V0	GND	NA	0V0	-	GND	Ground
TP287	GND	0V0	GND	NA	0V0	-	GND	Ground
TP288	GND	0V0	GND	NA	0V0	-	GND	Ground
TP289	GND	0V0	GND	NA	0V0	-	GND	Ground
TP290	GND	0V0	GND	NA	0V0	-	GND	Ground
TP291	GND	0V0	GND	NA	0V0	-	GND	Ground
TP292	GND	0V0	GND	NA	0V0	-	GND	Ground
TP293	GND	0V0	GND	NA	0V0	-	GND	Ground
TP294	GND	0V0	GND	NA	0V0	-	GND	Ground
TP295	GND	0V0	GND	NA	0V0	-	GND	Ground
TP296	GND	0V0	GND	NA	0V0	-	GND	Ground
TP297	GND	0V0	GND	NA	0V0	-	GND	Ground
TP298	GND	0V0	GND	NA	0V0	-	GND	Ground
TP299	GND	0V0	GND	NA	0V0	-	GND	Ground
TP300	GND	0V0	GND	NA	0V0	-	GND	Ground
TP301	GND	0V0	GND	NA	0V0	-	GND	Ground

FUNCTIONAL INTERFACES

This section shows the functional interfaces that are available at the PADs of the ARTIK 530 Module. The functions provided are related to the development environment used. Depending on your project you can always choose to reprogram some of the GPIOs that are currently assigned to the pre-defined functional interfaces.

ADC

Table 7. ADC

Ball Loc	Ball Name	Power	I/O Type	I/O	PU/PD	Function
PW1	AP_ADC4	1V8	S	IO	N	ADC Channel 4
PW2	AP_ADC5	1V8	S	IO	N	ADC Channel 5
PY1	AP_ADC0	1V8	S	IO	N	ADC Channel 0
PY2	AP_ADC1	1V8	S	IO	N	ADC Channel 1
PAA1	AP_ADC2	1V8	S	IO	N	ADC Channel 2
PAA2	AP_ADC3	1V8	S	IO	N	ADC Channel 3

BOOTING

Table 8. Booting

Ball Loc	Ball Name	Power	I/O Type	I/O	PU/PD	Function
PAK32	AP_GPB13_SD0_BOOT	3V3	S	IO	PU	Select Booting Scenario
PAL31	AP_GPB4_VID1_3_BOOT	3V3	S	IO	PU	Select Booting Scenario
PAL32	AP_GPB15_SD1_BOOT	3V3	S	IO	PD	Select Booting Scenario

BLUETOOTH® PCM

Table 9. Bluetooth® PCM

Ball Loc	Ball Name	Power	I/O Type	I/O	PU/PD	Function
PAJ39	BT_PCM_CLK	3V3	S	IO	N	PCM Clock
PAJ40	BT_PCM_D_IN	3V3	S	I	N	PCM Data In
PAJ41	BT_PCM_D_OUT	3V3	S	O	N	PCM Data Out
PAJ42	BT_PCM_LRCK	3V3	S	IO	N	PCM LR Clock

MIPI CSI

Table 10. MIPI CSI

Ball Loc	Ball Name	Power	I/O Type	I/O	PU/PD	Function
PA10	AP_MIPICSI_DNCLK	1V8	S	IO	N	MIPI CSI Data Negative Clock
PA11	AP_MIPICSI_DN0	1V8	S	IO	N	MIPI CSI Data Negative 0
PA12	AP_MIPICSI_DN1	1V8	S	IO	N	MIPI CSI Data Negative 1
PA13	AP_MIPICSI_DN2	1V8	S	IO	N	MIPI CSI Data Negative 2
PA14	AP_MIPICSI_DN3	1V8	S	IO	N	MIPI CSI Data Negative 3
PB10	AP_MIPICSI_DPCLK	1V8	S	IO	N	MIPI CSI Data Positive Clock
PB11	AP_MIPICSI_DP0	1V8	S	IO	N	MIPI CSI Data Positive 0
PB12	AP_MIPICSI_DP1	1V8	S	IO	N	MIPI CSI Data Positive 1
PB13	AP_MIPICSI_DP2	1V8	S	IO	N	MIPI CSI Data Positive 2
PB14	AP_MIPICSI_DP3	1V8	S	IO	N	MIPI CSI Data Positive 3

MIPI DSI

Table 11. MIPI DSI

Ball Loc	Ball Name	Power	I/O Type	I/O	PU/PD	Function
PA16	AP_MIPIDSI_DNCLK	1V8	S	IO	N	MIPI DSI Data Negative Clock
PA17	AP_MIPIDSI_DN0	1V8	S	IO	N	MIPI DSI Data Negative 0
PA18	AP_MIPIDSI_DN1	1V8	S	IO	N	MIPI DSI Data Negative 1
PA19	AP_MIPIDSI_DN2	1V8	S	IO	N	MIPI DSI Data Negative 2
PA20	AP_MIPIDSI_DN3	1V8	S	IO	N	MIPI DSI Data Negative 3
PB16	AP_MIPIDSI_DPCLK	1V8	S	IO	N	MIPI DSI Data Positive Clock
PB17	AP_MIPIDSI_DP0	1V8	S	IO	N	MIPI DSI Data Positive 0
PB18	AP_MIPIDSI_DP1	1V8	S	IO	N	MIPI DSI Data Positive 1
PB19	AP_MIPIDSI_DP2	1V8	S	IO	N	MIPI DSI Data Positive 2
PB20	AP_MIPIDSI_DP3	1V8	S	IO	N	MIPI DSI Data Positive 3

GMAC

Table 12. GMAC

Ball Loc	Ball Name	Power	I/O Type	I/O	PU/PD	Function
PA1	GMAC_TXEN	3V3	S	IO	N	GMAC Transmit Enable
PA2	GMAC_TXD1	3V3	S	IO	N	GMAC Transmit Data 1
PA3	GMAC_TXD3	3V3	S	IO	N	GMAC Transmit Data 3
PA5	GMAC_GTXCLK	3V3	S	IO	N	GMAC Transmit Clock
PA6	GMAC_RXDV	3V3	S	IO	N	GMAC Receive Enable
PA7	GMAC_RXD2	3V3	S	IO	N	GMAC Receive Data 2
PA8	GMAC_RXD0	3V3	S	IO	N	GMAC Receive Data 0
PB2	GMAC_TXD0	3V3	S	IO	N	GMAC Transmit Data 0
PB3	GMAC_TXD2	3V3	S	IO	N	GMAC Transmit Data 2
PB4	GMAC_MDC	3V3	S	IO	N	GMAC MDC
PB5	GMAC_RXCLK	3V3	S	IO	N	GMAX Receive Clock
PB6	GMAC_RXD3	3V3	S	IO	N	GMAC Receive Data 3
PB7	GMAC_RXD1	3V3	S	IO	N	GMAC Receive Data 1
PB8	GMAC_MDIO	3V3	S	IO	N	GMAC MDIO

GPIO

Table 13. GPIO

Ball Loc	Ball Name	Power	I/O Type	I/O	PU/PD	Function
PA37	AP_GPA13	3V3	S	IO	N	Generic GPIO
PA39	AP_GPA14	3V3	S	IO	N	Generic GPIO
PA40	AP_GPA9	3V3	S	IO	N	Generic GPIO
PA41	AP_GPA15	3V3	S	IO	N	Generic GPIO
PA42	AP_GPA12	3V3	S	IO	N	Generic GPIO
PB39	AP_GPA4	3V3	S	IO	N	Generic GPIO
PB40	AP_GPA5	3V3	S	IO	N	Generic GPIO
PB41	AP_GPA16	3V3	S	IO	N	Generic GPIO
PB42	AP_GPA11	3V3	S	IO	N	Generic GPIO
PP41	AP_GPB30	3V3	S	IO	-	Generic GPIO
PAG41	AP_GPB11	3V3	S	GPIO	N	Generic GPIO
PAG42	AP_GPB18	3V3	S	GPIO	N	Generic GPIO
PAH41	AP_GPC25	3V3	S	GPIO	PU	Generic GPIO
PAH42	AP_GPE31	3V3	S	GPIO	PU	Generic GPIO
PAK19	AP_GPD28	3V3	S	IO	N	Generic GPIO
PAK20	AP_GPE2	3V3	S	IO	N	Generic GPIO
PAK21	AP_GPE1	3V3	S	IO	N	Generic GPIO
PAK33	AP_GPC17	3V3	S	IO	N	Generic GPIO
PAK34	AP_GPC0	3V3	S	IO	N	Generic GPIO
PAK35	AP_GPC26	3V3	S	IO	PU	Generic GPIO
PAK36	AP_GPB8	3V3	S	IO	N	Generic GPIO
PAK37	AP_GPB14	3V3	S	IO	N	Generic GPIO
PAK38	AP_GPA20	3V3	S	IO	N	Generic GPIO
PAK39	AP_GPA18	3V3	S	IO	N	Generic GPIO
PAK40	AP_GPA21	3V3	S	IO	N	Generic GPIO
PAK41	AP_GPA10	3V3	S	IO	N	Generic GPIO
PAK42	AP_GPA6	3V3	S	IO	N	Generic GPIO
PAL20	AP_GPE3	3V3	S	IO	N	Generic GPIO
PAL21	AP_GPE0	3V3	S	IO	N	Generic GPIO
PAL25	AP_GPD31	3V3	S	IO	N	Generic GPIO
PAL33	AP_GPD8	3V3	S	IO	N	Generic GPIO
PAL34	AP_GPE30	3V3	S	IO	PU	Generic GPIO
PAL35	AP_GPC27	3V3	S	IO	PU	Generic GPIO
PAL36	AP_GPB22	3V3	S	IO	N	Generic GPIO
PAL37	AP_GPB16	3V3	S	IO	N	Generic GPIO
PAL38	AP_GPB23	3V3	S	IO	N	Generic GPIO
PAL39	AP_GPA22	3V3	S	IO	N	Generic GPIO
PAL40	AP_GPA19	3V3	S	IO	N	Generic GPIO
PAL41	AP_GPA17	3V3	S	IO	N	Generic GPIO
PAL42	AP_GPA3	3V3	S	IO	N	Generic GPIO
PAG2	AP_GPA25	3V3	S	IO	N	Generic GPIO
PAH1	AP_GPA26	3V3	S	IO	N	Generic GPIO
PAH2	AP_GPA0	3V3	S	IO	N	Generic GPIO
PAJ2	AP_GPA27	3V3	S	IO	N	Generic GPIO

HDMI

Table 14. HDMI

Ball Loc	Ball Name	Power	I/O Type	I/O	PU/PD	Function
PA29	AP_HDMI_CEC	3V3	S	IO	N	HDMI Consumer Electronics Control
PA30	AP_HDMI_TX2N	1V8	S	O	N	HDMI Transmit Channel 1 Negative
PA31	AP_HDMI_TX1N	1V8	S	O	N	HDMI Transmit Channel 0 Negative
PA32	AP_HDMI_TX0N	1V8	S	O	N	HDMI Transmit Channel 2 Negative
PA33	AP_HDMI_TXCN	1V8	S	O	N	HDMI Transmit Negative Clock
PB29	AP_HDMI_HPD	3V3	S	I	N	HDMI Hot 5V
PB30	AP_HDMI_TX2P	1V8	S	O	N	HDMI Transmit Channel 1 Positive
PB31	AP_HDMI_TX1P	1V8	S	O	N	HDMI Transmit Channel 0 Positive
PB32	AP_HDMI_TX0P	1V8	S	O	N	HDMI Transmit Channel 2 Positive
PB33	AP_HDMI_TXCP	1V8	S	O	N	HDMI Transmit Positive Clock

HSIC

Table 15. HSIC

Ball Loc	Ball Name	Power	I/O Type	I/O	PU/PD	Function
PA38	AP_HSIC_STROBE	1V2	S	IO	N	HSIC Strobe
PB38	AP_HSIC_DATA	1V2	S	IO	N	HSIC Data

I²C

Table 16. I²C

Ball Loc	Ball Name	Power	I/O Type	I/O	PU/PD	Function
PAK8	AP_GPD6_SCL2	3V3	S	IO	PU	I2C SCL
PAK9	AP_GPD4_SCL1	3V3	S	IO	PU	I2C SCL 1
PAK10	AP_GPD2_SCL0	3V3	S	IO	PU	I2C SCL 0
PAK11	AP_GPA23_HDMI_I2C_SCL	3V3	S	IO	N	HDMI I2C SCL
PAL8	AP_GPD7_SDA2	3V3	S	IO	PU	I2C SDA
PAL9	AP_GPD5_SDA1	3V3	S	IO	PU	I2C SDA 1
PAL10	AP_GPD3_SDA0	3V3	S	IO	PU	I2C SDA 0
PAL11	AP_GPA24_HDMI_I2C_SDA	3V3	S	IO	N	HDMI I2C SDA

I²S

Table 17. I²S

Ball Loc	Ball Name	Power	I/O Type	I/O	PU/PD	Function
PAK1	AP_I2S0_DOUT	3V3	S	IO	N	I2S 0 Data Out
PAK2	AP_I2S0_BCLK	3V3	S	IO	N	I2S 0 Bit Clock
PAK25	AP_GPB0_VID1_1_I2SLRCK1	3V3	S	IO	PU	I2S 1 Left Right Clock
PAK26	AP_GPA28_I2SMCLK1	3V3	S	IO	N	I2S 1 Master Clock
PAK27	AP_GPA30_VID1_0_I2SBCLK1	3V3	S	IO	PU	I2S 1 Bit Clock
PAL1	AP_I2S0_DIN	3V3	S	IO	N	I2S 0 Data In
PAL2	AP_I2S0_MCLK	3V3	S	IO	N	I2S 0 Master Clock
PAL26	AP_GPB9_I2SDIN1	3V3	S	IO	N	I2S 1 Data In
PAL27	AP_GPB6_VID1_4_I2SDOUT1	3V3	S	IO	PD	I2S 1 Data Out
PAJ1	AP_I2S0_LRCLK	3V3	S	IO	N	I2S 0 Left Right Clock

JTAG

Table 18. JTAG

Ball Loc	Ball Name	Power	I/O Type	I/O	PU/PD	Function
PAC1	AP_TCK	3V3	S	IO	PD	JTAG TCK
PAC2	AP_TMS	3V3	S	IO	PU	JTAG TMS
PAD1	AP_TDO	3V3	S	IO	N	JTAG TDO
PAD2	AP_TDI	3V3	S	IO	PU	JTAG TDI
PAE1	AP_NTRST	3V3	S	IO	PD	JTAG NTRST

ALIVE

Table 19. Key

Ball Loc	Ball Name	Power	I/O Type	I/O	PU/PD	Function
PAE2	AP_AGP2_RTC_INT_N	3V3	S	IO	N	AliveGPIO
PAF1	AP_PWRKEY	3V3	S	IO	N	AliveGPIO
PAF2	AP_AGP1	3V3	S	IO	N	AliveGPIO

LVDS

Table 20. LVDS

Ball Loc	Ball Name	Power	I/O Type	I/O	PU/PD	Function
PA22	AP_LVDS_TN0	1V8	S	IO	N	LVDS Transmit Channel 0 Negative
PA23	AP_LVDS_TN1	1V8	S	IO	N	LVDS Transmit Channel 1 Negative
PA24	AP_LVDS_TN2	1V8	S	IO	N	LVDS Transmit Channel 2 Negative
PA25	AP_LVDS_TNCLK	1V8	S	IO	N	LVDS Transmit Negative Clock
PA26	AP_LVDS_TN3	1V8	S	IO	N	LVDS Transmit Channel 3 Negative
PA27	AP_LVDS_TN4	1V8	S	IO	N	LVDS Transmit Channel 4 Negative
PB22	AP_LVDS_TP0	1V8	S	IO	N	LVDS Transmit Channel 0 Positive
PB23	AP_LVDS_TP1	1V8	S	IO	N	LVDS Transmit Channel 1 Positive
PB24	AP_LVDS_TP2	1V8	S	IO	N	LVDS Transmit Channel 2 Positive
PB25	AP_LVDS_TPCLK	1V8	S	IO	N	LVDS Transmit Positive Clock
PB26	AP_LVDS_TP3	1V8	S	IO	N	LVDS Transmit Channel 3 Positive
PB27	AP_LVDS_TP4	1V8	S	IO	N	LVDS Transmit Channel 4 Positive

MISCELLANEOUS

Table 21. Miscellaneous

Ball Loc	Ball Name	Power	I/O Type	I/O	PU/PD	Function
PAG1	AP_NRESET	3V3	S	I	PU	Reset
PAL19	AP_VDDPWRON	3V3	S	O	N	VDD Power On

POWER

Table 22. Power

Ball Loc	Ball Name	Power	I/O Type	I/O	PU/PD	Function
PAK17	VCC3P3_SYS*	3V3	P	O	-	POWER
PAK18	VCC3P3_SYS*	3V3	P	O	-	POWER
PAL17	VCC3P3_SYS*	3V3	P	O	-	POWER
PAL18	VCC3P3_SYS*	3V3	P	O	-	POWER
PD41	VCC5P0_OTGVBUS	-	P	I	-	POWER
PD42	VCC5P0_OTGVBUS	-	P	I	-	POWER
PV41	VIN	VBAT	P	I	-	POWER
PV42	VIN	VBAT	P	I	-	POWER
PW41	VIN	VBAT	P	I	-	POWER
PW42	VIN	VBAT	P	I	-	POWER
PY41	VIN	VBAT	P	I	-	POWER
PY42	VIN	VBAT	P	I	-	POWER
PAA41	VIN	VBAT	P	I	-	POWER
PAA42	VIN	VBAT	P	I	-	POWER
PAB41	VIN	VBAT	P	I	-	POWER
PAB42	VIN	VBAT	P	I	-	POWER

*Note: VCC3P3_SYS pads are not recommended as a current source, do not drive external Ics with these pads. VCC3P3_SYS pads turn off when the ARTIK 530 Module goes sleep mode.

PWM

Table 23. PWM

Ball Loc	Ball Name	Power	I/O Type	I/O	PU/PD	Function
PAK7	AP_GPC14_PWM2	3V3	S	IO	N	PWM 2
PAL7	AP_GPD1_PWM0	3V3	S	IO	N	PWM 0

SD/MMC

Table 24. SD/MMC

Ball Loc	Ball Name	Power	I/O Type	I/O	PU/PD	Function
PAK28	AP_SD0_CMD	3V3	S	IO	N	SD Command
PAK29	AP_SD0_D1	3V3	S	IO	N	SD Data 1
PAK30	AP_SD0_CLK	3V3	S	IO	N	SD Clock
PAL28	AP_SD0_D3	3V3	S	IO	N	SD Data 3
PAL29	AP_SD0_D2	3V3	S	IO	N	SD Data 2
PAL30	AP_SD0_D0	3V3	S	IO	N	SD Data 0

SPI

Table 25. SPI

Ball Loc	Ball Name	Power	I/O Type	I/O	PU/PD	Function
PAK3	AP_GPC11_SPI2_MISO	3V3	S	IO	N	SPI 2 Receive Data
PAK4	AP_GPC9_SPI2_CLK	3V3	S	IO	N	SPI 2 Clock
PAK5	AP_SPI0_MISO	3V3	S	IO	N	SPI 0 Receive Data
PAK6	AP_SPI0_CLK	3V3	S	IO	N	SPI 0 Clock
PAL3	AP_GPC12_SPI2_MOSI	3V3	S	IO	N	SPI 2 Transmit Data
PAL4	AP_GPC10_SPI2_CS	3V3	S	IO	PU	SPI 2 Frame
PAL5	AP_SPI0_MOSI	3V3	S	IO	N	SPI 0 Transmit Data
PAL6	AP_SPI0_CS	3V3	S	IO	N	SPI 0 Frame

UART

Table 26. UART

Ball Loc	Ball Name	Power	I/O Type	I/O	PU/PD	Function
PAK22	AP_UART_TX3	3V3	S	IO	N	UART Transmit Data 3
PAK23	AP_UART_TX4	3V3	S	IO	N	UART Transmit Data 4
PAK24	AP_UART_TX0	3V3	S	IO	N	UART Transmit Data 5
PAL22	AP_UART_RX3	3V3	S	IO	N	UART Receive Data 3
PAL23	AP_UART_RX4	3V3	S	IO	N	UART Receive Data 4
PAL24	AP_UART_RX0	3V3	S	IO	N	UART Receive Data 5

USB HOST/USB OTG

Table 27. USB Host/USB OTG

Ball Loc	Ball Name	Power	I/O Type	I/O	PU/PD	Function
PA35	AP_OTG_DM	3V3	S	IO	N	USB OTG Data Minus
PA36	AP_USBH_DM	3V3	S	IO	N	USB HOST Data Plus
PB35	AP_OTG_DP	3V3	S	IO	N	USB OTG Data Plus
PB36	AP_USBH_DP	3V3	S	IO	N	USB HOST Data Minus
PB37	AP_OTG_ID	-	S	IO	N	USB HOST ID

802.15.4

Table 28. 802.15.4

Ball Loc	Ball Name	Power	I/O Type	I/O	PU/PD	Function
PAK12	ZB_DEBUG_TDO_SWO	3V3	-	-	-	ZIGBEE Debug
PAK13	ZB_PTI_DATA_FRC_DOUT	3V3	-	-	-	ZIGBEE Debug
PAK14	ZB_DEBUG_TCK_SWCLK	3V3	-	-	-	ZIGBEE Debug
PAK15	COMBO_ZIG_UART_TXD	3V3	S	IO	-	ZIGBEE UART
PAL12	ZB_DEBUG_TMS_SWDIO	3V3	-	-	-	ZIGBEE Debug
PAL13	ZB_PTI_SYNC_FRC_DFRAME	3V3	-	-	-	ZIGBEE Debug
PAL14	PAD_ZB_RSTn	3V3	S	O	N	ZIGBEE Debug
PAL15	COMBO_ZIG_UART_RXD	3V3	S	IO	PU	ZIGBEE UART

GPIO Alternate Functions

A number of the GPIOs can be programmed to have alternate functions beyond their default behavior using the GPIO API provided in the SW development environment. *Table 29*, *Table 30*, *Table 31* and *Table 32* provide the alternate functions of all the GPIOs that are available on the PADs of the ARTIK 530 Module that can be user programmed.

Table 29. GPIO Alternate Functions NORTH PART

GPIO Alternate Functions NORTH PART								
Ball Loc	Ball Name	Default Function	I/O	Function 0	Function 1	Function 2	Function 3	Group
PA1	GMAC_TXEN	GMAC_TXEN	IO	GPIOE11	GMAC_TXEN	-	-	GMAC
PA2	GMAC_TXD1	GMAC_TXD1	IO	GPIOE8	GMAC_TXD1	-	-	GMAC
PA3	GMAC_TXD3	GMAC_TXD3	IO	GPIOE10	GMAC_TXD3	-	-	GMAC
PA5	GMAC_GTXCLK	GMAC_GTXCLK	IO	GPIOE24	GMAC_GTXCLK	-	-	GMAC
PA6	GMAC_RXDV	GMAC_RXDV	IO	GPIOE19	GMAC_RXDV	SPITXD1	-	GMAC
PA7	GMAC_RXD2	GMAC_RXD2	IO	GPIOE16	GMAC_RXD2	-	-	GMAC
PA8	GMAC_RXD0	GMAC_RXD0	IO	GPIOE14	GMAC_RXD0	SPICLK1	-	GMAC
PA29	AP_HDMI_CEC	SA3	IO	SA3	GPIOC3	HDMI_CEC	SDnRST0	HDMI
PA37	AP_GPA13	GPIOA13	IO	GPIOA13	DISD12	-	-	GPIO
PA39	AP_GPA14	GPIOA14	IO	GPIOA14	DISD13	-	-	GPIO
PA40	AP_GPA9	GPIOA9	IO	GPIOA9	DISD8	-	-	GPIO
PA41	AP_GPA15	GPIOA15	IO	GPIOA15	DISD14	-	-	GPIO
PA42	AP_GPA12	GPIOA12	IO	GPIOA12	DISD11	-	-	GPIO
PB2	GMAC_TXD0	GMAC_TXD0	IO	GPIOE7	GMAC_TXD0	VIVSYNC1	-	GMAC
PB3	GMAC_TXD2	GMAC_TXD2	IO	GPIOE9	GMAC_TXD2	-	-	GMAC
PB4	GMAC_MDC	GMAC_MDC	IO	GPIOE20	GMAC_MDC	-	-	GMAC
PB5	GMAC_RXCLK	GMAC_RXCLK	IO	GPIOE18	GMAC_RXCLK	SPIRXD1	-	GMAC
PB6	GMAC_RXD3	GMAC_RXD3	IO	GPIOE17	GMAC_RXD3	-	-	GMAC
PB7	GMAC_RXD1	GMAC_RXD1	IO	GPIOE15	GMAC_RXD1	SPIFRM1	-	GMAC
PB8	GMAC_MDIO	GMAC_MDIO	IO	GPIOE21	GMAC_MDIO	-	-	GMAC
PB39	AP_GPA4	GPIOA4	IO	GPIOA4	DISD3	-	-	GPIO
PB40	AP_GPA5	GPIOA5	IO	GPIOA5	DISD4	-	-	GPIO
PB41	AP_GPA16	GPIOA16	IO	GPIOA16	DISD15	-	-	GPIO
PB42	AP_GPA11	GPIOA11	IO	GPIOA11	DISD10	-	-	GPIO

Table 30. GPIO Alternate Functions SOUTH PART

GPIO Alternate Functions SOUTH PART								
Ball Loc	Ball Name	Default Function	I/O	Function 0	Function 1	Function 2	Function 3	Group
PAK1	AP_I2S0_DOUT	I2SDOUT0	IO	GPIOD9	I2SDOUT0	AC97_DOUT	-	I2S0
PAK2	AP_I2S0_BCLK	I2SBCLK0	IO	GPIOD10	I2SBCLK0	AC97_BCLK	-	I2S0
PAK3	AP_GPC11_SPI2_MISO	SPIRXD2	IO	SA11	GPIOC11	SPIRXD2	USB2.0OTG_DrvVBUS	SPI2
PAK4	AP_GPC9_SPI2_CLK	SPICLK2	IO	SA9	GPIOC9	SPICLK2	-	SPI2
PAK5	AP_SPI0_MISO	GPIOD0	IO	GPIOD0	SPIRXD0	PWM3	-	SPI0
PAK6	AP_SPI0_CLK	GPIOC29	IO	GPIOC29	SPICLK0	-	-	SPI0
PAK7	AP_GPC14_PWM2	PWM2	IO	SA14	GPIOC14	PWM2	VICLK2	PWM
PAK8	AP_GPD6_SCL2	SCL2	IO	GPIOD6	SCL2	-	-	I2C
PAK9	AP_GPD4_SCL1	SCL1	IO	GPIOD4	SCL1	-	-	I2C
PAK10	AP_GPD2_SCL0	SCL0	IO	GPIOD2	SCL0	ISO7816	-	I2C
PAK11	AP_GPA23_HDMI_I2C_SCL	GPIOA23	IO	GPIOA23	DISD22	-	-	I2C
PAK19	AP_GPD28	GPIOD28	IO	GPIOD28	VID0_0	TSIDATA1_0	SA24	MISC
PAK20	AP_GPE2	GPIOE2	IO	GPIOE2	VID0_6	TSIDATA1_6	-	MISC
PAK21	AP_GPE1	GPIOE1	IO	GPIOE1	VID0_5	TSIDATA1_5	-	MISC
PAK22	AP_UART_TX3	UARTTXD3	IO	GPIOD21	UARTTXD3	SDnCD1	-	UART
PAK23	AP_UART_TX4	UARTTXD4	IO	SD13	GPIOB29	TSIDATA0_5	UARTTXD4	UART
PAK24	AP_UART_TX0	GPIOD18	IO	GPIOD18	UARTTXD0	ISO7816	SDWP2	UART
PAK25	AP_GPB0_VID1_1_I2SLRCK1	GPIOB0	IO	GPIOB0	VID1_1	SDEX1	I2SLRCLK1	I2S1
PAK26	AP_GPA28_I2SMCLK1	GPIOA28	IO	GPIOA28	VICLK1	I2SMCLK2	I2SMCLK1	I2S1
PAK27	AP_GPA30_VID1_0_I2SBCLK1	GPIOA30	IO	GPIOA30	VID1_0	SDEX0	I2SBCLK1	I2S1
PAK28	AP_SD0_CMD	SDCMD0	IO	GPIOA31	SDCMD0	-	-	SD/MMC
PAK29	AP_SD0_D1	SDDAT0_1	IO	GPIOB3	SDDAT0_1	-	-	SD/MMC
PAK30	AP_SD0_CLK	SDCLK0	IO	GPIOA29	SDCLK0	-	-	SD/MMC
PAK32	AP_GPB13_SD0_BOOT	SD0	IO	SD0	GPIOB13	-	-	BOOTING
PAK33	AP_GPC17	GPIOC17	IO	SA17	GPIOC17	TSIDP0	VID2_0	GPIO
PAK34	AP_GPC0	GPIOC0	IO	SA0	GPIOC0	TSERR0	-	GPIO
PAK35	AP_GPC26	GPIOC26	IO	RDNWR	GPIOC26	-	-	GPIO
PAK36	AP_GPB8	GPIOB8	IO	GPIOB8	VID1_5	SDEX5	I2SDOUT2	GPIO
PAK37	AP_GPB14	GPIOB14	IO	RnB0	RnB1	GPIOB14	-	MISC
PAK38	AP_GPA20	GPIOA20	IO	GPIOA20	DISD19	-	-	GPIO
PAK39	AP_GPA18	GPIOA18	IO	GPIOA18	DISD17	-	-	GPIO
PAK40	AP_GPA21	GPIOA21	IO	GPIOA21	DISD20	-	-	GPIO
PAK41	AP_GPA10	GPIOA10	IO	GPIOA10	DISD9	-	-	GPIO
PAK42	AP_GPA6	GPIOA6	IO	GPIOA6	DISD5	-	-	GPIO
PAL1	AP_I2S0_DIN	I2SDIN0	IO	GPIOD11	I2SDIN0	AC97_DIN	-	I2S0
PAL2	AP_I2S0_MCLK	I2SMCLK0	IO	GPIOD13	I2SMCLK0	AC97_nRST	-	I2S0
PAL3	AP_GPC12_SPI2_MOSI	SPITXD2	IO	SA12	GPIOC12	SPITXD2	SDnRST2	SPI2
PAL4	AP_GPC10_SPI2_CS	SPIFRM2	IO	SA10	GPIOC10	SPIFRM2	-	SPI2
PAL5	AP_SPI0_MOSI	GPIOC31	IO	GPIOC31	SPITXD0	-	-	SPI0
PAL6	AP_SPI0_CS	GPIOC30	IO	GPIOC30	SPIFRM0	-	-	SPI0
PAL7	AP_GPD1_PWM0	PWM0	IO	GPIOD1	PWM0	SA25	-	PWM
PAL8	AP_GPD7_SDA2	SDA2	IO	GPIOD7	SDA2	-	-	I2C
PAL9	AP_GPD5_SDA1	SDA1	IO	GPIOD5	SDA1	-	-	I2C
PAL10	AP_GPD3_SDA0	SDA0	IO	GPIOD3	SDA0	ISO7816	-	I2C
PAL11	AP_GPA24_HDMI_I2C_SDA	GPIOA24	IO	GPIOA24	DISD23	-	-	I2C
PAL15	COMBO_ZIG_UART_RXD	NSCS1	IO	GPIOC28	NSCS1	UARTnRI1	-	802.15.4
PAL20	AP_GPE3	GPIOE3	IO	GPIOE3	VID0_7	TSIDATA1_7	-	MISC

GPIO Alternate Functions SOUTH PART								
Ball Loc	Ball Name	Default Function	I/O	Function 0	Function 1	Function 2	Function 3	Group
PAL21	AP_GPE0	GPIOE0	IO	GPIOE0	VID0_4	TSIDATA1_4	-	MISC
PAL22	AP_UART_RX3	UARTRXD3	IO	GPIOD17	UARTRXD3	-	-	UART
PAL23	AP_UART_RX4	UARTRXD4	IO	SD12	GPIOB28	TSIDATA0_4	UARTRXD4	UART
PAL24	AP_UART_RX0	GPIOD14	IO	GPIOD14	UARTRXD0	ISO7816	-	UART
PAL25	AP_GPD31	GPIOD31	IO	GPIOD31	VID0_3	TSIDATA1_3	-	MISC
PAL26	AP_GPB9_I2SDIN1	GPIOB9	IO	GPIOB9	VID1_6	SDEX6	I2SDIN1	I2S1
PAL27	AP_GPB6_VID1_4_I2SDOUT1	GPIOB6	IO	GPIOB6	VID1_4	SDEX4	I2SDOUT1	I2S1
PAL28	AP_SD0_D3	SDDAT0_3	IO	GPIOB7	SDDAT0_3	-	-	SD/MMC
PAL29	AP_SD0_D2	SDDAT0_2	IO	GPIOB5	SDDAT0_2	-	-	SD/MMC
PAL30	AP_SD0_D0	SDDAT0_0	IO	GPIOB1	SDDAT0_0	-	-	SD/MMC
PAL31	AP_GPB4_VID1_3_BOOT	VID1_3	IO	GPIOB4	VID1_3	SDEX3	I2SLRCLK2	BOOTING
PAL32	AP_GPB15_SD1_BOOT	SD1	IO	SD1	GPIOB15	-	-	BOOTING
PAL33	AP_GPD8	GPIOD8	IO	GPIOD8	PPM	-	-	GPIO
PAL34	AP_GPE30	GPIOE30	IO	NSOE	GPIOE30	-	-	GPIO
PAL35	AP_GPC27	GPIOC27	IO	NSDQM	GPIOC27	-	-	GPIO
PAL36	AP_GPB22	GPIOB22	IO	SD6	GPIOB22	-	-	GPIO
PAL37	AP_GPB16	GPIOB16	IO	NNFOE0	NNFOE1	GPIOB16	-	MISC
PAL38	AP_GPB23	GPIOB23	IO	SD7	GPIOB23	-	-	GPIO
PAL39	AP_GPA22	GPIOA22	IO	GPIOA22	DISD21	-	-	GPIO
PAL40	AP_GPA19	GPIOA19	IO	GPIOA19	DISD18	-	-	GPIO
PAL41	AP_GPA17	GPIOA17	IO	GPIOA17	DISD16	-	-	GPIO
PAL42	AP_GPA3	GPIOA3	IO	GPIOA3	DISD2	-	-	GPIO

Table 31. GPIO Alternate Functions EAST PART

GPIO Alternate Functions EAST PART								
Ball Loc	Ball Name	Default Function	I/O	Function 0	Function 1	Function 2	Function 3	Group
PAC1	AP_TCK	TCLK	IO	TCLK	GPIOE28	-	-	JTAG
PAC2	AP_TMS	TMS	IO	TMS	GPIOE26	-	-	JTAG
PAD1	AP_TDO	TDO	IO	TDO	GPIOE29	-	-	JTAG
PAD2	AP_TDI	TDI	IO	TDI	GPIOE27	-	-	JTAG
PAE1	AP_NTRST	NTRST	IO	NTRST	GPIOE25	-	-	JTAG
PAG2	AP_GPA25	GPIOA25	IO	GPIOA25	DISVSYNC	-	-	GPIO
PAH1	AP_GPA26	GPIOA26	IO	GPIOA26	DISHSYNC	-	-	GPIO
PAH2	AP_GPA0	GPIOA0	IO	GPIOA0	DISCLK	-	-	GPIO
PAJ1	AP_I2S0_LRCLK	I2SLRCLK0	IO	GPIOD12	I2SLRCLK0	AC97_SYNC	-	I2S0
PAJ2	AP_GPA27	GPIOA27	IO	GPIOA27	DISDE	-	-	GPIO

Table 32. GPIO Alternate Functions WEST PART

GPIO Alternate Functions WEST PART								
Ball Loc	Ball Name	Default Function	I/O	Function 0	Function 1	Function 2	Function 3	Group
PP41	AP_GPIOB30	GPIOB30	IO	SD14	GPIOB30	TSIDATA0_6	-	GPIO
PAG41	AP_GPB11	CLE0	IO	CLE0	CLE1	GPIOB11	-	GPIO
PAG42	AP_GPB18	GPIOB18	IO	NNFWE0	nNFWE1	GPIOB18	-	GPIO
PAH41	AP_GPC25	GPIOC25	IO	NSWAIT	GPIOC25	SPDIFTX	-	GPIO
PAH42	AP_GPE31	GPIOE31	IO	NSWE	GPIOE31	-	-	GPIO

BOOTING SEQUENCE

The ARTIK 530 Module supports a variety of booting scenarios as depicted in

Table 33. *Table 34* describes the values of the PAD signals needed to initiate the various booting scenarios. When nothing is done default booting will take place. (AP_GPB13_SD0_BOOT is High, AP_GPB15_SD1_BOOT is Low and AP_GPB4_VID1_3_BOOT is High) In this case the ARTIK 530 Module will try to boot from eMMC, if this fails it will continue to initiate a boot from SD0 and if this fails it will continue booting from the USB device. The other booting options perform in a similar manner. Changing the PAD signals according to the values in *Table 34* will allow for different booting options to be executed.

Table 33. Booting Scenarios

Booting Scenario	Primary Booting Device	Secondary Booting Device	Tertiary Booting Device
1	Boot from eMMC	Boot from SD0	Boot from USB device
2	Boot from SD0	Boot from USB device	–
3	Boot from USB device	–	–

Table 34. Booting Options

Signal Name	Booting Scenario 1 (default)	Booting Scenario 2	Booting Scenario 3
AP_GPB13_SD0_BOOT	High (Internal PU)	High*	Low*
AP_GPB15_SD1_BOOT	Low (Internal PD)	Low*	High*
AP_GPB4_VID1_3_BOOT	High (Internal PU)	Low*	X

*Additional external PU/PD resistors are needed.

POWER STATES

Figure 3 shows the Power Management state diagram. In this diagram the entry and WAKEUP conditions for each power down mode are given.

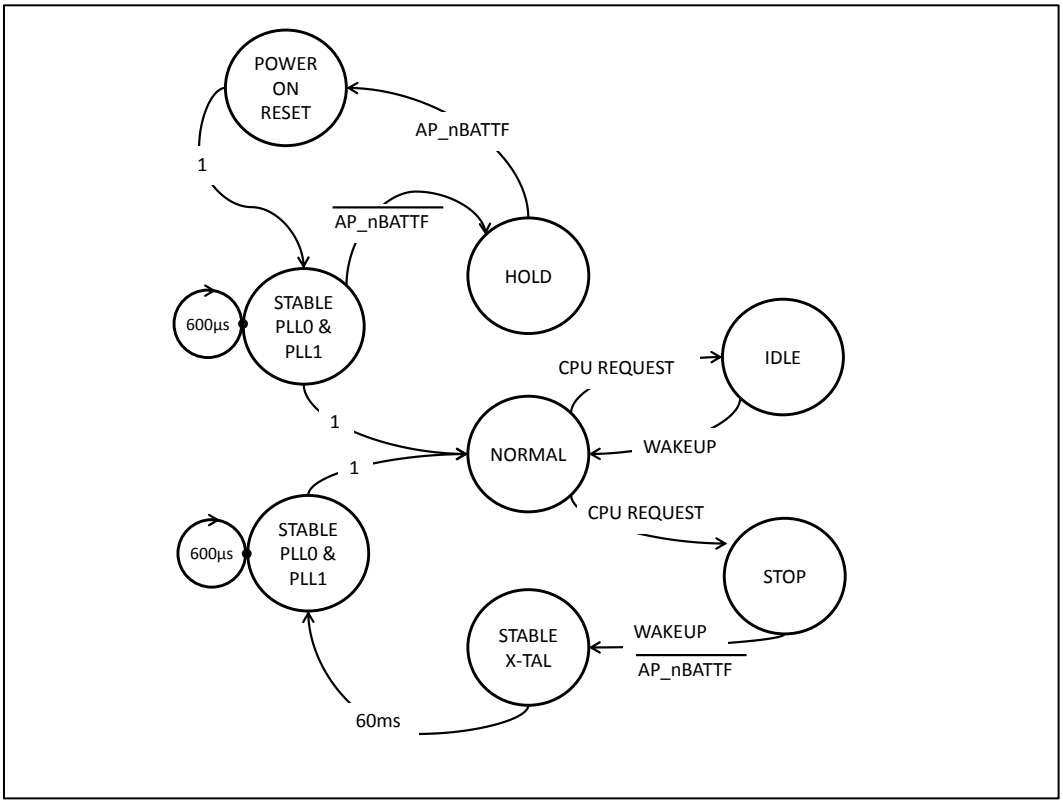


Figure 3. ARTIK 530 Module Power Management State Diagram

The following Modes of operation can be distinguished:

- NORMAL Mode
  - Everything is running, this is the normal mode of operation when applications are executed on the ARM cores
- IDLE Mode
  - CPU clocks are turned off
  - IDLE state can be initiated by CPU using Software API
  - The following WAKEUP sources can be used to return to NORMAL Mode:
    - GPIO Interrupt, RTC Interrupt, AliveGPIO Interrupt (see PAE2, PAF:[1,2]), External IRQ
- STOP Mode
  - PLL's are turned off, DRAM goes into self-refresh
  - STOP state can be initiated by CPU using Software API
  - Certain WAKEUP sources or the ARTIK 530 Module $\overline{\text{AP\_nBATTF}}$ signal can be used to transition to NORMAL Mode
  - The following WAKEUP sources can be used to return to NORMAL Mode:
    - RTC Interrupt, AliveGPIO Interrupt

For more information on how to access discussed WAKEUP mechanisms like AliveGPIO interrupts, GPIO Interrupts, RTC Interrupts and External Interrupts, please refer to the Software User Guide.

ANTENNA CONNECTIONS

Two antennas are required to use the full set of radio communication links on the ARTIK 530 Module. One supports the combination of 802.11/Bluetooth®, and the other is dedicated to 802.15.4.

Caution: Do not apply power (enable) the radio chips before connecting antennas or damage to the chip may result.

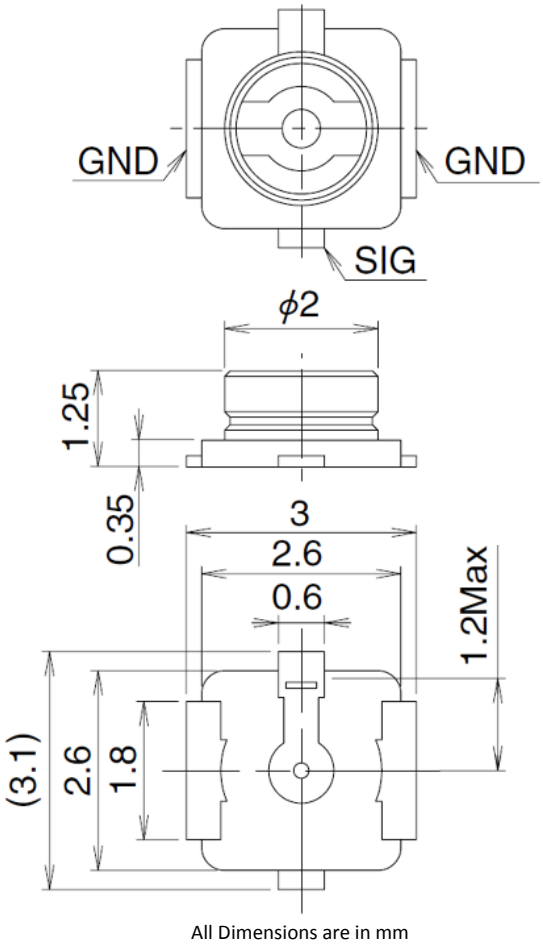


Figure 4. RF Connector for Bluetooth®/802.11 and 802.15.4 (ZigBee/Thread)

The U.FL-R-SMT Hirose connector is used for both the Bluetooth®/802.11 and the 802.15.4 (ZigBee/Thread) antenna connectors on the ARTIK 530 Module.

The mechanical size of the connector (receptacle) is described in *Figure 4*. For suggestions on mating plug and more details on the connector, please contact Hirose Electric Co., LTD.

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

The ratings given in this section are associated only with stress. It does not imply any functional operation of the device. Exposure to the absolute-maximum rated conditions for long duration affects the reliability of the device.

Table 35. Absolute Maximum Ratings

Absolute Maximum Ratings					
Parameter	**Symbol**	**Condition**	**Min**	**Max**	**Units**
Main power supply	VIN	–	-0.3	6.0	V
DC input/output voltage	PA:[1,2,3,5,6,7,8,29,37,39,40,41,42] PB:[2,3,4,5,6,7,8,39,40,41,42] PAK:[1,2,3,4,5,6,7,8,9,10,11,19,20,21,22,23,24,25,26,27,28,29,30,32,33,34,35,36,37,38,39,40,41,42] PAL:[1,2,3,4,5,6,7,8,9,10,11,20,21,22,23,24,25,26,27,28,29,30,31,32,33,34,35,36,37,38,39,40,41,42] PP:[41] PAC:[1,2] PAD:[1,2] PAE:[1] PAG:[2,41,42] PAH:[1,2,41,42] PAJ:[1,2]	3.3V Buffer	-0.5	3.8	
	PAK:[12,13,14] PAL:[12,13]	5V Tolerant buffer	-0.3	5.3	
	PAK:[15] PAL:[15]	Non 5V Tolerant Buffer	-0.3	3.6	
	PAL:[19] PAF:[1] PAG:[1]	–	-0.3	3.8	
	PAL:[14]	Voltage at Pin	-0.5	3.8	V
DC Input/output current	PA:[1,2,3,5,6,7,8,29,37,39,40,41,42] PB:[2,3,4,5,6,7,8,39,40,41,42] PAK:[1,2,3,4,5,6,7,8,9,10,11,19,20,21,22,23,24,25,26,27,28,29,30,32,33,34,35,36,37,38,39,40,41,42] PAL:[1,2,3,4,5,6,7,8,9,10,11,20,21,22,23,24,25,26,27,28,29,30,31,32,33,34,35,36,37,38,39,40,41,42] PP:[41] PAC:[1,2] PAD:[1,2] PAE:[1] PAG:[2,41,42] PAH:[1,2,41,42] PAJ:[1,2]	–	-20	20	mA
	PAK:[12,13,14,15] PAL:[12,13]	–	-50	50	mA
	PAL:[14]	Current at Pin	-1	1	mA
Storage Temperature	T_A	–	-40	85	°C

Recommended Operating Conditions

The recommended operation of the ARTIK 530 Module is based on the operating conditions listed in

Table 36.

Table 36. Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
Main power supply	VIN PV:[41,42],PW:[41,42],PY:[41,42],PAA:[41,42],PAB:[41,42]	3.7	4.20	5.0	V
Operating Temperature	T_C	-25	–	85	°C

DC Module Use Case Characteristics

Power Supply Requirements

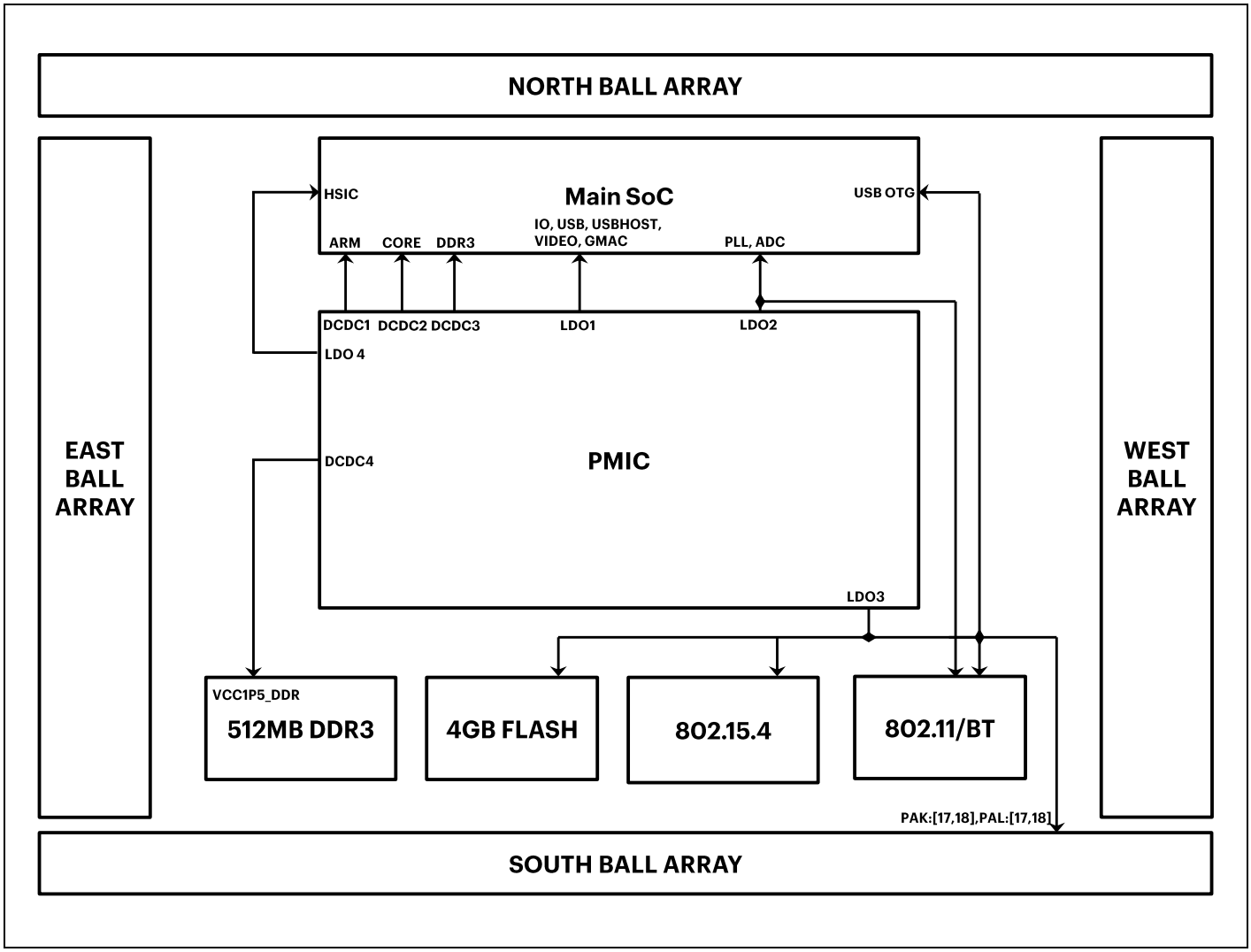


Figure 5. ARTIK 530 Module Power Distribution

The power management of the ARTIK 530 Module as described in *Figure 5* is controlled by a PMIC. This PMIC contains four high efficiency DC-DC converters and five LDO regulators. See *Table 37* and *Table 38* for details on voltage and amperage ranges and how they are used in the ARTIK 530 Module.

Table 37. DC-DC Converter Description

Buck	Powers	Header	Max Current [mA]	Range [V]	Default [V]
DCDC1	ARM of Main SoC	–	3000	0.60-3.50	1.0
DCDC2	Core of Main SoC	–	3000	0.60-3.50	1.0
DCDC3	DDR3 IO Memory	–	2000	0.60-3.50	1.50
DCDC4	DDR3 Core Memory	–	2000	0.60-3.50	1.50

Table 38. PMIC LDOs

LDO	Powers	Header	Current [mA]	Range [V]	Step [mV]	Default [V]
LDO1	Main SoC :[IO,USB,USBHOST,VIDEO,GMAC]	–	300	0.90-3.50	50	–
LDO2	802.11/Bluetooth®, Main SoC:[ADC,PLL]	–	300	0.90-3.50	50	–
LDO3	FLASH, 802.11/Bluetooth®, 802.15.4, Main SoC:[USB OTG]	PAK:[17,18],PAL:[17,18]	300	0.90-3.50	50	3.30
LDO4	Main SoC:[HSIC]	–	200	0.90-3.50	50	1.20
LDO5	Not Used	–	–	–	–	–

Table 39. AC/DC Characteristics LDO3

PAK:[17,18],PAL:[17,18] Operating Conditions V_{IN}=3.6V, C_{OUT}=1µF, T_A=25°C unless otherwise specified						
Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{IN}	Input Voltage Range	–	1.70	3.60	5.5	V
V_{OUT}	Output Voltage Range	50µA < I_{OUT} < I_{OUTMAX}	0.60	–	3.50	V
	Voltage Setting Step Width	–	–	50	–	mV
V_{ACCU}	Output Voltage Accuracy	V_{OUT} = All Output Range, I_{OUT}=1mA	-1.50	–	1.50	%
I_{OUTMAX}	Output Current	–	–	–	300	mA
I_{LIM}	Limit Current	–	350	–	–	mA
V_{DIFF}	Dropout Voltage	V_{OUT} Setting=V_{IN}, I_{OUT}=I_{OUTMAX}	–	–	0.30	V
V_{LINE}	Line Regulation	2.7 < V_{IN} <5.5V, I_{OUT}=1mA	–	–	0.20	%/V
V_{LOAD}	Load Regulation	100µA < I_{OUT} < I_{OUTMAX}	–	–	30	mV
V_{TR}	Transient Response	I_{OUT}=100µA <> I_{OUTMAX}/2	–	40	–	mV
RR	Ripple Rejection	F=217 ~ 1kHz, I_{OUT}=I_{OUTMAX}/2, V_{DIFF} > 0.6V	–	60	–	dB
O_{NOISE}	Output Noise	I_{OUT}=I_{OUTMAX}/2, BW=10Hz-100kHz, V_{OUT}=1.2V	–	60	–	uVrms
I_{SS}	Supply Current	I_{OUT}=0mA	–	20	–	µA
I_{OFF}	Standby Current	I_{OUT}=0mA	–	–	1	µA
T_R	Rising Time	V_{OUT}x0.9, I_{OUT}=0mA	–	–	500	µs
T_F	Falling Time	V_{OUT}x0.1, I_{OUT}=0mA	–	–	500	µs
C_{OUT}	Output Capacitor		–	1.0	–	µF

ESD RATINGS

Table 40. ESD Ratings

Symbol	Min.	Max.	Units
ESD stress voltage Human Body Model	–	1	kV
ESD stress voltage Charged Device Model	–	TBD	V

Table 41. Shock and Vibration Ratings

Shock and Vibration		Range
Shock	Operating	TBD
	Non Operating	TBD
Vibration	Operating	TBD
	Non Operating	TBD

DC Electrical Characteristics

The DC characteristics for the GPIO pins of the ARTIK 530 Module are listed in *Table 42*. Use the parameters from *Table 42* to determine maximum DC loading and to determine maximum transition times for a given load.

Table 42. I/O DC Electrical Characteristics GPIO

V_{DD} = 3.3V, V_{ext} = 3.0 to 3.6 V, T_J = -25 to 85 °C (T_J = Junction Temperature), 3.30V Tolerant

GPIO BALL Coordinates	Parameter		Condition		Min	Typ	Max	Units
PA:[1,2,3,5,6,7,8,29,37,39,40,41,42] PB:[2,3,4,5,6,7,8,39,40,41,42] PAK:[1,2,3,4,5,6,7,8,9,10,11,19,20,21,22,23,24,25,26,27,28,29,30,32,33,34,35,36,37,38,39,40,41,42] PAL:[1,2,3,4,5,6,7,8,9,10,11,20,21,22,23,24,25,26,27,28,29,30,31,32,33,34,35,36,37,38,39,40,41,42] PP:[41] PAC:[1,2] PAD:[1,2] PAE:[1] PAG:[2,41,42] PAH:[1,2,41,42] PAJ:[1,2]	V_{TOL}	Tolerant external voltage	V_{DD} Power Off & On		–	–	3.60	V
	V_{IH}	High Level Input Voltage						
		CMOS Interface	–		2.31	–	3.60	V
	V_{IL}	Low Level Input Voltage						
		CMOS Interface	V_{DD} = 3.3V ± 10 %		-0.3	–	0.70	V
	ΔV	Hysteresis Voltage	–		0.15	–		V
	I_{IH}	High Level Input Current						
		Input Buffer	V_{IN} = V_{DD}	V_{DD} Power On	-3	–	3	µA
				V_{DD} Power Off & SNS = 0	-5	–	5	
		Input Buffer with pull-down	V_{IN} = V_{DD}	V_{DD} = 3.3V ± 10 %	15	40	80	
	I_{IL}	Low Level Input Current						
		Input Buffer	V_{IN} = V_{SS}	V_{DD} Power On & Off	-3	–	3	µA
		Input Buffer with pull-up	V_{IN} = V_{SS}	V_{DD} = 3.3V ± 10 %	-15	-40	-110	
	V_{OH}	Output High Voltage	I_{OH} = -1.8mA, -3.6mA, -7.2mA, -10.8mA		2.64	–	3.30	V
	V_{OL}	Output Low Voltage	I_{OH} = -1.8mA, -3.6mA, -7.2mA, -10.8mA		0	–	0.66	
	I_{OZ}	Output Hi-Z current	–		-5	–	5	µA
	C_{IN}	Input capacitance	Any input and bi-directional buffers		–	–	5	pF
	C_{OUT}	Ouput capacitance	Any output buffer		–	–	5	pF

Table 43. I/O DC Electrical Characteristics 802.15.4

802.15.4 BALL Coordinates	Symbol	Description	Condition	Min	Typ	Max	Units
PAK:[12,13,14,15] PAL:[12,13,15]	V_{IL}	V_{IL} input logic level low V_{DD}=3.3V		–	–	0.70	V
	V_{IH}	V_{IH} input logic level high V_{DD}=3.3V		2.31	–	–	V
	Output Voltage Levels						
	$V_{OL[3mA]}$	V_{OL} output logic level low V_{DD}=3.3V, I_{OL}=3ma, weak driver		–	–	0.66	V
	$V_{OH[-3mA]}$	V_{OH} output logic level high V_{DD}=3.3V, I_{OH}=-3ma, weak driver		2.64	–	–	V
	$V_{OH[20mA]}$	V_{OH} output logic level high V_{DD}=3.3V, I_{OL}=20ma, strong driver		–	–	0.66	V
	$V_{OH[-20mA]}$	V_{OH} output logic level high V_{DD}=3.3V, I_{OL}=-20ma, strong driver		2.64	–	–	V
PAL:[14]	I_Q	Quiescent Current	Static Inputs and Outputs	–	1.00	–	µA
	V_O	Maximal voltage applied to PIN in High-Impedance State	–	–	–	3.30	V
	V_{IH}	High Level Input Voltage	Logic input at V_{DD}=3.3V	1.84	–	3.30	
	V_{IL}	Low Level Input Voltage	Logic input at V_{DD}=3.3V	–	–	1.255	
	I_{IH}	High Level Input Current	Logic input V_{IN}=V_{DD}=3.3V	-1.00	–	1.00	µA
	I_{IL}	Low Level Input Current	Logic input V_{IN}=0V	-1.00	–	1.00	
	V_{OH}	High Level Output Voltage	Push-Pull & PMOS OD, I_{OL}=3mA, 1x Driver at V_{DD}=3.3V	2.721	3.108	–	V
	V_{OL}	Low Level Output Voltage	Push-Pull, IOL=3mA, 1x Driver at VDD=3.3V		0.175	0.257	

802.15.4 BALL Coordinates	Symbol	Description	Condition	Min	Typ	Max	Units
	I_{OH}	High Level Output Current	Push-Pull & PMOS OD, V_{OH}=2.4V, 1x Driver at V_{DD}=3.3V	5.774	11.066	–	mA
	I_{OL}	Low Level Output Current	Push-Pull, V_{OL}=0.4V, 1x Driver at V_{DD}=3.3V	4.491	6.438	–	

Table 44. I/O DC Electrical Characteristics PMIC

PMIC BALL Coordinates	Parameter	Symbol	Test Condition	Min	Typ	Max	Units
PAG:[1]	Open drain, I_{OUT}=2mA	V_{OL}	–	–	–	0.40	V
	Open drain, I_{OUT}=2mA	V_{OH}		–	–	VIN	V
PAF:[1],PAL:[19]	Input only : Low level input voltage	V_{IL}	–	–	–	0.40	V
	Input only : High level input voltage	V_{IH}		1.40	–	VIN	V

Table 45. I/O DC Electrical Characteristics GPIO

802.11/Bluetooth® BALL Coordinates	Parameter	Symbol	Condition	Min	Typ	Max	Unit
PAJ:[39,40,41,42]	High level input voltage	V_{IH}	–	2.31	–	3.70	V
	Low level input voltage	V_{IL}	–	-0.40	–	0.99	
	Output High voltage	V_{OH}	–	2.90	–	–	V
	Output Low voltage	V_{OL}	–	–	–	0.40	

Table 46. GPIO Pull-up Resistor Current

BALL Coordinates	Condition	Pull Up	Min	Typ	Max	Unit
PA:[1,2,3,5,6,7,8,29,37,39,40,41,42] PB:[2,3,4,5,6,7,8,39,40,41,42] PAK:[1,2,3,4,5,6,7,8,9,10,11,19,20,21,22,23,24,25,26,27,28,29,30,32,33,34,35,36,37,38,39,40,41,42] PAL:[1,2,3,4,5,6,7,8,9,10,11,20,21,22,23,24,25,26,27,28,29,30,31,32,33,34,35,36,37,38,39,40,41,42] PP:[41] PAC:[1,2] PAD:[1,2] PAE:[1] PAG:[2,41,42] PAH:[1,2,41,42] PAJ:[1,2]	Every GPIO has a 100kΩ internal pull-up resistor	Enable	10	33	72	µA
		Disable	–	–	0.1	µA

*Based on 100kΩ internal pull-up resistor

Table 47. Power on Reset Timing Specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_{RESW}	Reset assert time after clock stabilization	TBD	–	–	ns

AC Electrical Characteristics

AC characteristics covered in this section are preliminary and are likely to change.

SD/MMC AC Electrical Characteristics

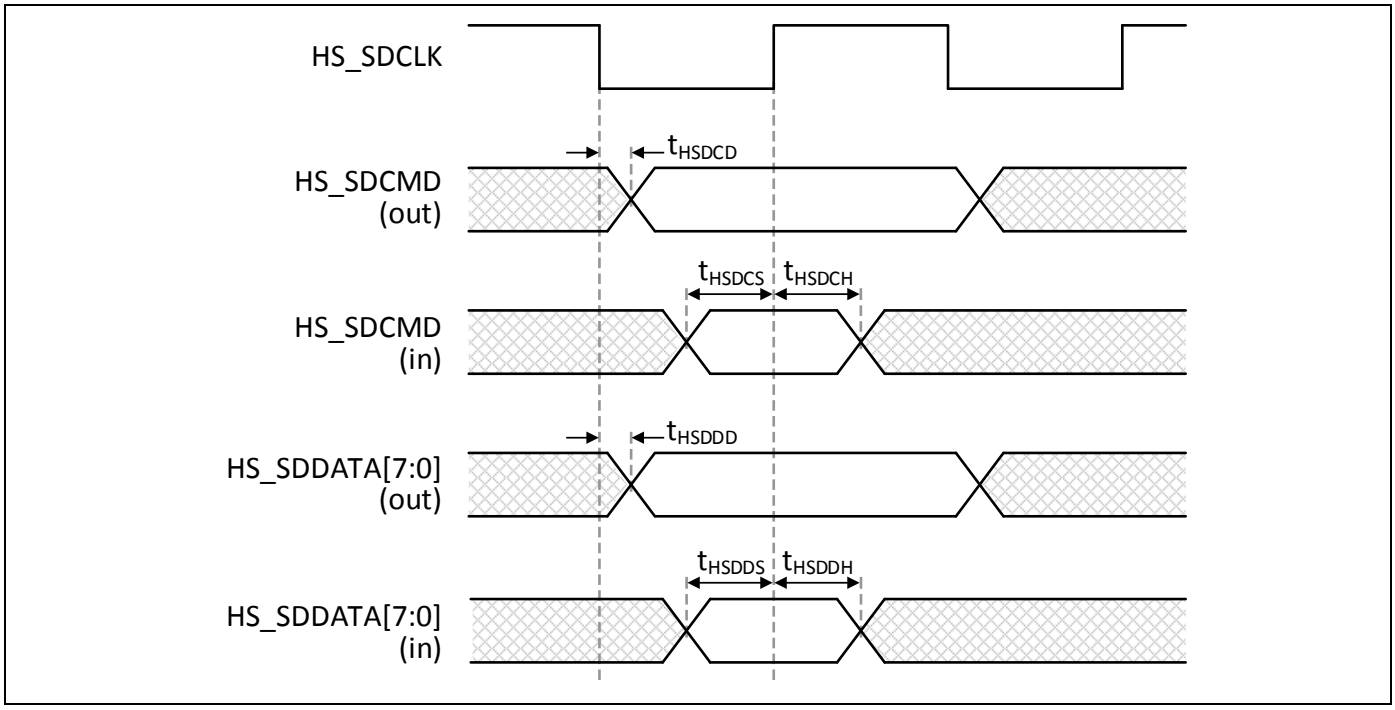


Figure 6. High Speed SD/MMC Interface Timing

Table 48. High Speed SD/MMC Interface Transmit/Receive Timing Constants

(V_{DDINT} = 1.0V ± 5%, T_J = -25 to 85°C, V_{DDmmc} = 3.3V ± 5 %, 2.5V ± 5%, 1.8V ± 5%)

BOT:[59,60,61,62,63,64]					
Symbol	**Parameter**	**Min**	**Typ**	**Max**	**Unit**
t_{SDCD}	SD command output delay time	–	–	4.0	ns
t_{SDCS}	SD command input setup time	4.0	–	–	
t_{SDCH}	SD command input hold time	0	–	–	
t_{SDDD}	SD data output delay time	–	–	4.0	
t_{SDDS}	SD data input setup time	4.0	–	–	
t_{SDDH}	SD data input hold time	0	–	–	

SPI AC Electrical Characteristics

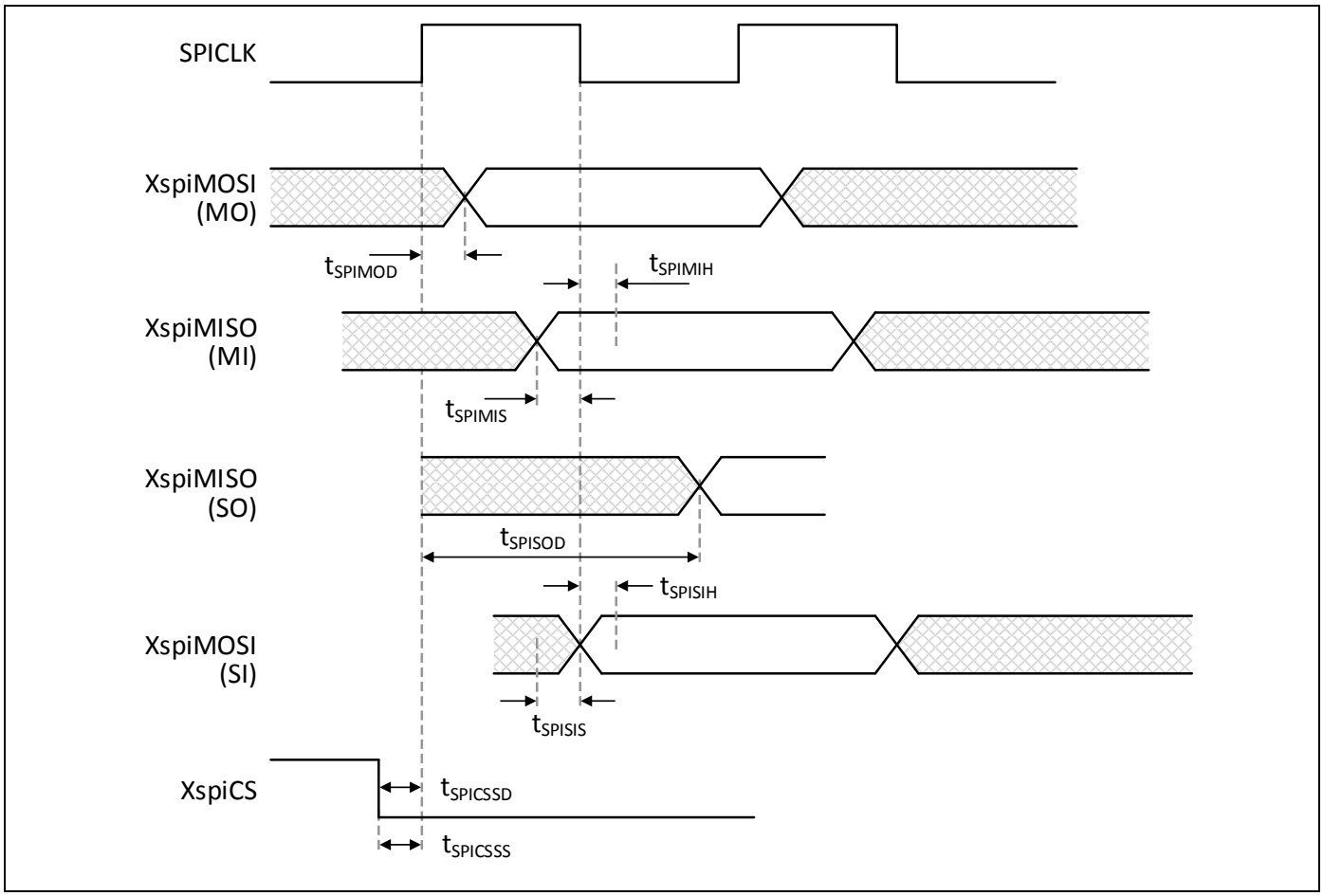


Figure 7. SPI Interface Timing (CPHA = 0, CPOL = 1 (Format A))

Table 49. SPI Interface Transmit/ Receive Timing Constants with 15pF Load

(V_{DDINT} = 1.0 V ± 5 %, T_J = -25 to 85 °C, V_{DDext} = 1.8 V ± 10 %, load = 15 pF)

Parameter		Symbol	Min.	Typ.	Max.	Unit
Ch 0	SPI MOSI Master Output Delay time	t_{SPIMOD}	–	–	5	ns
	SPI MISO Master Input Setup time (FB_CLK_SEL = 00)	t_{SPIMIS}	12	–	–	
	SPI MISO Master Input Setup time (FB_CLK_SEL = 01)		7	–	–	
	SPI MISO Master Input Setup time (FB_CLK_SEL = 10)		2	–	–	
	SPI MISO Master Input Setup time (FB_CLK_SEL = 11)		-3	–	–	
	SPI MISO Master Input Hold time	t_{SPIMIH}	5	–	–	
	SPI MOSI Slave Input Setup time	t_{SPISIS}	2	–	–	ns
	SPI MOSI Slave Input Hold time	t_{SPISIH}	5	–	–	
	SPI MISO Slave Output Delay time	t_{SPISOD}	–	–	17	
	SPI nSS Master Output Delay time	$t_{SPICSSD}$	7	–	–	
	SPI nSS Slave Input Setup time	$t_{SPICSSS}$	5	–	–	
Ch 1	SPI MOSI Master Output Delay time	t_{SPIMOD}	–	–	4	ns
	SPI MISO Master Input Setup time (FB_CLK_SEL = 00)	t_{SPIMIS}	13	–	–	
	SPI MISO Master Input Setup time (FB_CLK_SEL = 01)		8	–	–	
	SPI MISO Master Input Setup time (FB_CLK_SEL = 10)		3	–	–	
	SPI MISO Master Input Setup time (FB_CLK_SEL = 11)		-2	–	–	
	SPI MISO Master Input Hold time	t_{SPIMIH}	5	–	–	
	SPI MOSI Slave Input Setup time	t_{SPISIS}	3	–	–	
	SPI MOSI Slave Input Hold time	t_{SPISIH}	5	–	–	ns
	SPI MISO Slave Output Delay time	t_{SPISOD}	–	–	18	
	SPI nSS Master Output Delay time	$t_{SPICSSD}$	7	–	–	
	SPI nSS Slave Input Setup time	$t_{SPICSSS}$	5	–	–	

Note: SPICLKout = 50 MHz

- t_{SPIMIS},CH0 = 12 – (cycle period/4) x FB_CLK_SEL
- t_{SPIMIS},CH1 = 13 – (cycle period/4) x FB_CLK_SEL

Table 50. SPI Interface Transmit/ Receive Timing Constants with 30pF Load

(VDDINT = 1.0 V ± 5 %, T_J = –25 to 85°C, VDDext = 3.3 V ± 10 %, load = 30 pF)

Parameter		Symbol	Min.	Typ.	Max.	Unit
Ch 0	SPI MOSI Master Output Delay time	t_{SPIMOD}	–	–	6	ns
	SPI MISO Master Input Setup time (FB_CLK_SEL = 00)	t_{SPIMIS}	13	–	–	
	SPI MISO Master Input Setup time (FB_CLK_SEL = 01)		8	–	–	
	SPI MISO Master Input Setup time (FB_CLK_SEL = 10)		3	–	–	
	SPI MISO Master Input Setup time (FB_CLK_SEL = 11)		-2	–	–	
	SPI MISO Master Input Hold time	t_{SPIMIH}	5	–	–	
	SPI MOSI Slave Input Setup time	t_{SPISIS}	4	–	–	ns
	SPI MOSI Slave Input Hold time	t_{SPISIH}	5	–	–	
	SPI MISO Slave Output Delay time	t_{SPISOD}	–	–	18	
	SPI nSS Master Output Delay time	$t_{SPICSSD}$	8	–	–	
	SPI nSS Slave Input Setup time	$t_{SPICSSS}$	6	–	–	
Ch 1	SPI MOSI Master Output Delay time	t_{SPIMOD}	–	–	5	ns
	SPI MISO Master Input Setup time (FB_CLK_SEL = 00)	t_{SPIMIS}	14	–	–	
	SPI MISO Master Input Setup time (FB_CLK_SEL = 01)		9	–	–	
	SPI MISO Master Input Setup time (FB_CLK_SEL = 10)		4	–	–	
	SPI MISO Master Input Setup time (FB_CLK_SEL = 11)		-1	–	–	
	SPI MISO Master Input Hold time	t_{SPIMIH}	5	–	–	
	SPI MOSI Slave Input Setup time	t_{SPISIS}	4	–	–	
	SPI MOSI Slave Input Hold time	t_{SPISIH}	5	–	–	ns
	SPI MISO Slave Output Delay time	t_{SPISOD}	–	–	19	
	SPI nSS Master Output Delay time	$t_{SPICSSD}$	8	–	–	
	SPI nSS Slave Input Setup time	$t_{SPICSSS}$	6	–	–	

Note: SPICLKout = 50 MHz

- tSPIMIS,CH0 = 12 – (cycle period/4) x FB_CLK_SEL
- tSPIMIS,CH1 = 13 – (cycle period/4) x FB_CLK_SEL

I²C AC Electrical Characteristics

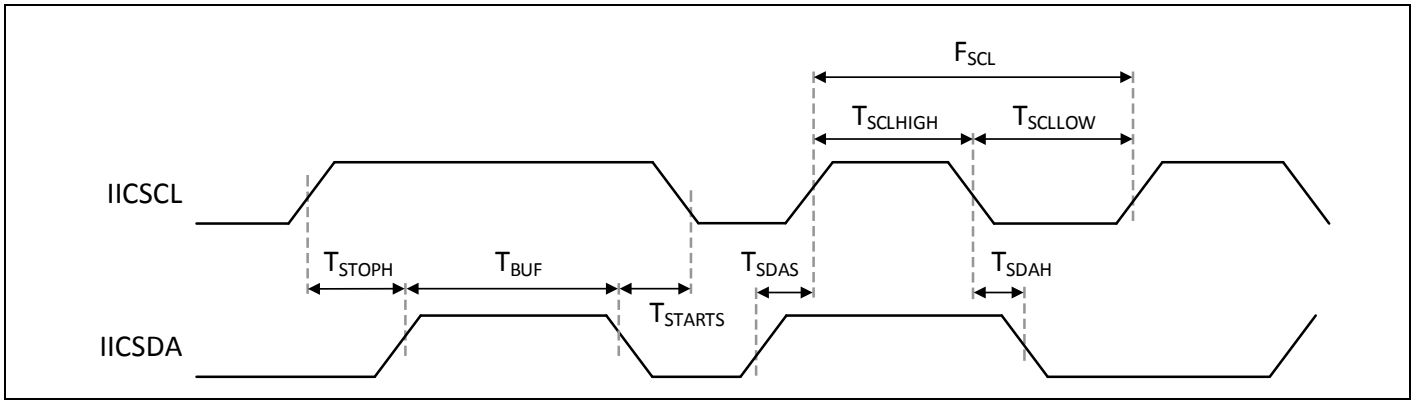


Figure 8. I²C Interface Timing

Table 51. I²C BUS Controller Module Signal Timing

(VDDINT, VDDarm = 1.1 V ± 5 %, T_J = -25 to 85°C, VDDext = 3.3 V ± 10 %)

Parameter	Symbol	Min.	Typ.	Max.	Unit
SCL clock frequency	F_{SCL}	–	–	std. 100 fast 400	kHz
SCL high level pulse width	$T_{SCLHIGH}$	std. 4.0 fast 0.6	–	–	µs
SCL low level pulse width	T_{SCLLOW}	std. 4.7 fast 1.3	–	–	
Bus free time between STOP and START	T_{BUF}	std 4.7 fast 1.3	–	–	
START hold time	T_{STARTS}	std. 4.0 fast 0.6	–	–	
SDA hold time	T_{SDAH}	std. 0 fast 0	–	std. fast 0.9	
SDA setup time	T_{SDAS}	std. 250 fast 100	–	–	ns
STOP setup time	T_{STOPH}	std. 4.0 fast 0.6	–	–	µs

Note: std. refers to Standard Mode and fast refers to Fast Mode.

1. The I²C data hold time (t_{SDAH}) is minimum 0ns.
   (I²C data hold time is minimum 0ns for standard/fast bus mode I²C specification v2.1)
   Check whether the data hold time of your I²C device is 0 ns or not.
2. The I²C controller supports I²C bus device only (standard/fast bus mode), and does not support C bus device.

RF Electrical Characteristics

All performance numbers related to 802.11/Bluetooth® and 802.15.4 mentioned in this section are preliminary and likely to change once module characterization has taken place.

802.11, 2.4GHz Receiver RF Specifications

Table 52. 802.11, 2.4GHz Receiver RF Specifications

Parameter	Conditions	Min	Typ.	Max	Unit
Frequency Range	–	2400	–	2500	MHz
Minimum receiver sensitivity in 802.11b mode (2.4GHz)					
1Mbps	PER < 8%, Packet size = 1024 bytes	–	-97	–	dBm
2Mbps		–	-95	–	dBm
5.5Mbps		–	-94	–	dBm
11Mbps		–	-90	–	dBm
Minimum receiver sensitivity in 802.11g mode (2.4GHz)					
6Mbps	PER < 10%, Packet size= 1024 bytes	–	-91	–	dBm
9Mbps		–	-90	–	dBm
12Mbps		–	-89	–	dBm
18Mbps		–	-87	–	dBm
24Mbps		–	-84	–	dBm
36Mbps		–	-81	–	dBm
48Mbps		–	-76	–	dBm
54Mbps		–	-75	–	dBm
Minimum receiver sensitivity in 802.11n mode (2.4GHz)					
MCS 0	PER<10%, Packet size= 4096 bytes, GF, 800ns GI, Non-STBC	–	-89	–	dBm
MCS 1		–	-88	–	dBm
MCS 2		–	-86	–	dBm
MCS 3		–	-83	–	dBm
MCS 4		–	-79	–	dBm
MCS 5		–	-75	–	dBm
MCS 6		–	-73	–	dBm
MCS 7		–	-72	–	dBm

802.11, 2.4GHz Transmitter RF Specifications

Table 53. 802.11, 2.4GHz Transmitter RF Specifications

Parameter	Conditions	Min	Typ.	Max	Unit
Linear output power					
Maximum output power in 802.11b mode	As specified in IEEE802.11	–	15	–	dBm
Maximum output power in 802.11g mode		–	15	–	dBm
Maximum output power in 802.11n mode		–	13	–	dBm
Transmit spectrum mask					
Margin to 802.11b spectrum mask	Maximum output power	0	–	–	dBr
Margin to 802.11g spectrum mask		0	–	–	dBr
Margin to 802.11n spectrum mask		0	–	–	dBr
Transmit modulation accuracy in 802.11b mode					
1Mbps	As specified in IEEE 802.11b	–	–	35	%
2Mbps		–	–	35	%
5.5Mbps		–	–	35	%
11Mbps		–	–	35	%
Transmit modulation accuracy in 802.11g mode					
6Mbps	As specified in IEEE 802.11g	–	–	-5	dB
9Mbps		–	–	-8	dB
12Mbps		–	–	-10	dB
18Mbps		–	–	-13	dB
24Mbps		–	–	-16	dB
36Mbps		–	–	-19	dB
48Mbps		–	–	-22	dB
54Mbps		–	–	-25	dB
Transmit modulation accuracy in 802.11n mode					
MCS7	As specified in IEEE 802.11n	–	–	-27	dB
Transmit power-on and power-down ramp time in 802.11b mode					
Transmit power-on ramp time from 10% to 90% output power	–	–	–	2	µs
Transmit power-down ramp time from 90% to 10% output power	–	–	–	2	µs

802.11, 5GHz RF Specifications

Table 54. 802.11, 5GHZ Receiver RF Specifications

Parameter	Conditions	Min	Typ.	Max	Unit
Frequency Range	–	4900	–	5845	MHz
Minimum receiver sensitivity in 802.11a mode					
6Mbps	PER < 10%	–	-90	–	dBm
9Mbps		–	-89	–	dBm
12Mbps		–	-88	–	dBm
18Mbps		–	-87	–	dBm
24Mbps		–	-84	–	dBm
36Mbps		–	-80	–	dBm
48Mbps		–	-76	–	dBm
54Mbps		–	-75	–	dBm
Minimum receiver sensitivity in 802.11n (HT-20) mode					
MCS 0	PER < 10%	–	-89	–	dBm
MCS 1		–	-88	–	dBm
MCS 2		–	-85	–	dBm
MCS 3		–	-82	–	dBm
MCS 4		–	-79	–	dBm
MCS 5		–	-75	–	dBm
MCS 6		–	-72	–	dBm
MCS 7		–	-71	–	dBm
Minimum receiver sensitivity in 802.11n (HT-40) mode					
MCS 0	PER < 10%	–	-86	–	dBm
MCS 1		–	-85	–	dBm
MCS 2		–	-83	–	dBm
MCS 3		–	-80	–	dBm
MCS 4		–	-77	–	dBm
MCS 5		–	-73	–	dBm
MCS 6		–	-71	–	dBm
MCS 7		–	-69	–	dBm

Table 55. 802.11, 5GHz Transmitter RF Specifications

Parameter	Conditions	Min	Typ.	Max	Unit
Frequency Range	–	4900		5845	MHz
Linear output power					
Maximum output power in 802.11a mode	54M, UNII-2e	–	13	–	dBm
Maximum output power in 802.11n mode	HT20, MCS7, UNII-2e	–	12	–	dBm
	HT40, MCS7, UNII-2e	–	11	–	dBm
Transmit spectrum mask					
Margin to 802.11a spectrum mask	Maximum output power	0	–	–	dBr
Margin to 802.11n spectrum mask		0	–	–	dBr
Transmit constellation error in 802.11a mode					
54Mbps	As specified in IEEE 802.11n	–	–	-25	dB
Transmit constellation error in 802.11n (HT-20, HT-40) mode					
MCS 7	As specified in IEEE 802.11n	–	–	-27	dB

BLUETOOTH® RF SPECIFICATIONS

Table 56. Bluetooth® RF Specifications

Parameter	Conditions	Min	Typ	Max	Unit
Frequency Range	–	2402	–	2480	MHz
Sensitivity (BER)	GPSK, BER ≤0.1%	–	–92	–	dBm
	π/4-DQPSK, BER ≤ 0.1%	–	–92	–	dBm
	BER ≤ 0.1%, 8DPSK	–	–89	–	dBm
Maximum Input Level	GPSK, BER ≤0.1%	-20	–	–	dBm
	π/4-DQPSK, BER ≤ 0.1%	-20	–	–	dBm
	BER ≤ 0.1%, 8 DPSK	-20	–	–	dBm
BDR					
Intermodulation Performance	–	–	–	0.1	%
Rx C/I Performance	1DH1	–	–	0.1	%
	1DH3	–	–	0.1	%
	1DH5	–	–	0.1	%
EDR					
Rx C/I Performance	2DH1	–	–	0.1	%
	2DH3	–	–	0.1	%
	2DH5	–	–	0.1	%
	3DH1	–	–	0.1	%
	3DH3	–	–	0.1	%
	3DH5	–	–	0.1	%
Rx BER Floor Performance	BER ≤ 0.001%	–	–	-70	dBm

Table 57. Bluetooth® Transmitter RF Specifications

Parameter	Conditions	Min	Typ	Max	Unit
Frequency Range	–	2402	–	2480	MHz
Output Power (Average)					
BDR (QPSK)	2440 MHz	–	6	–	dBm
EDR (π/4-DQPSK)	2440 MHz	–	2	–	dBm
EDR (8DPSK)	2440 MHz	–	2	–	dBm

Table 58. BLE RF Specifications

Parameter	Conditions	Min	Typ	Max	Unit
Frequency Range	–	2402	–	2480	MHz
Rx Receiver Sensitivity PER	At -70dBm	–	–	30.8	%
Rx C/I and Receiver Selectivity Performance PER	–	–	–	30.8	%
Tx Power	–	–	6	–	dBm

802.15.4 RF Specifications

The Typical numbers indicated in *Table 59* and *Table 60* are one standard deviation below the mean, measured at room temperature 25°C. The Min and Max numbers were measured over process corners at room temperature.

Table 59. 802.15.4 RF Receive Specifications

Parameter	Test Condition	Min	Typ	Max	Unit
Operating Frequency Range	–	2400	–	2483.5	MHz
Receiver Sensitivity PER	At -95dBm	–	–	1	%
Receiver Sensitivity Search	At PER 1%	–	–95		dBm
Receiver Interference Rejection PER	At -2 Channel, Alternate Channel, 30dB	–	–	1	%
Receiver Interference Rejection PER	At -1 Channel, Adjacent Channel, 0dB	–	–	1	%
Receiver Interference Rejection PER	At +1 Channel, Adjacent Channel, 0dB	–	–	1	%
Receiver Interference Rejection PER	At +2 Channel, Alternate Channel, 30dB	–	–	1	%
Error Vector Magnitude - RMS (EVM)	At Target Power	–	–	30	%
Error Vector Magnitude - Offset (EVM)	At Target Power	–	–	10	%
Receiver Maximum Input Level of Desired Signal	At -20dBm Input	–	–	1	%

Table 60. 802.15.4 RF Transmit Specifications

Parameter	Test Condition	Min	Typ	Max	Unit
Maximum output power	At highest normal mode power setting		6/16*	–	dBm
Minimum output power	At lowest power setting	–	-27	–	dBm
Error vector magnitude (Offset-EVM)	As defined by IEEE 802.15.4-2003, which sets a 35% maximum	–	–	10	%
Carrier frequency error	–	-40	–	+40	ppm
PSD mask relative	3.5 MHz away (Normal)	-20	–	–	dBm
PSD mask absolute	100 KHz BW	-30	–	–	dBm

*The ARTIK 530 Module default setting is 6dBm for CE. You can change the setting to 16dBm for FCC testing.

MECHANICAL SPECIFICATIONS

The ARTIK 530 Module supports PAD Balls and two RF connectors on a 49mm x 36mm footprint as shown in *Figure 9*. Refer to section *Antenna Connections* for RF connector details. In addition the top view, side view and bottom view with its dimensions can be seen in *Figure 10* and *Figure 11*.

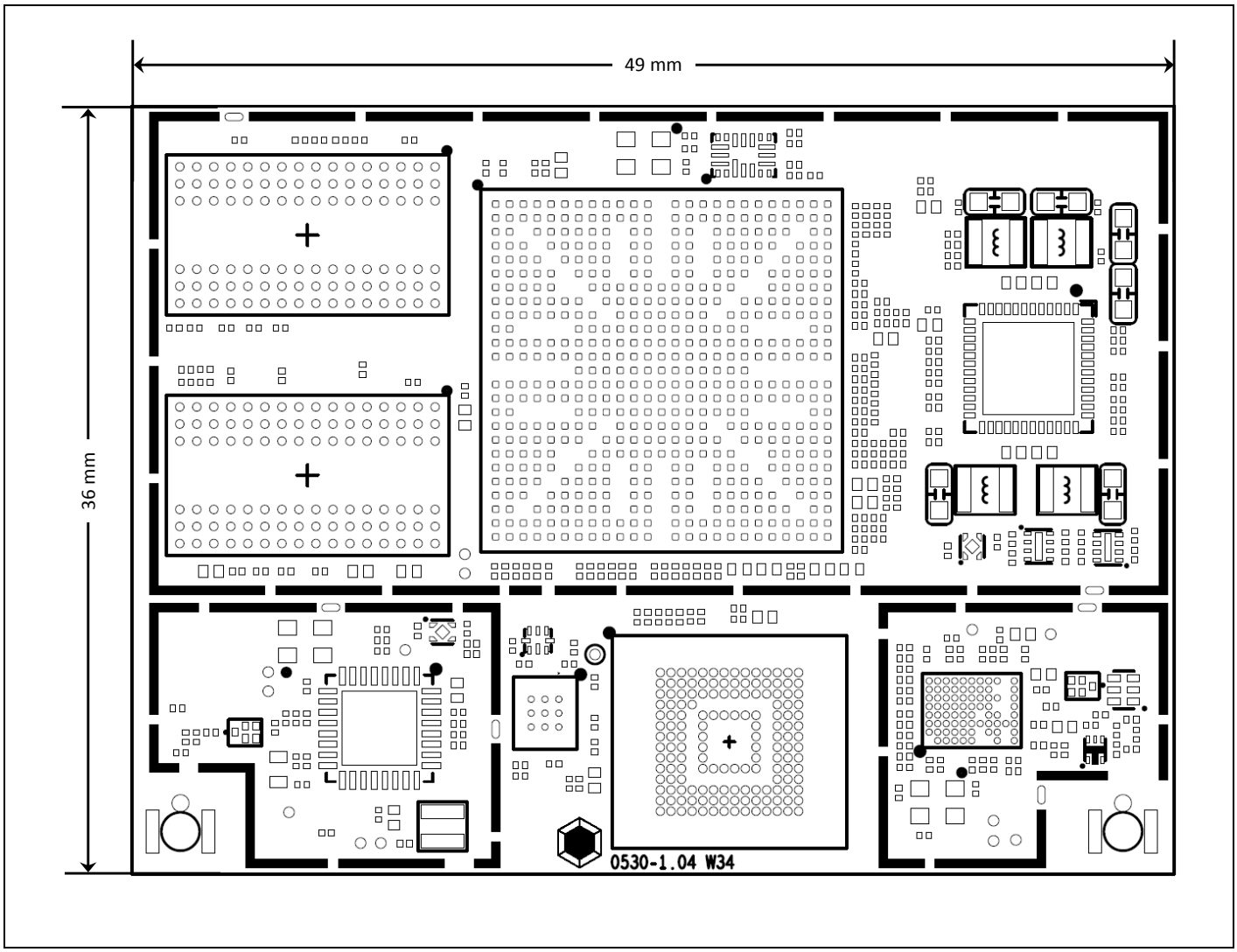


Figure 9. ARTIK 530 Module Top View Mechanical Dimensions and Part Location

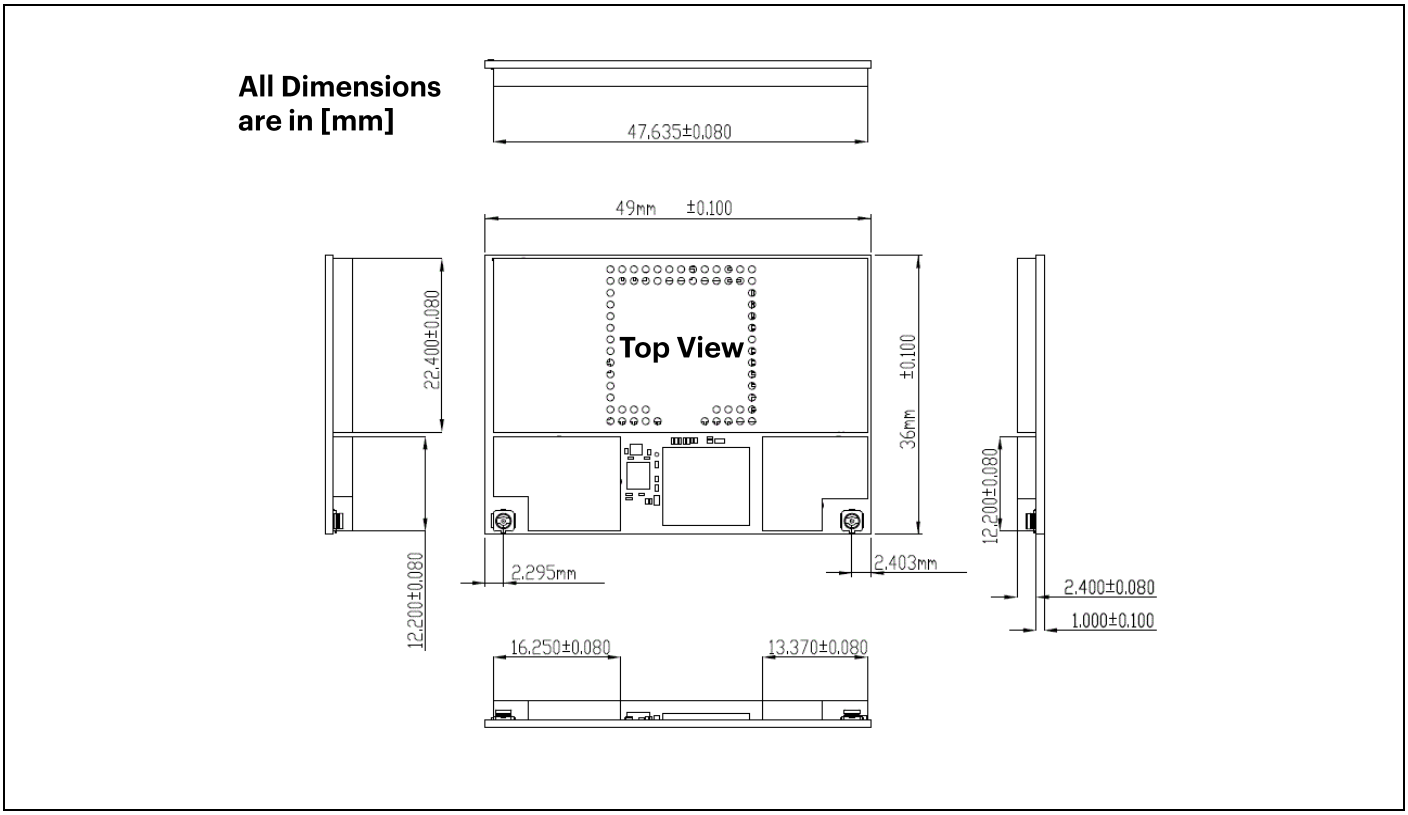


Figure 10. ARTIK 530 Module Mechanical Dimensions Top View

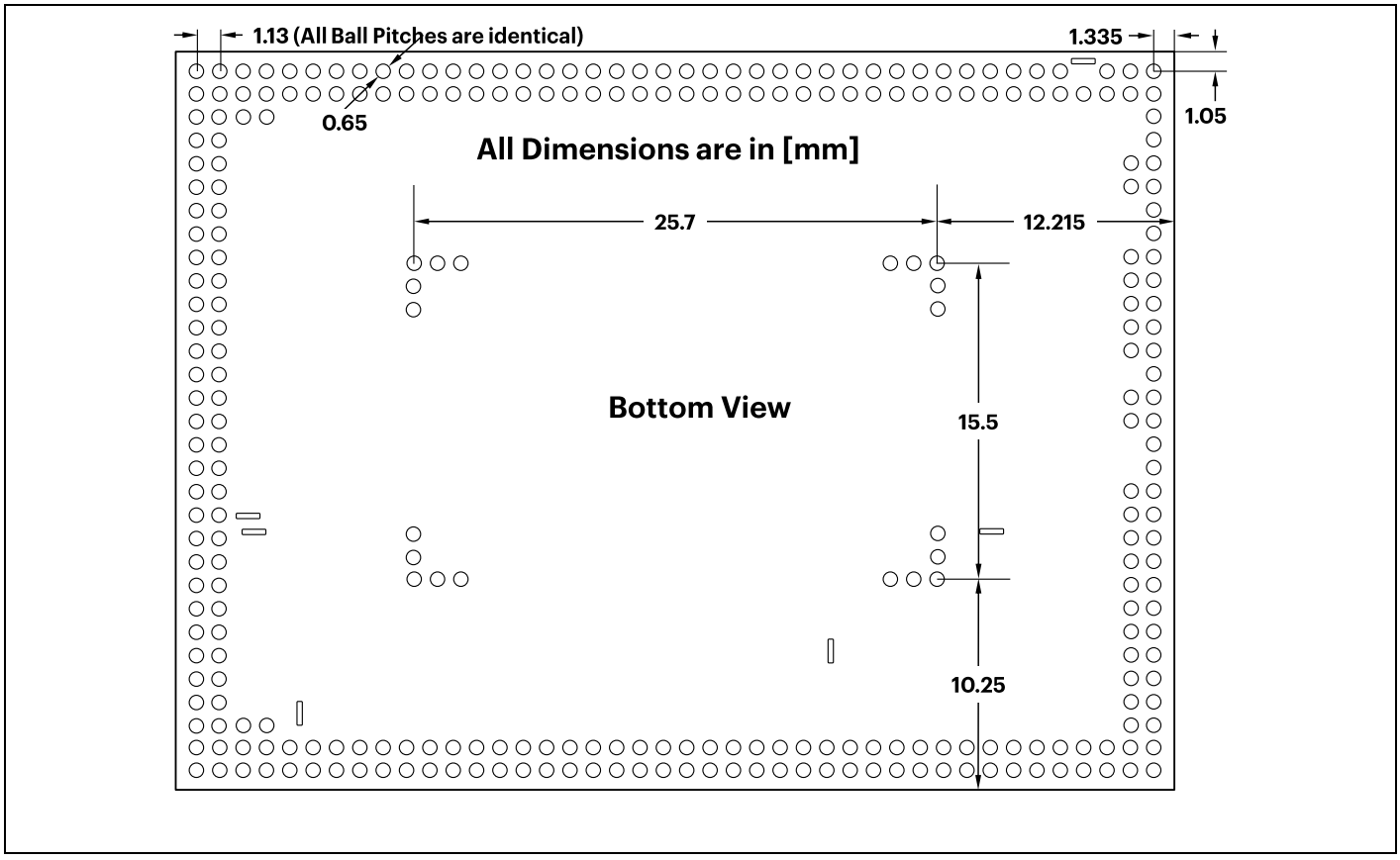


Figure 11 ARTIK 530 Module Mechanical Dimensions Bottom View

The inner pin locations on the PAD, positioned in an L-shaped form, as depicted in *Figure 12*, are located in *Table 61*. The inner PAD's are on a different grid from the outer PAD's as indicated with the dashed blue lines in *Figure 12*. For exact dimensions on location see *Figure 11*. The locations given in *Table 61* are the absolute coordinates measured from the edge of the ARTIK 530 Module to the center of each ball.

Table 61. L-Shaped Ball Locations

Ball Name	Ball Number	Netlist Name	X-Location Center Ball → [mm]	Y-Location Center Ball ↑ [mm]
TP	296	GND	12.215	10.25
TP	297	GND	12.215	11.38
TP	294	GND	12.215	12.51
TP	300	GND	12.215	23.49
TP	292	GND	12.215	24.62
TP	288	GND	12.215	25.75
TP	298	GND	13.345	10.25
TP	295	GND	13.345	25.75
TP	291	GND	14.475	10.25
TP	293	GND	14.475	25.75
TP	290	GND	35.655	10.25
TP	286	GND	35.655	25.75
TP	289	GND	36.785	10.25
TP	283	GND	36.785	25.75
TP	299	GND	37.915	10.25
TP	287	GND	37.915	11.38
TP	301	GND	37.915	12.51
TP	285	GND	37.915	23.49
TP	282	GND	37.915	24.62
TP	284	GND	37.915	25.75

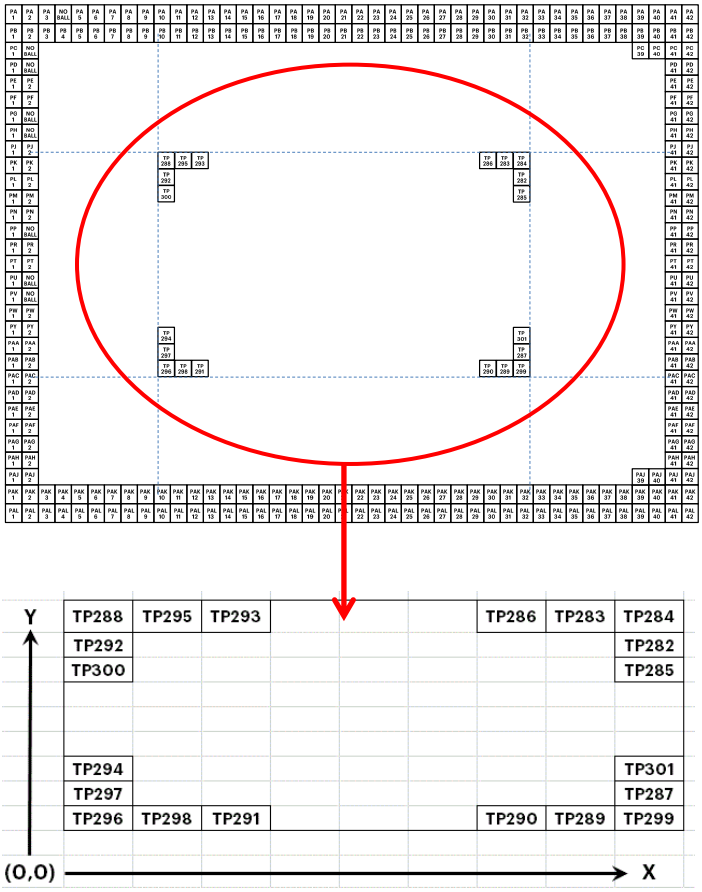


Figure 12. L-Shaped PAD Pins

CERTIFICATIONS AND COMPLIANCE

BLUETOOTH®

The ARTIK 530 Module is recognized as a qualified design as set out by Bluetooth® SIG.

Declaration ID: D032725

Qualified Design ID: 88390

CE

The ARTIK 530 Module is in compliance with each applicable article of the R&TTE directive. Compliance with the following standards was confirmed:

- LVD: EN60950-1 (2006+A11, 2009+A1, 2010+A12, 2011+A2, 2013)
- EMF: EN62311:2008
- EMC: 301 489-1 V1.9.2, EN 301 489-17 V2.2.1, EN 55032:2012/AC:2013, EN 55024:2010, EN 61000-3-2:2014, EN 61000-3-3:2013
- Radio spectrum use: EN 300 328 V1.9.1, EN301 893 V1.8.1, EN 300 440-2 V1.4.1

Notified body number: 0984

Notified body opinion number: AN16C10894-1

For a formal notified body statement of opinion contact your sales representative.

IC

The ARTIK 530 Module complies with the IC license–exempt RSS standard.

Radio certification number: 649E-SIP005AFS30

FCC

The ARTIK 530 Module complies with the following 2 sections (15C and 15E) of Part 15 of the FCC rules namely:

- Spread spectrum transmitter (SST) compliancy (15C) in the:
  - 2402-2480MHz frequency range, output power 0.0049W
- Digital transmission system (DTS) compliancy (15C) in the:
  - 2402-2480MHz frequency range, output power 0.004W
  - 2405-2475MHz frequency range, output power 0.0412W
  - 2412-2462MHz frequency range, output power 0.0308W
- Unlicensed national information infrastructure TX compliancy (15E) in the:
  - 5180-5240MHz frequency range, output power 0.0206W
  - 5260-5320MHz frequency range, output power 0.0221W
  - 5500-5720MHz frequency range, output power 0.0222W
  - 5745-5825MHz frequency range, output power 0.01W

FCC Identifier: A3LSIP005AFS30

Modular Type: Limited Single Modular

KCC

The ARTIK 530 Module complies with the standards set by the Korean communications commission (KCC).

KCC Identifier: MSIP-CRM-SEC-SIP005AFS30

SRRC

Both the ARTIK 530 Module and the ARTIK 530 Development Kit comply with the standards set by the People's Republic of China.

CMIIT ID: 2017AJ3123 (M) (ARTIK 530 Module)

CMIIT ID: 2017AJ2921 (ARTIK 530 Development Kit)

RoHS Compliance

The ARTIK 530 Module complies with the hazardous substance limits of directive 2011/65/EU and the conformity assessment procedure as outlined in Decision 768/2008/EC, Annex II, Module A, Point 2, as well as RoHS harmonized standard EN 50581.

Report reference number: F690101/LF-CTSAYGU16-06911

HDMI Compliance

The ARTIK 530 Module passed the self-test, HDMI CTS version 1.4b on 8/26/2016 provided by HDMI Licensing LLC.

FCC Regulatory Disclosures

This device complies with Part 15 of the FCC`s Rules. Operation is subject to the following two Conditions: (1) This device may not cause harmful interference, and (2) This device must accept any interference received, including interference that may cause undesirable operation.

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/ TV technician for help.

This equipment complies with FCC radiation exposure limits set forth for an uncontrolled environment. This equipment should be installed and operated with a minimum distance of 20cm between the transmitter's radiating structure(s) and the body of the user or nearby persons.

This module is intended for OEM integration. The OEM integrator is responsible for FCC compliance and compliance with all applicable regulations including those for modular transmitters 47 C.F.R. 15.212. The OEM product must comply with all applicable labeling requirements including those contained in 15 C.F.R. 15.19. The OEM is solely responsible for certification and testing and labeling of its own products. In addition to any independently required labels, the OEM shall also affix to the outside of a device into which the module is installed a label referring to the enclosed module. This exterior label should be prepared in a legible font and permanently affixed and using the wording "Contains Transmitter Module FCCID: A3LSIP005AFS30"

The OEM is required to ensure that the end product integrates this module so as to maintain a minimum distance of 20 cm between the equipment's radiating structure(s) and the body of the user or nearby persons. The OEM shall also advise its end user of this requirement as required by applicable rules.

The OEM shall require that the end user of its product be informed that the FCC radio frequency exposure guidelines for an uncontrolled environment can be satisfied. The OEM shall further inform its end user that any change or modifications to this module not expressly approved by the manufacturer will void the warranty and the users' authority to operate the equipment.

INDUSTRY CANADA REGULATORY DISCLOSURES

INDUSTRY CANADA STATEMENT

This device complies with Industry Canada license-exempt RSS standard(s). Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Cet appareil est conforme avec Industrie Canada exempts de licence standard RSS (s). L'opération est soumise aux deux conditions suivantes:(1) cet appareil ne peut causer d'interférences, et (2) cet appareil doit accepter toute interférence, y compris les interférences qui peuvent causer un mauvais fonctionnement de l'appareil.

INDUSTRY CANADA RADIATION EXPOSURE STATEMENT AND LIMITATIONS ON USE

This equipment complies with IC RSS-102 radiation exposure limits set forth for an uncontrolled environment. This equipment should be installed and operated with minimum distance 20 cm between the radiator and your body. This equipment should be installed and must not be co-located or operating in conjunction with any other antenna or transmitter.

This equipment is restricted to indoor use in the 5.15-5.25 GHz range. This equipment is not able to be operated at 5600-5650. In the United States and Canada, only Channel 1~11 can be operated and these channel assignments deal only with the 2.4 GHz range.

The end product must be labeled to display the Industry Canada certification number of the module.
"Contains transmitter module IC: 649E-SIP005AFS30"

Le dispositif d'accueil doivent être étiquetés pour afficher le numéro de certification d'Industrie Canada du module.
"Contient module émetteur IC : 649E-SIP005AFS30"

EU Regulatory Disclosures

CE Statement*

The following statement must be supplied with each product but can be printed in the user manual, the packaging, or provided as a separated leaflet.

> Hereby, Samsung declares that this IoT Module is in compliance with the essential requirements and other relevant provisions of Article 3 of the R&TTE Directive 1999/5/EC, 2004/108/EC and RoHS directive 2011/65/EU.
> "The declaration of conformity may be consulted at [www.artik.io/certification]"

The 5150 - 5350 MHz and 5470 - 5725 MHz bands are for indoor use only.

The OEM is required to ensure that the end product integrates this module so as to maintain a minimum distance of 20 cm between the equipment's radiating structure(s) and the body of the user or nearby persons. The OEM shall also advise its end user of this requirement as required by applicable rules.

ORDERING INFORMATION

Please contact a sales representative in your area using the ARTIK official webpage – http://www.artik.io

LEGAL INFORMATION

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