MacroGiga Electronics Ltd. Co.

MG126, BLE Transceiver

Data Sheet

Revision History:

Rev. No.	History	Issue Date	Remark
0.1	Initial issue	April 3, 2015	Preliminary
0.2	update rf pin info	April 23, 2015	Preliminary
0.3	Update block diagram and application schematic	June 4, 2015	Preliminary
0.4	Update pinout info	June 9, 2015	Preliminary
0.5	Update TX power consumption	Nov 2, 2015	Preliminary
0.6	Add QFN16, Update Reflow profile	June 9, 2016	Preliminary
0.7	Update characteristic	Dec 11, 2016	Preliminary
1.0	Initial release	Feb 8, 2017	release
1.1	Update package info	April 6, 2017	release
1.2	Add ESD info	July 5, 2017	release
1.3	Update characteristic	Sept 4, 2017	release

Table of Contents

1. Overview

MG126 is a single mode BLE RF transceiver with software configurable registers, embedded packet handling engine, and designed for ultra low power Bluetooth Smart Devices.

The chips are configured and operated via the 4-wire SPI(Serial Peripheral Interface).

Internal voltage regulators ensure a high Power Supply Rejection Ratio (PSRR) and a wide power supply range(1.9~3.6V).

1.1 Features

- Radio

Worldwide 2.4GHz ISM band operation with 2MHz channel spacing

Common RX and TX pins

GFSK modulation

1Mbps air data rate

- Transmitter

Programmable output power: -28 ~ +4 dBm, without an external RF PA

20mA at 0dBm output power

- Receiver

Integrated channel filters

-85 dBm sensitivity

Programmable LNA gain

- Baseband

Dedicated logic performs:

    Cyclic redundancy check

Data whitening

Access code correlation

- Host Interface

4-wire hardware SPI

Max 10Mbps

- Power Management

Integrated voltage regulator

1.9 to 3.6V supply range

Idle modes with fast start-up times for advanced power management

50 uA in Standby mode, 3 uA in sleep mode

Max 1.5ms start-up from sleep mode

- Low cost BOM

Provides a single-ended RF TX / RX port pin

Single end RF output, No balun needed

Built-in 32.768KHz oscillator, no need external RTC crystal

Support low cost crystal(12MHz or 16MHz)

1.2 Typical Application

- Remote Controller

- Sport and Fitness sensors

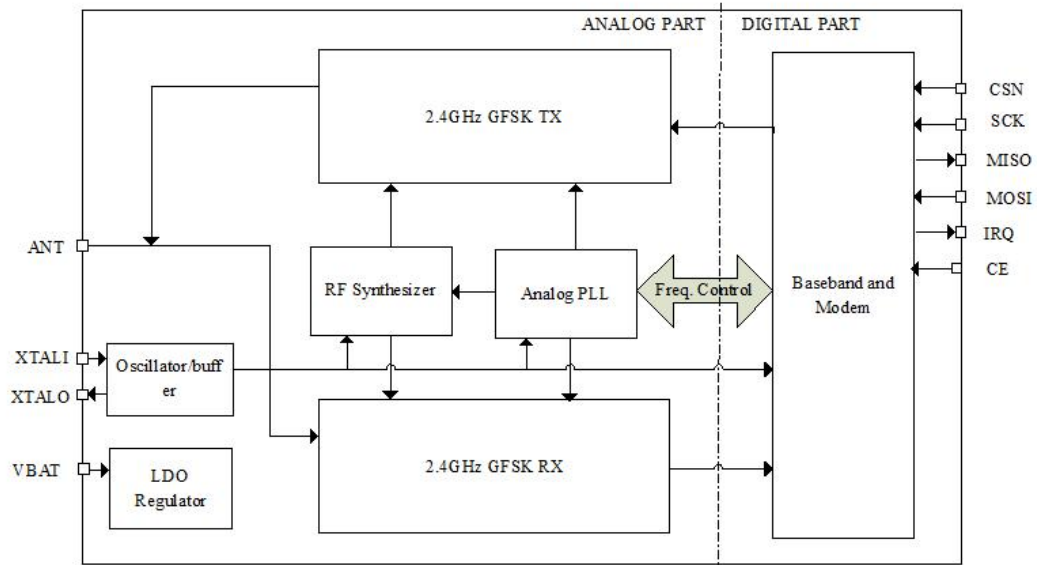- Wireless keyboard and mouse

- BLE watches

1.3 Block Diagram

Figure1.1 Block Diagram

2. Pin Description

Pin No.	Symbol	I/O	Function Description
1	CSN	DI	SPI Chip Select
2	VSS	Power	Ground (0V)
3	SCK	DI	SPI Clock
4	MOSI	DI	SPI Slave Data Input
5	MISO	DO	SPI Slave Data Output
6	DVDD	Power	Digital VDD 1.2v Output
7	VSS	Power	Ground (0V)
8	XTALO	AO	Crystal Pin
9	XTALI	AI	Crystal Pin
10	VBAT	Power	Power Supply
11	VSS	Power	Ground (0V)
12	ANT	RF	Antenna interface
13	VBAT	Power	Power Supply
14	VSS	Power	Ground (0V)

15	IRQ	DO	Maskable interrupt pin
16	CT	DI	Test Use

Table2.1 MG126 Pin Description

3. Example Application Schematic

MG126 with single ended RF output, crystal and decoupling capacitors.
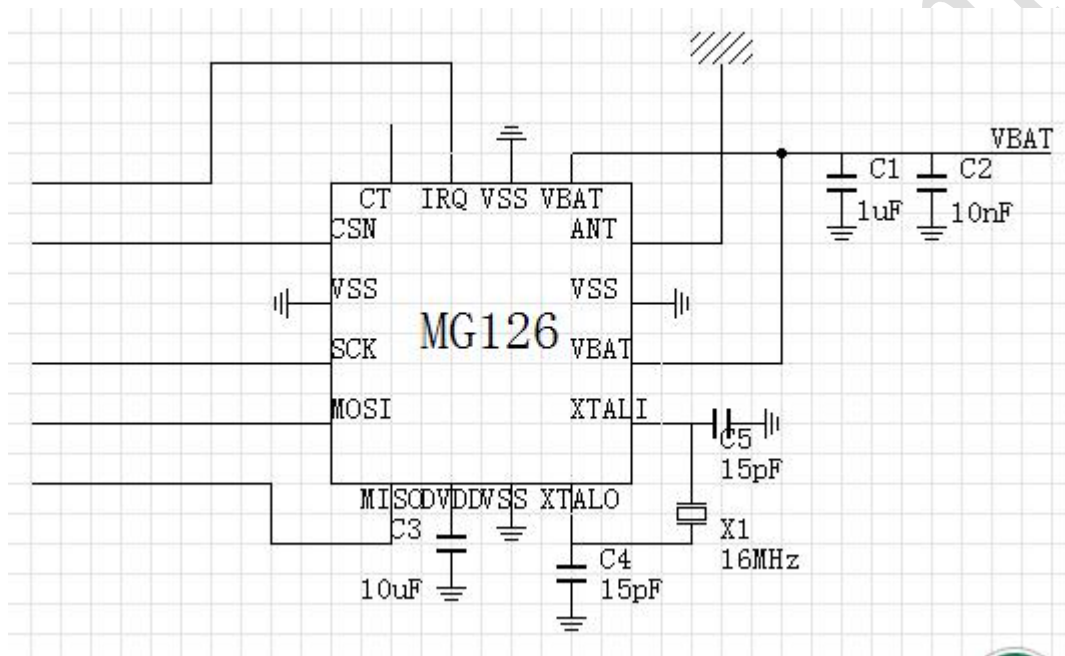

Figure 3.1 MG126 Example Application Schematic

4. Operating modes

The chip has 4 operating modes:

- Standby

- Sleep

- TX active

- RX active

5. Data and Control Interface

The data and control interface gives you access to all the features in the chip. The data and control interface consists of the following digital signals:

- IRQ (this signal is active low and is controlled by maskable interrupt sources)

- CSN (SPI signal)

- SCK (SPI signal)

- MOSI (SPI signal)

- MISO (SPI signal)

5.1 Features

- 4-wire SPI serial interface, as slave

- up to 10Mbps data rate

- Easily configurable register map

5.2 Functional Description

The SPI is a standard SPI with a maximum data rate of 10Mbps.

5.3 SPI Timing

The interface supports SPI. SPI operation and timing is given in Figure 5.3.1 and Figure 5.3.2. The device must be in one of the standby modes or sleep mode before writing to the configuration registers.
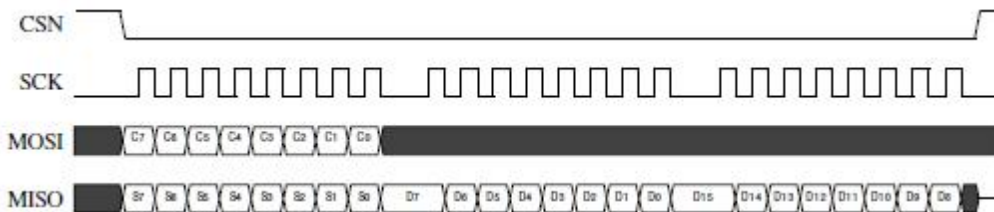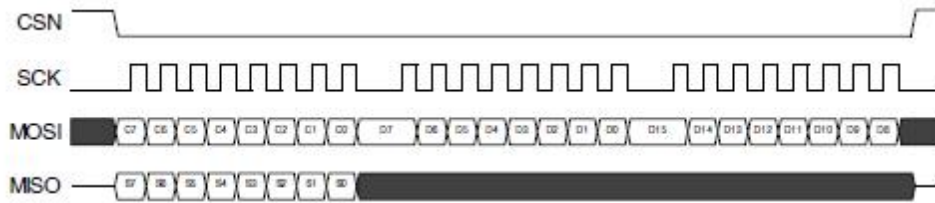

Figure 5.3.1 SPI read operation
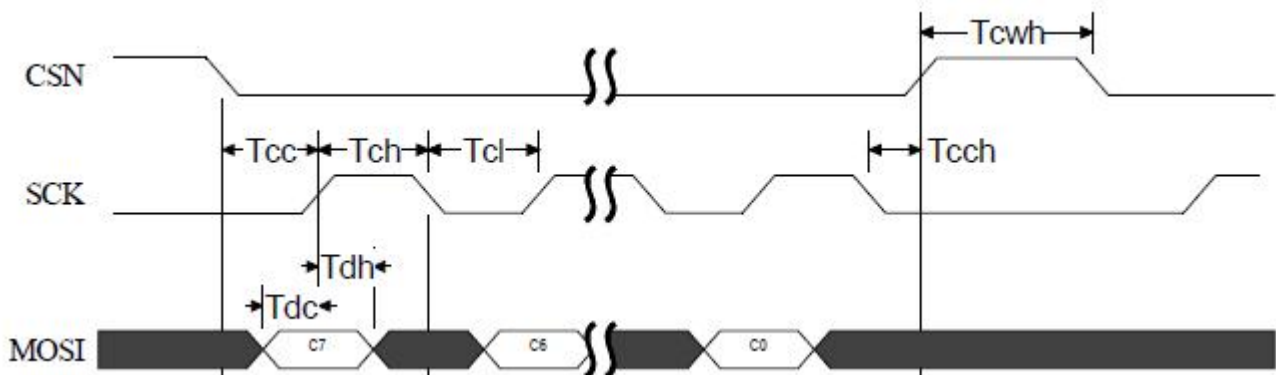
Figure 5.3.2 SPI write operation

Figure 5.3.3 SPI timing diagram

Symbol	Parameters	Min.	Max	Unit
Tcc	CSN to SCK setup	2	-	ns
Tch	SCK high time	40	-	ns
Tcl	SCK low time	40	-	ns
Tcwh	CSN inactive time	50	-	ns
Tcch	SCK to CSN hold	2	-	ns
Tdc	Data to SCK setup	2	-	ns
Tdh	SCK to Data hold	2	-	ns

5.4 Interrupt

The chip has an active low interrupt (IRQ) pin. The IRQ pin is activated by the state machine, and is

resets when MCU writes '1' to the IRQ source bit in the STATUS register. The IRQ mask in the register is used to select the IRQ sources that are allowed to assert the IRQ pin. By setting one of the MASK bits high, the corresponding IRQ source is disabled. By default all IRQ sources are enabled.

6. Register Map

You can configure and control the radio chip by accessing the register map through the SPI by using read and write commands.

7. Electrical Characteristic

Absolute Maximum Ratings

		MIN	MAX	UNIT
Supply Voltage	All supply pins have the same voltage	0	3.6	V
Input RF level			10	dBm
Storage temperature range		-40	125	℃
ESD	According to human-body model		4	KV
	According to charged device model		800	V
	According to man-machine model		200	V

Recommended Operating Conditions

	MIN	NOM	MAX	UNIT
Operating ambient temperature range, T_A	-40		85	℃
Operating supply voltage	1.9		3.6	V

Electrical Characteristics

Conditions: VDD = +3V, VSS = 0V, TA = - 40ºC to + 85ºC

Symbol	Parameter	Notes	Min.	Typ.	Max.	Unit

	General RF condition					
f_{OP}	Operating frequency		2402		2480	MHz
R_{GFSK}	Air data rate			1000		kbps
$F_{channel}$	Non-overlapping channel spacing			2		MHz
	Transmitter Operation condition					
P_{RF}	Maximum output power				+4	dBm
	Receiver Operation					
RX_{SENS}	Sensitivity (0.1% BER)			-85		dBm
	Power on Reset					
T_{RUP}	Power ramp up time				100	ms
T_{POR}	Power on reset time		1.5	5.3	10.3	ms

Table 7.1 Electrical Specification

8. Current Consumption

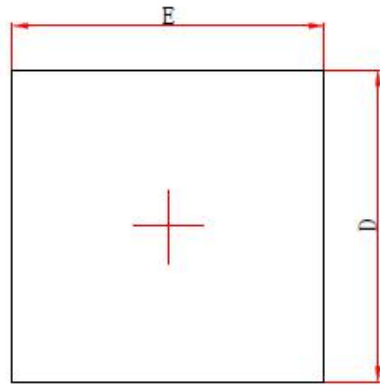Table 8.1 shows total typical current consumption measured at the battery.

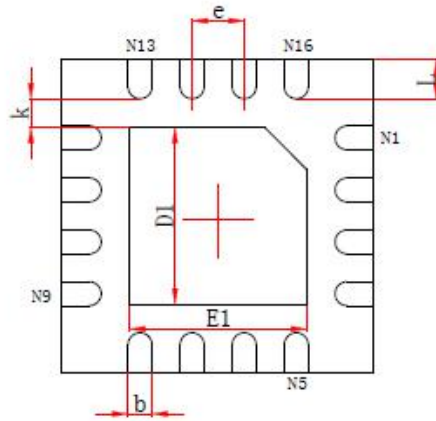| Mode	Description	Total Typical Current at 3.0v
Standby	In wakeup state, no TX, no RX	50 uA
sleep	Sleep. wakeup through SPI command	3 uA
TX active	In transmitting	20 mA @ 0dBm output power
RX active	In receiving	20 mA

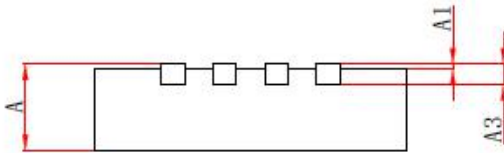*Table 8.1 Current Consumption*
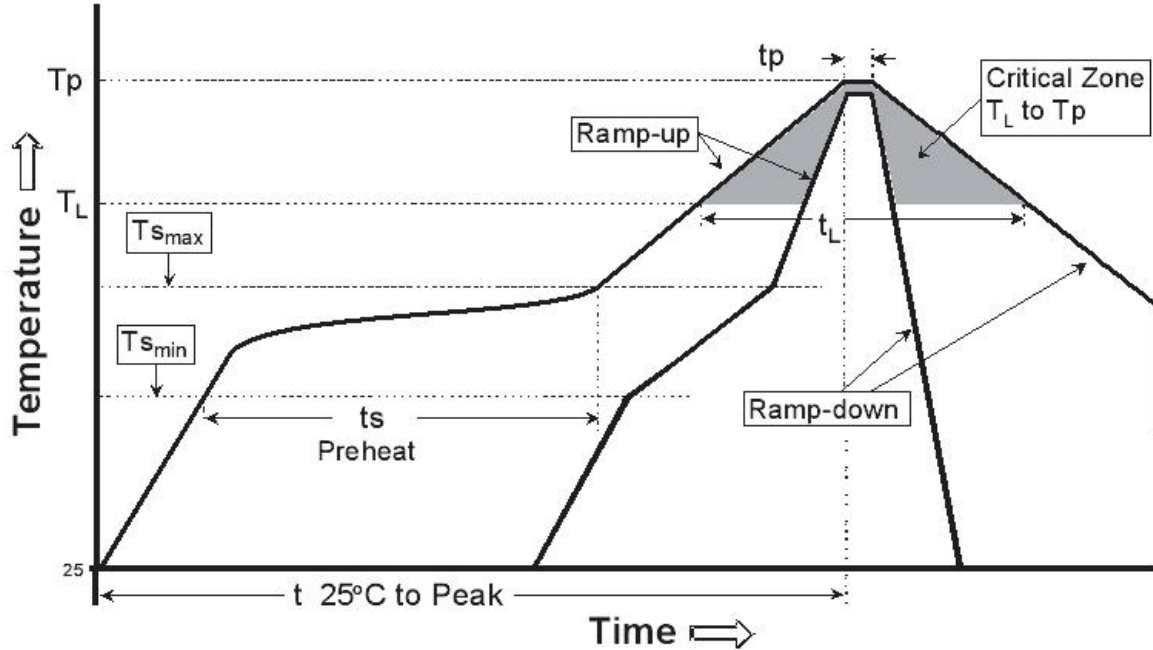
9. Package Information

QFN16 3x3

Top View

Bottom View

Side View

Symbol	Dimensions in Milimeters		Dimensions in Inches	
	Min.	Max.	Min.	Max.
D/E	2.900	3.100	0.114	0.122
D1/E1	1.600	1.800	0.063	0.071
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.203 REF		0.008 REF	
k	0.200 MIN.		0.008 MIN.	
b	0.180	0.300	0.007	0.012
e	0.500 TYP.		0.020 TYP.	
L	0.300	0.500	0.012	0.020

Table 9.1 QFN16 3x3 Package outline

10. Reflow Profile
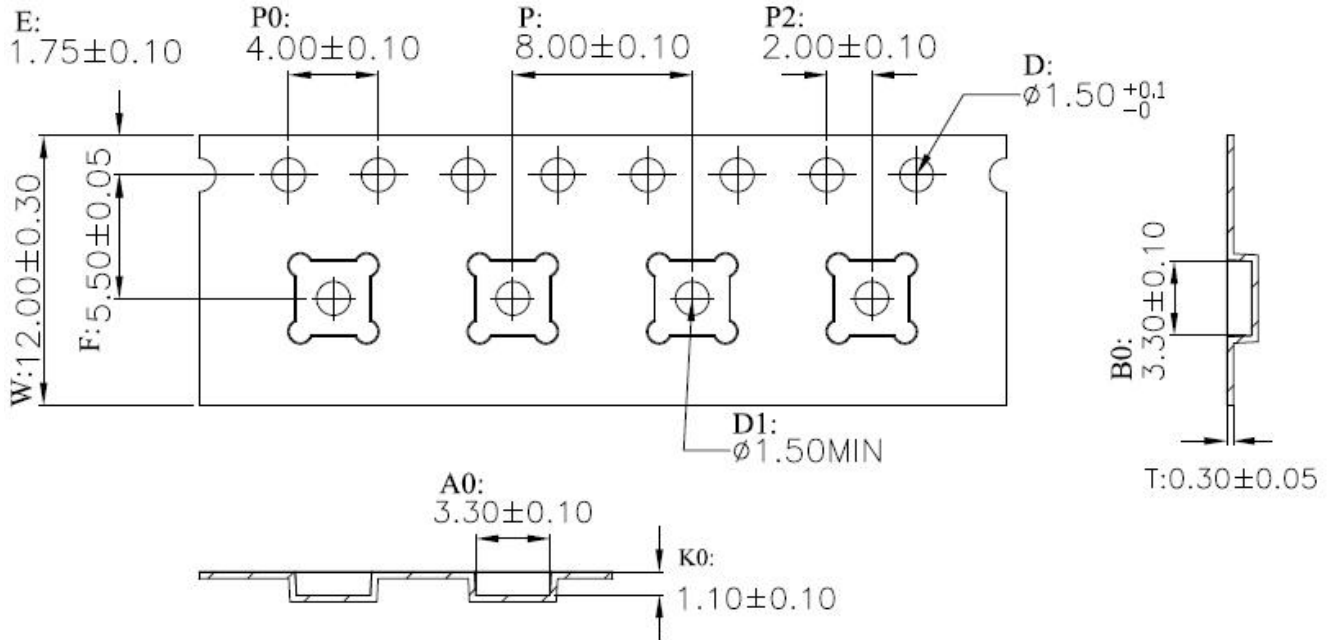
Follow：IPC/JEDEC J-STD-020 C

IPC-020c-5-1

Table 5-2 Classification Reflow Profiles

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Average Ramp-Up Rate (Ts_{max} to Tp)	3 °C/second max.	3° C/second max.
Preheat – Temperature Min (Ts_{min}) – Temperature Max (Ts_{max}) – Time (ts_{min} to ts_{max})	100 °C 150 °C 60-120 seconds	150 °C 200 °C 60-180 seconds
Time maintained above: – Temperature (T_L) – Time (t_L)	183 °C 60-150 seconds	217 °C 60-150 seconds
Peak/Classification Temperature (Tp)	See Table 4.1	See Table 4.2
Time within 5 °C of actual Peak Temperature (tp)	10-30 seconds	20-40 seconds
Ramp-Down Rate	6 °C/second max.	6 °C/second max.
Time 25 °C to Peak Temperature	6 minutes max.	8 minutes max.

Note 1: All temperatures refer to topside of the package, measured on the package body surface.
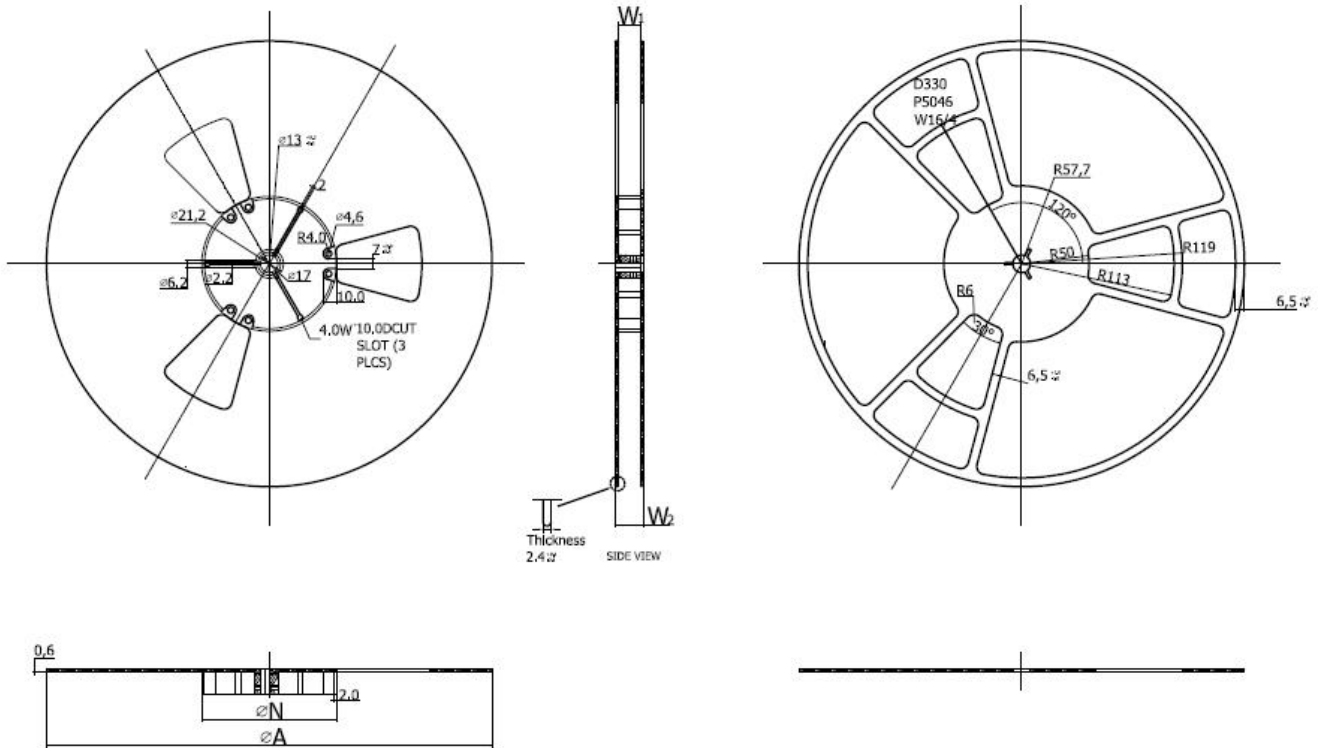
11. Tape and Reel Information

11.1 Tape Information

W	12.00 ±0.30	mm
A0	3.30 ±0.10	mm
B0	3.30 ±0.10	mm
K0	1.10 ±0.10	mm

11.2 Reel Information

Package Type	Tape Width	φA	φN	W1	W2max
3x3x0.8mm QFN	12 mm	330 mm	100 mm	12.8 mm	18.2 mm

Thanks