

Digital Design IE1204

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Module 1

Aim

The aim of the lab in module 1 was to build a three-input CMOS AND gate.

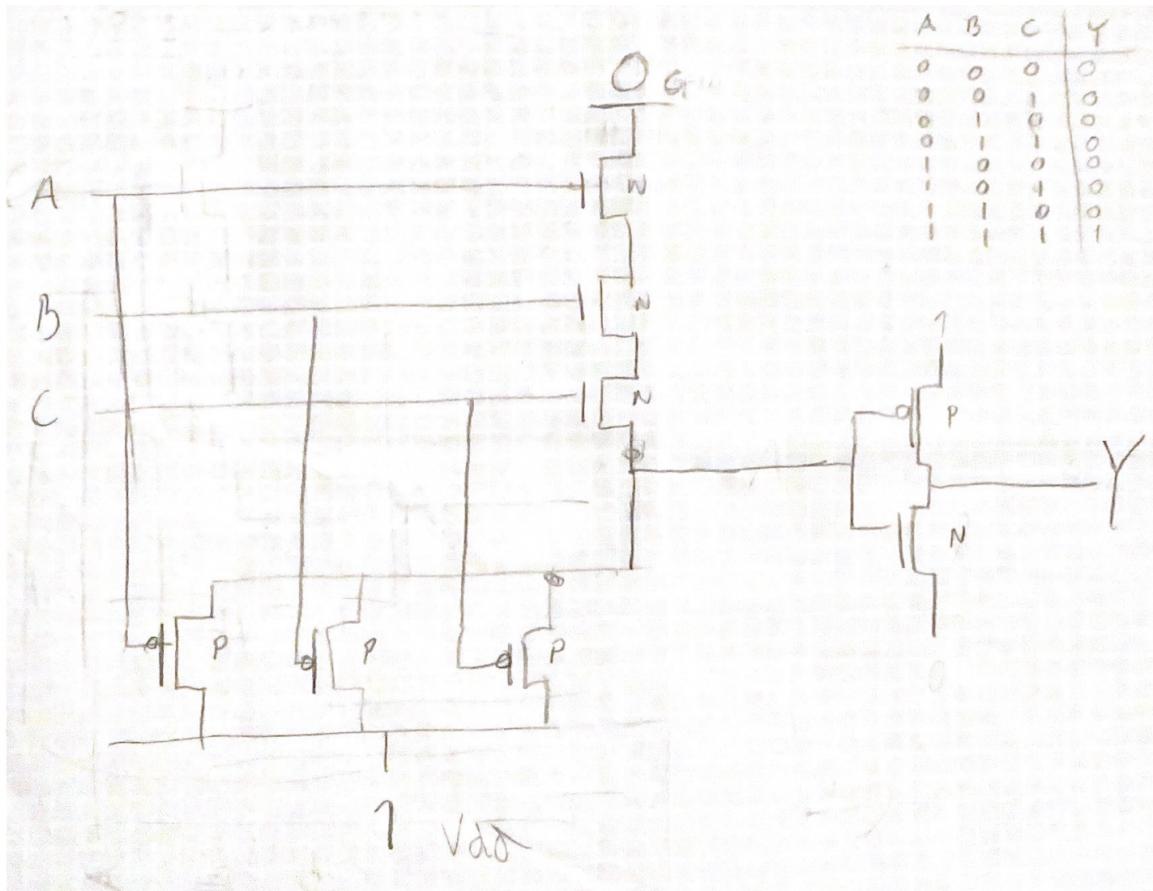
Background

I was born on the 14th of the month (even) therefore, I built a three-input CMOS AND gate. In order to build an AND gate, a NAND gate was first built and inverted using a NOT gate. The result in return was an AND gate. The NAND gate was built using 3 NMOS in series along with 3 PMOS connected in parallel. Additionally, the NOT gate was built using one PMOS and one NMOS.

Table 1: A truth table displaying the possible outcomes of a three-input AND gate. The inputs A B, C are shown below along with output Y.

<i>A</i>	<i>B</i>	<i>C</i>	<i>Y</i>
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	1

Circuit



Circuit 1: The Circuit illustrates how a three input CMOS AND gate is built using four NMOS and four PMOS.

Figure 1

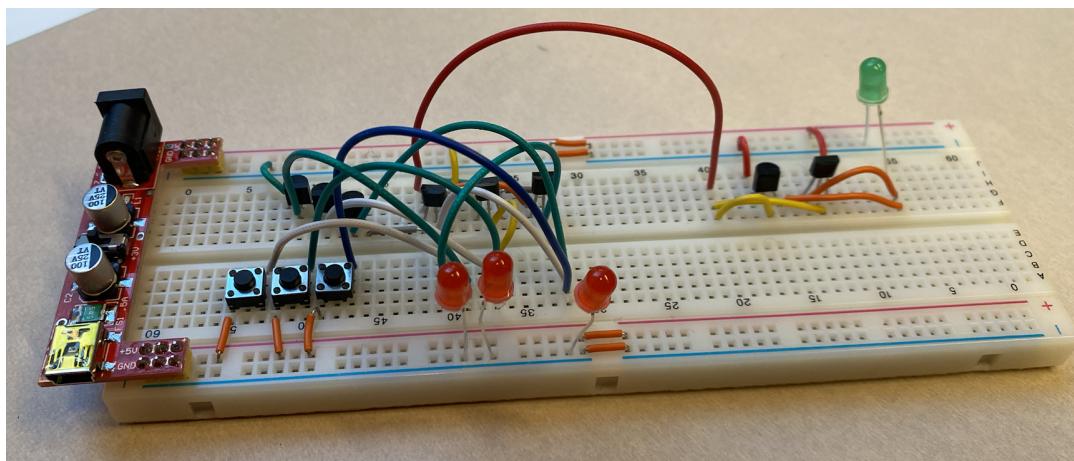


Figure 1: The figure represents the three input CMOS AND gate on a breadboard.

Module 2

Aim

The aim of the lab in module 2 was to build a combinational logic circuit using integrated circuits. From my date of birth (2002-11-14) a 16 bits output gate was generated. In order to achieve the 16 bits truth table, 3 fixed bits were used (001). Thus, a 4x4 k-map was also made.

Table 1: A table displaying the date of birth in binary with additional fixed bits (001).

Year-bit				Month-bits				Fixed bits			Day-bits				
0	0	1	0	1	0	1	1	0	0	1	0	1	1	1	0

Table 2: Table 2 displays the 16 bits from the DOB in a truth table with rows 0- 15 respectively. The truth table below shows q0, q1, q2, q3 as inputs and Y as an output.

Row	q3	q2	q1	q0	Y
0	0	0	0	0	0
1	0	0	0	1	1
2	0	0	1	0	1
3	0	0	1	1	1
4	0	1	0	0	0
5	0	1	0	1	1
6	0	1	1	0	0
7	0	1	1	1	0
8	1	0	0	0	0
9	1	0	0	1	1
10	1	0	1	0	0
11	1	0	1	1	0
12	1	1	0	0	1
13	1	1	0	1	1

14	1	1	1	0	1
15	1	1	1	1	0

Figure 2

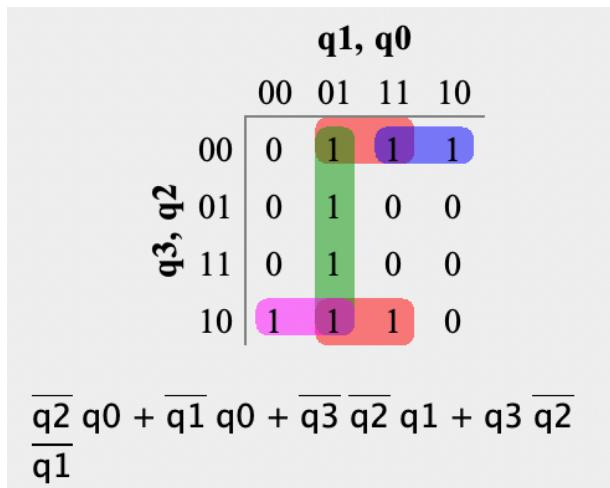


Figure 2: The figure above displays a 4x4 K-Map stimulated on Logisim. The K-Map was constructed from the truth table displayed in table 2. The figure also shows the boolean expression for sums of products.

Figure 3

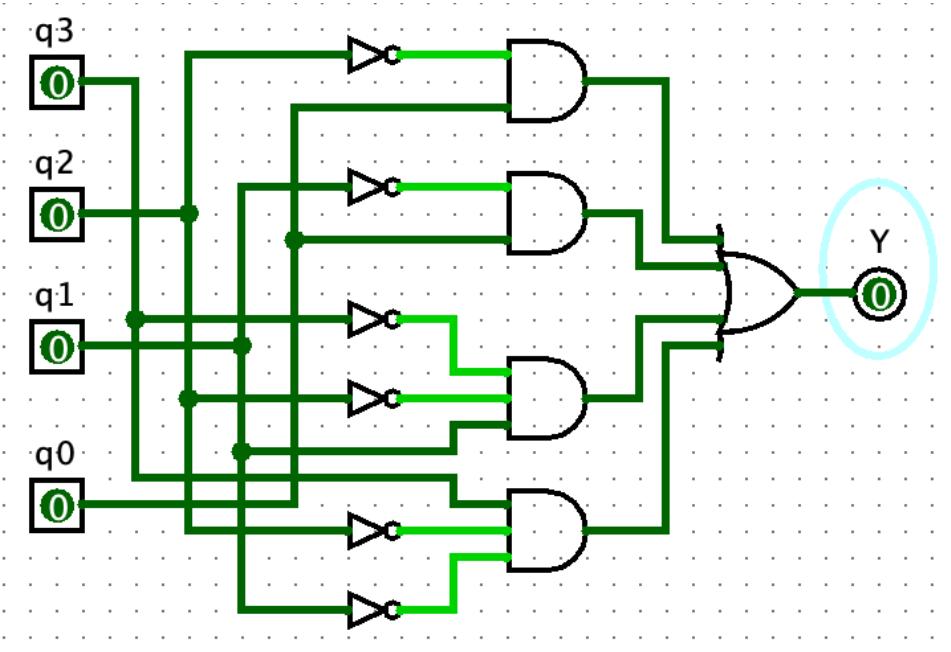


Figure 3: Figure 2 displays the logical circuit with 4 inputs (q_0, q_1, q_2, q_3) and Y as an output. It demonstrates a logical circuit with two, two-input and gates as well as two, three-input and gates. The output Y is then connected to a four input OR gate.

Figure 4

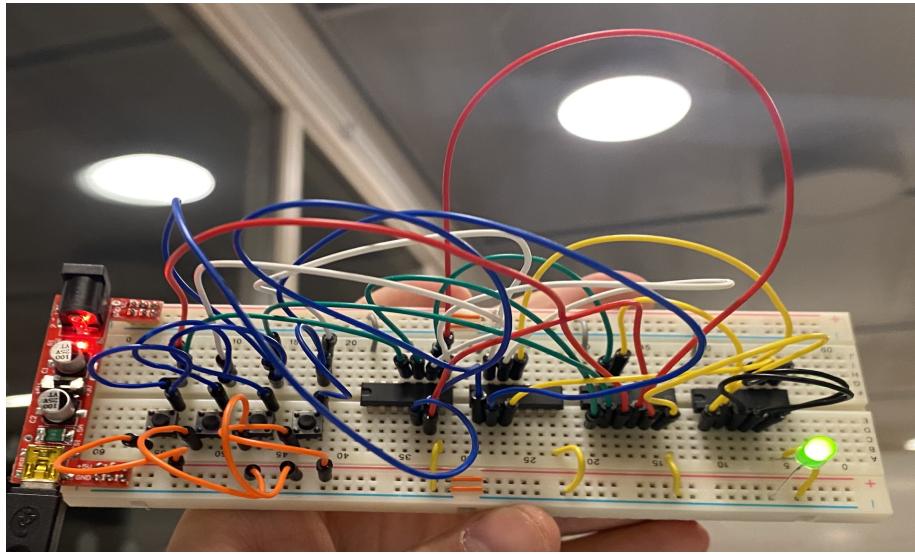


Figure 4: The figure above shows the combinational circuit from figure 2 displayed on a breadboard with IC's.

Module 3

Aim

The aim of the lab in module 3 was to build a finite state machine (FSM). The selected FSM was based on the month and date of the birthday. I was born on the 14th of November, hence I built the FSM based on November 1-16th, version 7.

Figure 5

**November 1-15
Version 7 ↓**

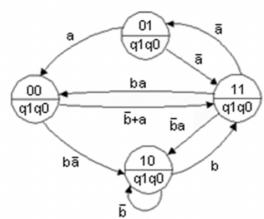


Figure 5: The figure above shows a finite state machine for the month of november 1-15, version 7.

Figure 6

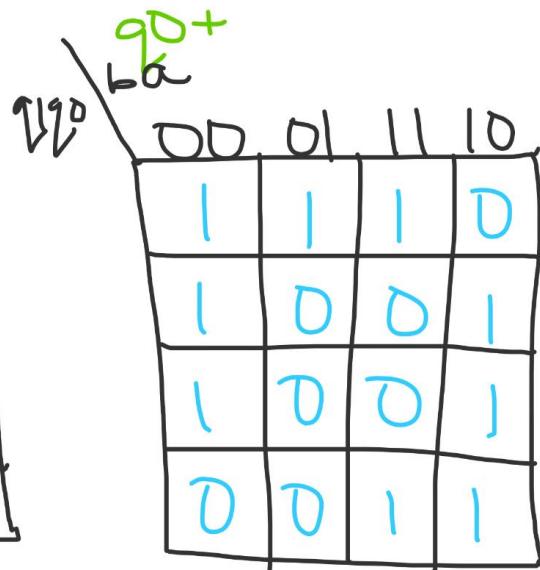
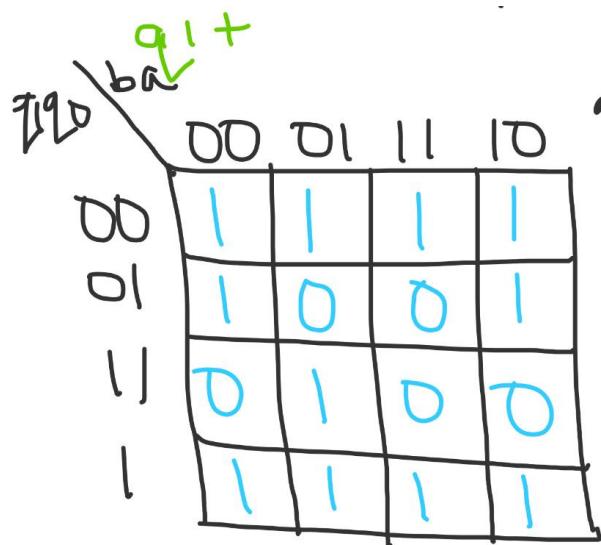
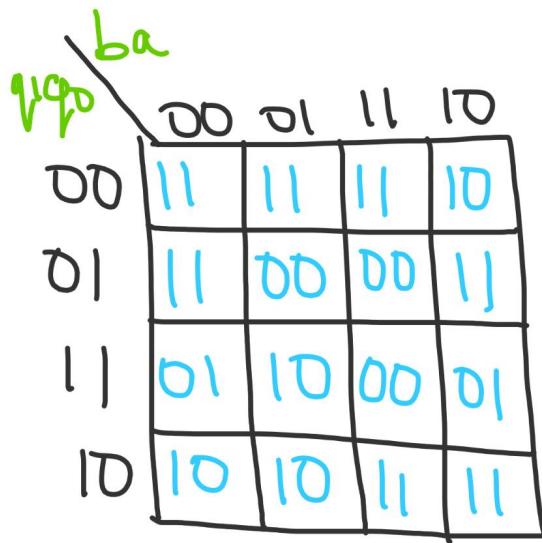


Figure 6: The figures above show the K-map for Q_0^+ and Q_1^+ .

Figure 7

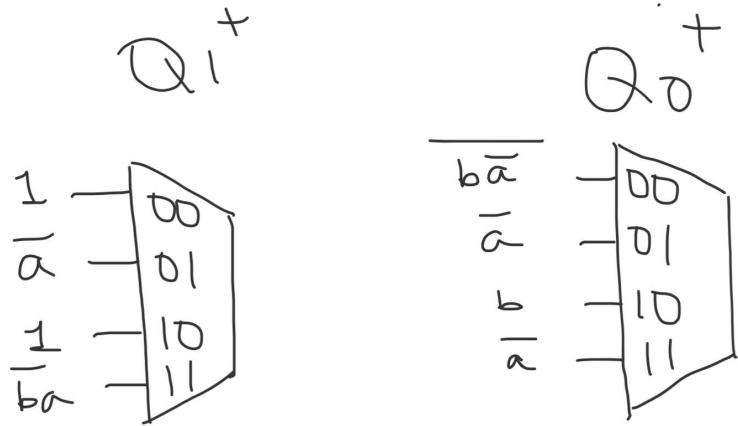


Figure 7: Figure 7 displays the MUX for Q1+ and Q0+.

Figure 8

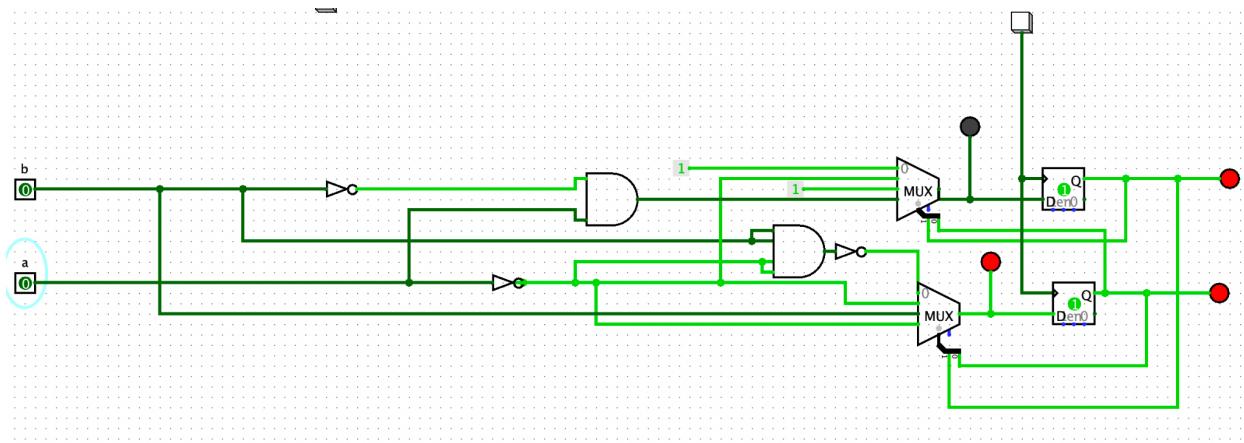


Figure 8: The figure above displays the finite state machine with input a and b as buttons and Q0 and Q1 as Dual flip flops as well as a clock

Figure 9

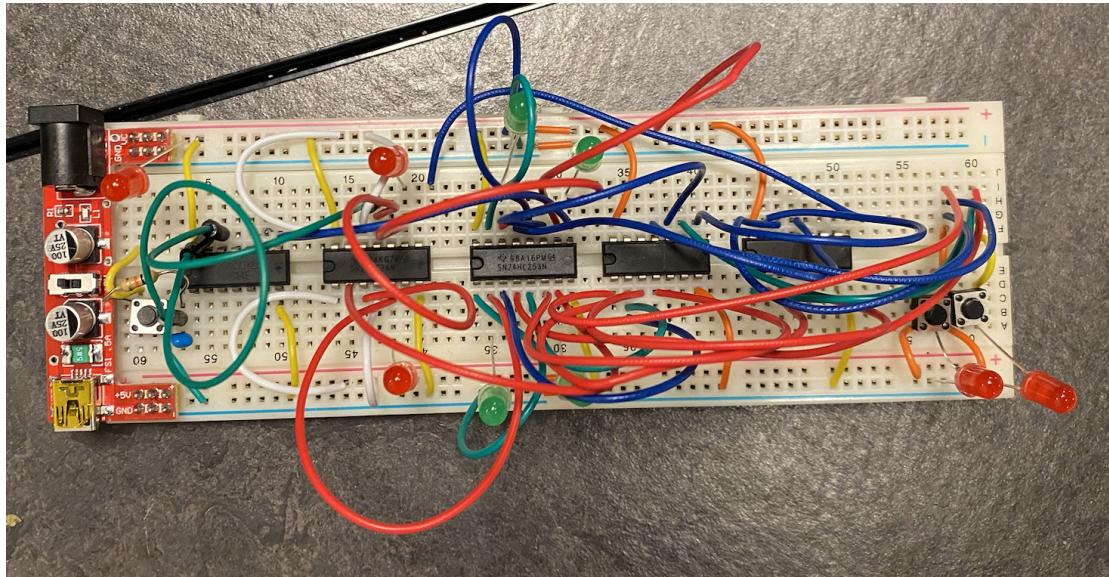


Figure 9: Figure 9 displays the FSM on a breadboard. The circuit is constructed with a 2 D-flip-flop, 2 MUX as well as 2 AND gates. Additionally, the clock was built using a Schmitt trigger IC.

Module 4

Aim

The aim of this lab in module 4 was to show the date of birth (8 digits) on the 7 segment display. The lab was constructed using ROM memory. My date of birth (20021114) is first converted into binary digits.

Figure 10

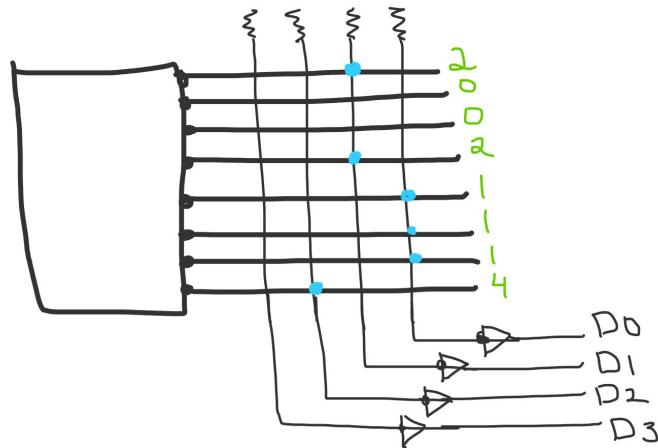


Figure 10: The figure above illustrates the circuit built in lab 4.

Figure 11

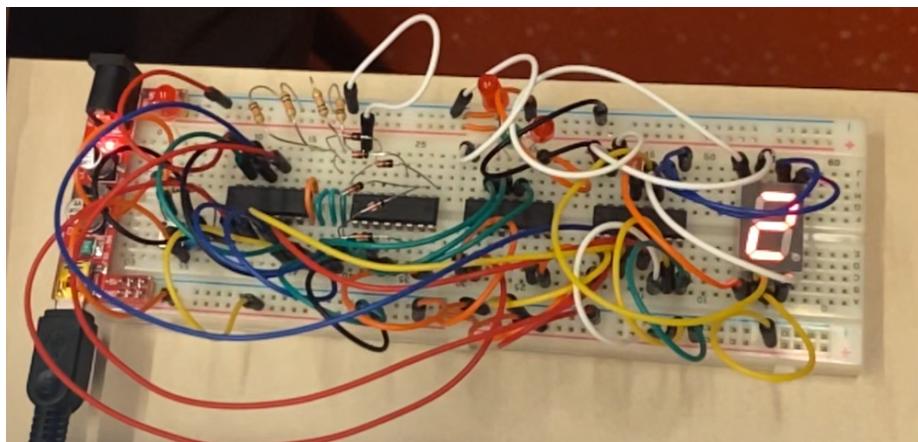


Figure 11: The figure above shows the circuit built on a breadboard.