Jordan University of Science and Technology

Department of Computer Engineering

Irbid, 22110, Jordan

VLSI, CPE 748

Assignment / Homework No. 7

Title: *Paper summarization and simulation of*

"Analytic Models of CMOS Logic in Various Regimes"

Day and Date: 10 May 2020

Analytic Models of CMOS Logic in Various Regimes- summary

Current research of circuit development is concentrating on reducing power consumption by decreasing power supply voltage Vdd. Now, the two most common metric for a good chip are power and speed. Semiconductor material is the base for the most integrated circuits. Years ago, sub-threshold played the main role in CMOS logic (the current between the source and drain when the transistor in weak inversion is called sub-threshold or leakage current, hence the gate-to-source voltage is below the threshold voltage). As transistor size scales down the voltages decreases, and sub-threshold conduction becomes more significant factor. Leakage can consume half of power, with the low power supply technology such as 0.2 V and the total power consumption is very low. These days sub-threshold is optimal factor for digital framework of independent power supply. Today, weak and strong inversions are fully used in digital circuits. For example, to choose digital logic field of application, focus on the slight difference of speed and power consumption relying on the two regions.

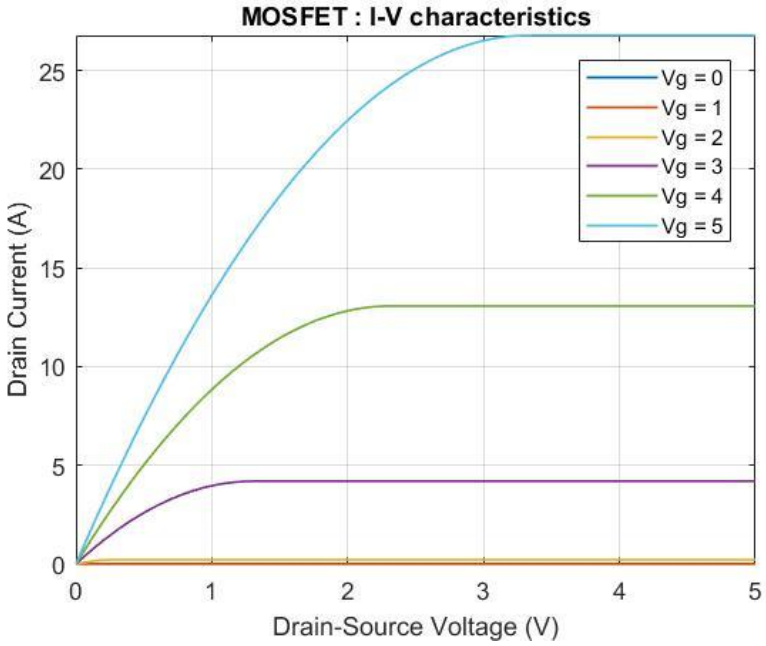
In this paper, authors study the relative analytical models of static and dynamic characteristic of CMOS digital circuits in three different regions strong, weak and mixed inversion. They analyze the analogy behavior and functional dependencies of parameters in CMOS regimes, besides the dependency of threshold voltage and delay time on temperature in static model. Moreover, the authors proposed dynamic model with constant current and they have shown that digital circuits with dynamic threshold voltage of MOS transistor (DT-CMOS) have better logic delay characteristics. They rely on current-voltage MOS models in strong and weak inversion regimes, and 180 nm technology as PSPICE parameters.

There are three static characteristics of MOS transistor. Vt is known as the gate-source voltage. On the other hand, Id (Vds,Vgs) characteristics in strong inversion (ON mode) there are two regions linear (non-saturated) region and saturation region as shown mathematically below:

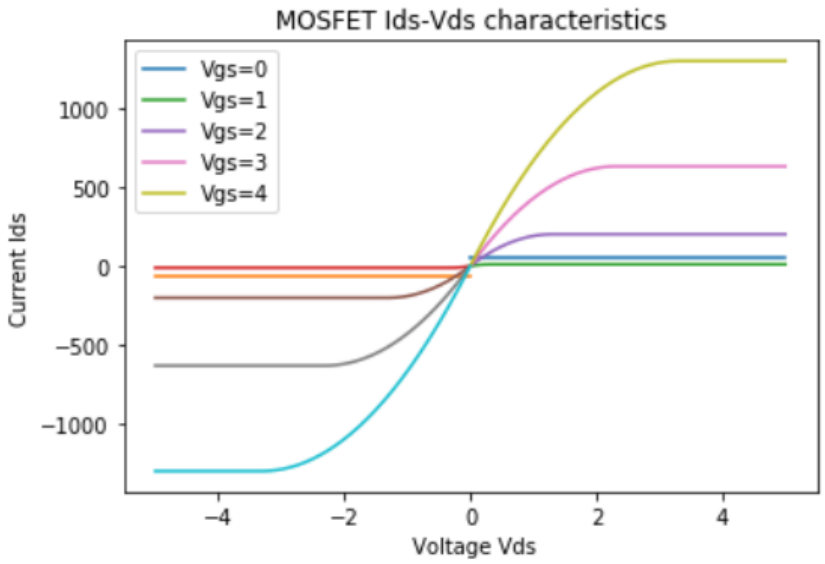
$$I_d = \begin{cases} k\left[2\left(V_{gs} - V_t\right)V_{ds} - V_{ds}^2\right], & V_{ds} < V_{gs} - V_t \\ k\left(V_{gs} - V_t\right)^2, & V_{ds} > V_{gs} - V_t \end{cases}$$

Where:

$$k = \frac{\mu C_{ox}}{2t_{ox}}\left(\frac{W}{L}\right).$$



It's noticed that, in saturation region Id is independent of Vds and become a linear function of gate-source voltage Vgs. μ is a mobility of major charge carriers (electrons and holes in nMOS to pMOS transistor), $C_{ox} = \varepsilon_{ox} / t_{ox}$ is gate capacitance (ε_{ox} is a dielectric constant, t_{ox} is a thickness of the gate oxide), *W* and *L* are width and length of the channel. In weak inversion the Vds is Fixed on $V_{ds} = 3\phi_t$ where $\phi_t = 26\,\text{mV}$ at $T = 300\,\text{K}$ and Vgs = Vds – Vt.



In this paper, the authors displays **three Regimes of CMOS Logic** and they have come out with the third region which is not known before**.** CMOS inverter has been used as a base example to explore the CMOS logic regimes.

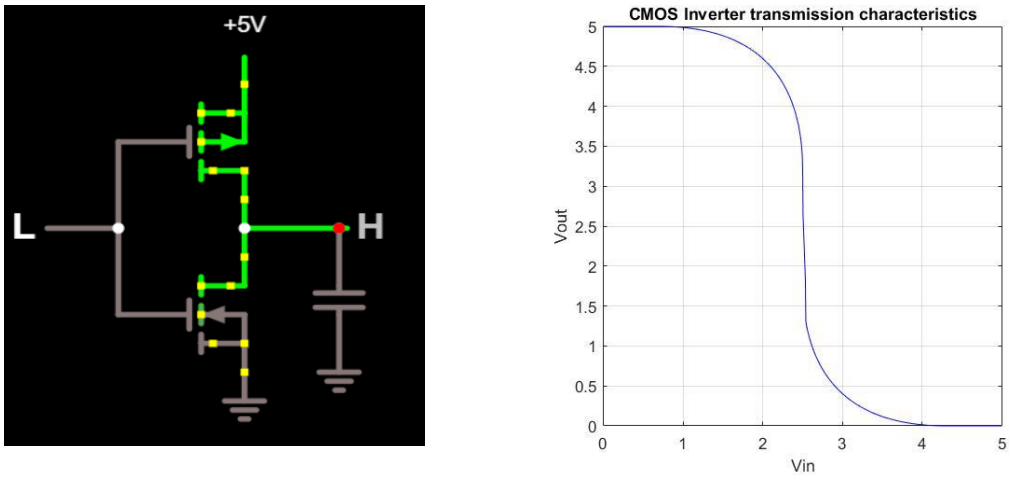


Fig . CMOS inverter (a) strong and weak inversion area on transfer characteristic in mixed regime (b).

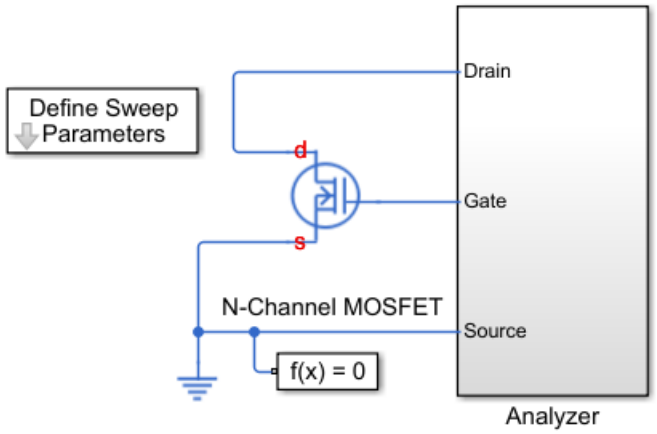
Drain current in pMOS must be the same in nMOS all the time, and Vdd equals the voltage across the pMOS and the voltage across the nMOS by KVL. Operating voltage range for three CMOS regimes are summarized in table 1.

	Inversion		
	Weak	Strong	Mixed
Power supply	$3\phi_t < V_{dd} < V_t$	$V_{dd} > 2V_t$	$V_t < V_{dd} < 2V_t$

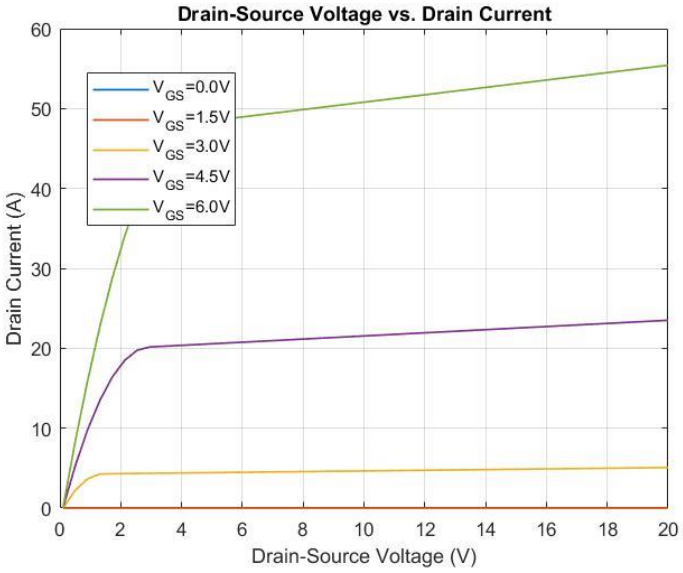
Table 1

Static CMOS circuits use complementary nMOS pulldown and pMOS pullup networks to implement logic gates or logic functions in integrated circuits. While, Dynamic gates use a clocked pMOS pullup. The implemented logic function or the logic gate is achieved through 2 modes of operation: Precharge and Evaluate. In this paper, authors display both static and dynamic CMOS.

Static transfer characteristics is illustrated in figure 2 using CMOS inverter and analyzing the weak and strong inversion



MOSFET Characterization Using Y Parameters



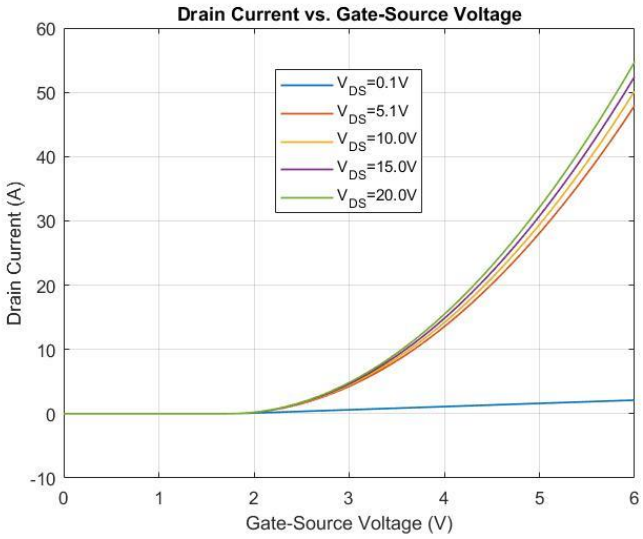
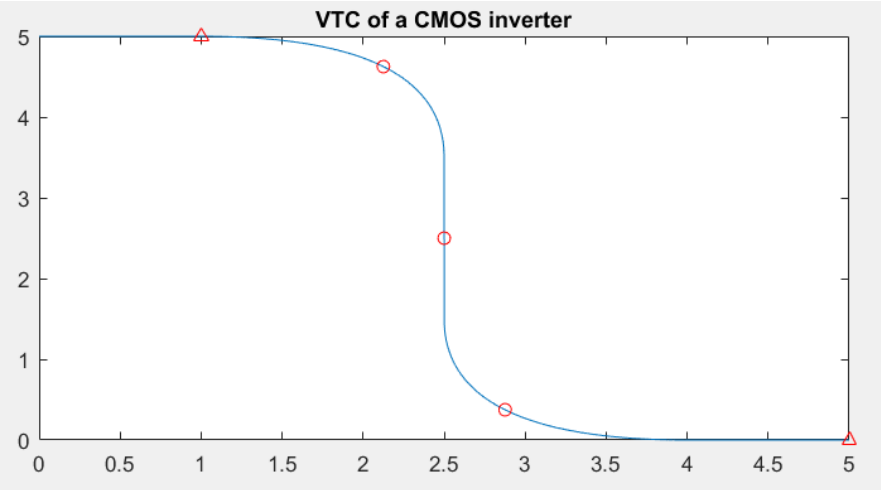
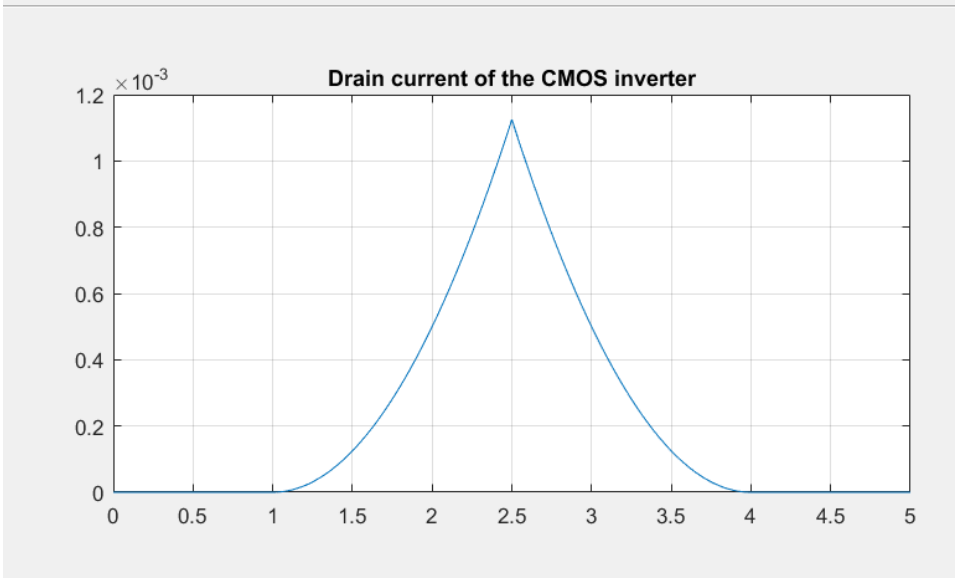


Fig . $I-V$ *in CMOS sub-threshold regime.*

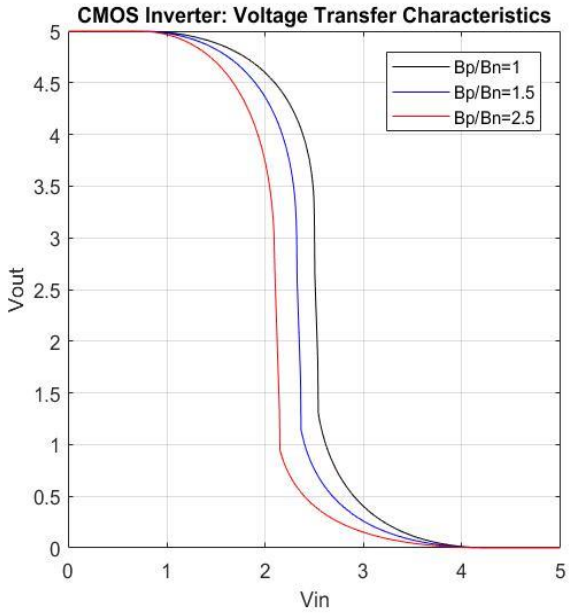




It's known that Vgsn = Vi and Vgsp = Vi-Vdd. For strong inversion ,let Vi = Vt then:

Vt = Vdd/2

And for the inverter in the weak inversion regime Inverters with different beta ratios $r = \beta_p/\beta_n$. Transfer characteristics in both regimes, besides from supply voltage, are dependent on CMOS transistors geometry ratio displays in figure 3.



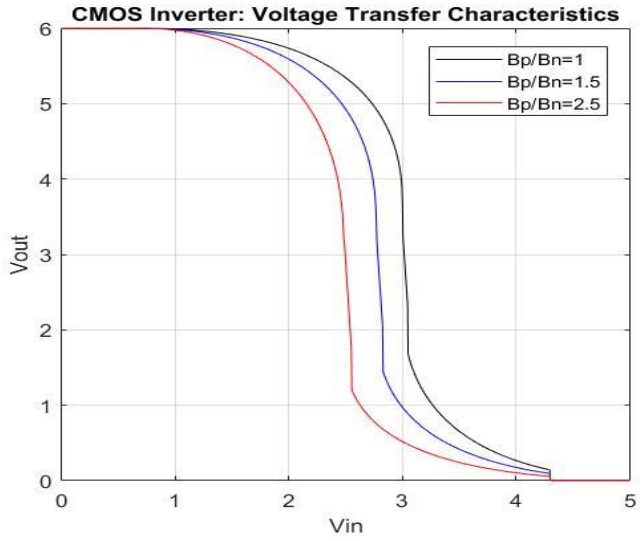


Fig *V –V inverter transfer characteristics in strong and weak inversion regime for different* W_p / W_n *ratio*

Power consumption is analyzed for static power consumption as the expression below:

$$P_S = V_{dd}\left(I_{dss} + I_{dsub} + I_g\right)$$

Whereas the dynamic power consumption is:

$$P_d = C_L V_{dd}^2 f$$

I_{dss} represents the current of inverse polarized p-n junction drain-source, and I_{dsub} is sub-threshold current while Vgs =0. Ig is tunelling current through gate which has its significance at CMOS nanometer technologies. Cl is load capacitance, and f is operating frequency. Power dissipation in CMOS in static phase has four reasons sub-threshold leakage through OFF transistors, gate leakage through gate dielectric, junction leakage from source/drain diffusions and contention current in ratioed circuits. However, dynamic power dissipation happen as a result of charging and discharging load capacitances as gates switch and/or short-circuit current while both pMOS and nMOS stacks are partially ON. And the total power dissipation equals the summation of both static and dynamic dissipation.

In dynamic models the value of power supply is different which leads to different values of capacitances and currents. And logic delay expressed as RC. In this paper, they describe the influence of lower value of power supply through the switching regime. It is defined by I_d - V_{ds} characteristics in both regions.

Dynamic delay between input and output signal of inverter is called propagation delay. During early stages of discharged, nMOS is saturated and pMOS is cutoff. The switch is on whenever the transistor is off and the opposite case in the on transistor. Hence, switching speed is limited by the required time for charge and discharge. Rise time tr = time for a waveform to rise from 20% to 80% of its steady-state value. Fall time, tf = time for a waveform to fall from 80% to 20% of its steady-state value. Propagation delay time, tpd = maximum time from the input crossing 50% to the output crossing 50%. In this paper, they studies the CMOS inverter as a basic optimal example to explore the delay model. In CMOS inverter, capacitances are performed between drain and body and between source and body of each transistor and gate capacitance, the wire capacitance also performs load. All capacitors are connected to the ground. The charge carrier between drain and source require shorter time than the charge and discharge in capacitor. This means on and off switching and initializing Id currents in pMOS and nMOS, which are shown in I-V static transistor characteristics.

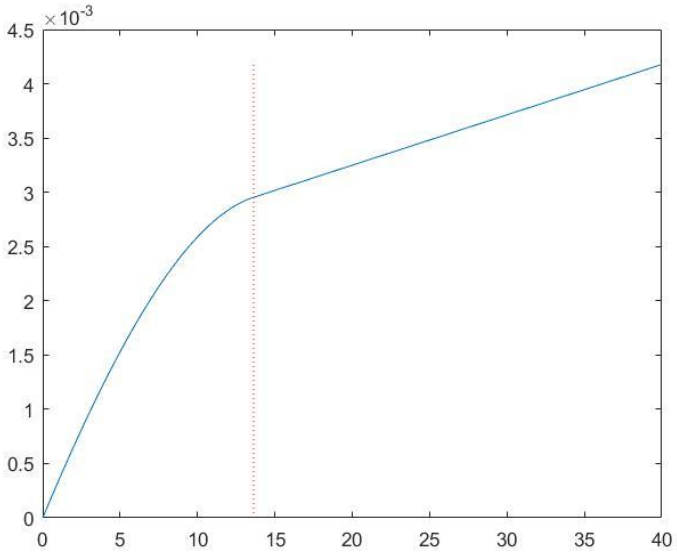


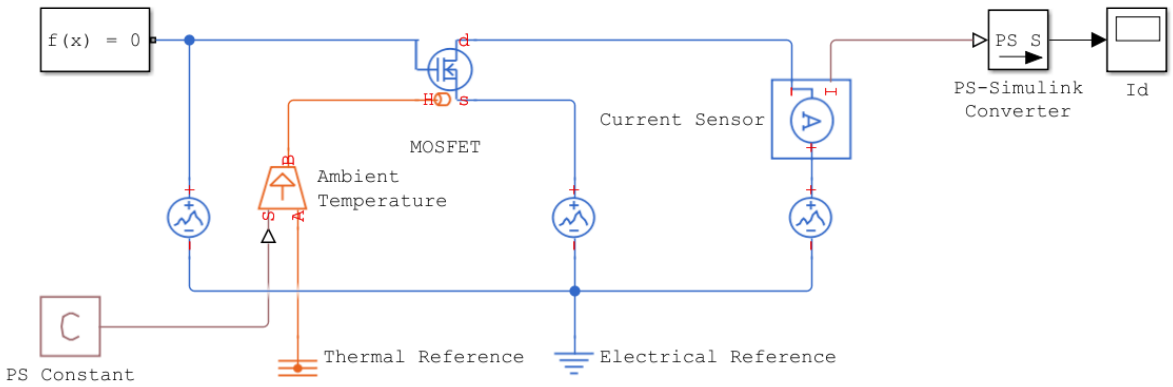
Fig. *– Operating point trajectory while charging*

To design the **optimal geometry** inverter, threshold voltages should implies

$$V_{tn} = |V_{tp}| = V_t$$

And transistor constants are equal $k_p = k_n$. Consider the transistor geometry is optimal when pMOS transistor channel width is μ_n/μ_p (around 2.5) times wider than NMOS.
NAND and NOR circuits are contain the same number of transistors in parallel and series structure. On the other hand, rise and fall time as well as the out resistance are different. Hence, circuit structure is asymmetric. In this paper, they implies the NAND and NOR circuits using the inverter by modifying its geometric characteristics.

Voltage threshold **temperature coefficient** relies on transistor geometry ratio, for example the symmetric CMOS inverter is independent on temperature. It has been noticed that the weak inversion has much higher changes in logic delay temperature than the strong inversion regime. The authors shows that "In temperature range from -40°C to 100°C, logic delay relative change in strong inversion regime is plus/minus few tenths of percent. In weak inversion regime, this range is from several hundreds of percent in plus, comparing to few tenths of percent in minus."



Thermal MOSFET Characteristics

This test model is used by the elec_thermal_mosfet_characteristics app. It is invoked by the app when generating current-voltage and capacitance-voltage characteristics.

delay times in weak inversion regime exponentially decreases with decrease of threshold voltage Vt . However, decrease of Vt results with increase of static consumption because sub-threshold current increases as well.