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Irbid, 22110, Jordan

VLSI, CPE 748

Assignment / Homework No. 7

Title: ***Doctoral Thesis summarization*** **of**

Characterization and Modeling of Low Frequency Noise and Dielectric Traps in Scaled MOSFET Devices

Day and Date: 12/05/2020

Characterization and Modeling of Low Frequency Noise and Dielectric Traps in Scaled MOSFET Devices, Summary

Abstract

A wide variety of novel complementary-metal-oxide-semiconductor (CMOS) devices that are strong contenders for future high-speed and low-noise RF circuits have been evaluated by means of static electrical measurements and low-frequency noise characterizations. Materials with a high dielectric constant (high-k) is necessary to replace the conventional SiO2 as gate dielectrics in the future in order to maintain a low leakage current at the same time as the capacitance of the gate dielectrics is scaled up.

The author in this Thesis focuses on the trapping effects of nanoscaled CMOS devices with high-K and high-quality SiON dielectrics. Specifically, 1/f noise mechanisms in these scaled devices are investigated. They additionally compared a variety of performances and physical properties of both N and P type advanced transistors. This dissertation also includes the device study of channel carbon ion implantation in nanoscaled CMOS devices fabricated with replacement gate technology. They describes the modeling and electrical characterization of nanoscaled high-K and SiON MOSFET devices. Moreover, They introduce surface roughness scattering through fluctuations in the normal electric field due to fluctuations in the free carrier density with a surface scattering parameter (β) proportional to the SPICE surface roughness parameter θS.

They aim to develop a quantum mechanical treatment of low-frequency noise to extend the "unified" noise model and includes remote Coulomb scattering and surface roughness

- the latter is a new consideration in the theory.

Their working methodology base on scaled NMOS devices with a composite dielectric consisting of a 0.5 nm SiO2 covered with a high-K, 1.6 nm HfO2 with a metal gate. They modeled remote Coulomb scattering into the dielectric film as traps in these films easily lie within a tunneling distance from the interface and conduct experimental characterization to validate the proposed model. They rely mainly on electron mobility in the improvement, while at the same time the Coulomb scattering is reduced. Besides the using the bi-sectional algorithm to solve the problem, which will be explain in the coming sections.

Introduction

Semiconductor devices are designed for higher and higher speeds, propelled by the electronics industry's pursuit and the consumer's demands in achieving faster computers that can perform heavier tasks. The metal-oxide-semiconductor field-effect transistor (MOSFET) is a key semiconductor component, the heart and brain in almost all electronic circuits, the evolution of which has stimulated the recent explosion in information and communication technology.

noise is a principal issue in science and engineering, perceived and underlined for an assortment of fields, for example, media transmission, nanoelectronics, and natural frameworks. The noise can't

be totally removed and will consequently at last breaking point the precision of estimations and set a lower limit on how little signals that can be recognized and prepared in an electronic circuit.
The low-frequency noise, or 1/f noise, is the excess noise at low frequencies whose power spectral density (PSD) approximately depends inversely on the frequency and therefore escalates at low frequencies.
The 1/f noise originating from the transistors is a severe obstacle in analog circuits. The 1/f noise is, for example, up converted to undesired phase noise in voltage controlled oscillator (VCO) circuits, which can limit the information capacity of communication systems. Additional, the downscaling of the device dimensions entails a downscaling of the voltage levels too, which lowers the signal-to-noise ratio.

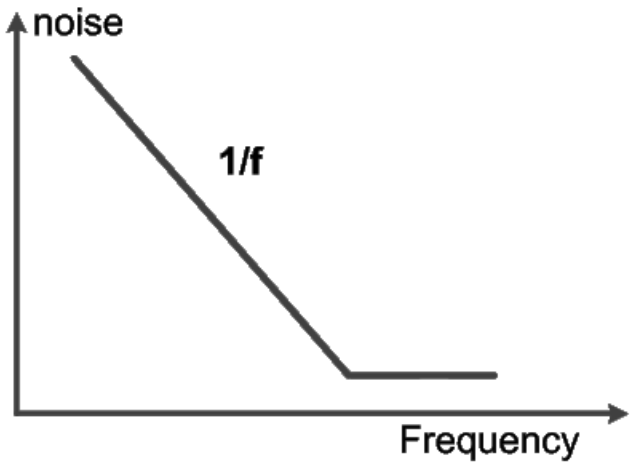


Figure 1.1: Spectrum of low frequency or "1/f " noise versus frequency

There are two theoretical methods of low frequency or 1/f noise:

1) the carrier number fluctuation model
2) the bulk mobility fluctuation model

Surface channel MOSFETs show a large noise at low frequencies, which make the study of 1/f noise very important.

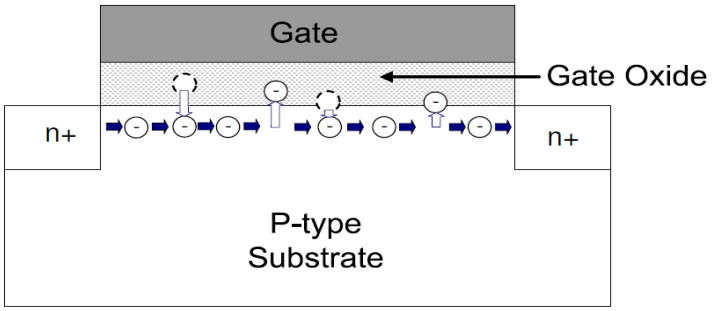


Figure 1.2: Cross-section of the MOSFET depicting the trapping and detrapping of the electroncs in the channel from oxide traps.

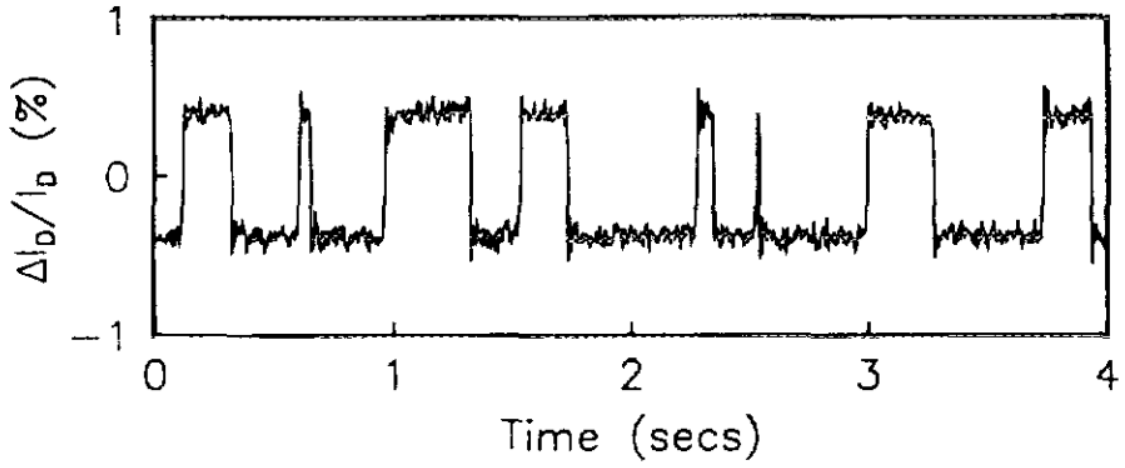


Figure 1.2: Example of random telegraph signal (RTS) noise measured in the drain current of a MOSFET as a function of time

In order to minimize the device 1/f noise, an understanding of the noise mechanisms, the underlying physics and the location of the sources is necessary. Still today, after several decades of debate, the exact origin of the 1/f noise is in many aspects an open question.

The incorporation of high-K dielectrics into MOSFET overcomes the issue of gate leakage current; however, the process gives rise to other issues such as an observed increase in the trap density at the silicon interface.

In constant-field scaling, the device physical dimensions and applied voltages are reduced by a factor of α ($\alpha > 1$) and the substrate doping concentration is increased by α in order to maintain the constant electric field in the device and prevent short-channel effects.

Features of “shrinking”:

1) the focus on scaling through constant improvements in lithography, guided by certain scaling principles
2) the introduction and incorporation of new materials and structures

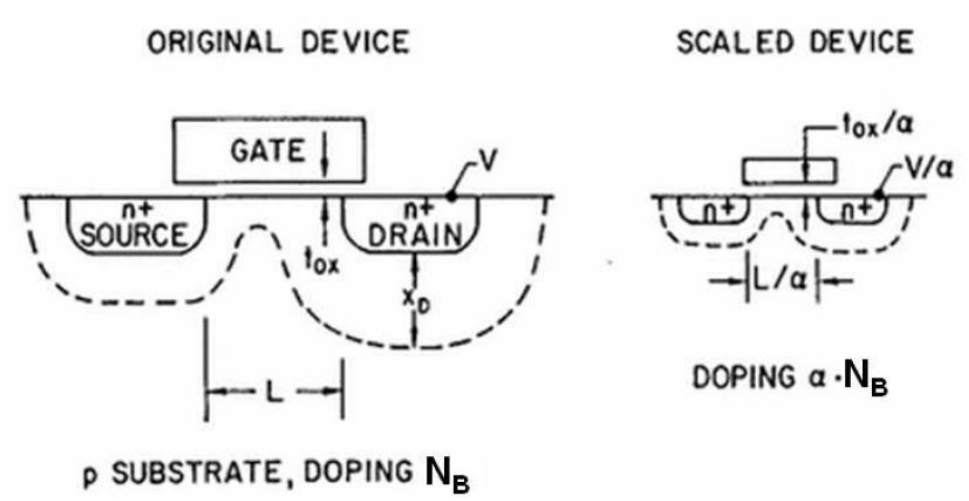
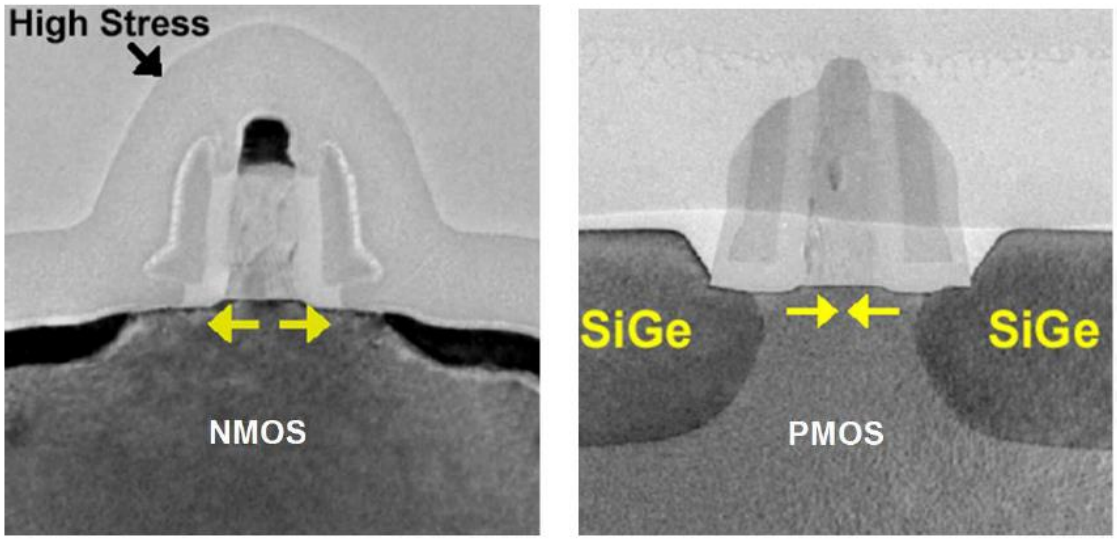


Figure 1.3: Schematic illustration of MOSFET constant electric field scaling

An important benefit of scaling is the increased circuit density which come out with reducing manufacturing costs, the circuit speed is improved by a factor of α and the power dissipation is reduced to $1/\alpha$ together with the constant power density.

There are two motivations to increase MOSFET scaling:

1) to improve the drive current
2) to reduce the short channel effects (SCE)



(a) NMOS: Silicon nitride capping layer creates a tensile stress to enhance electron moblity.

(b) PMOS: SiGe selective heteroepitaxy film creates a compressive stress to enhance hole mobility.

The gate has more control of the channel charge, the off-current path is eliminated between the source and the drain terminal. Therefore, the on/off current ratio can be increased, which means better switching capability.

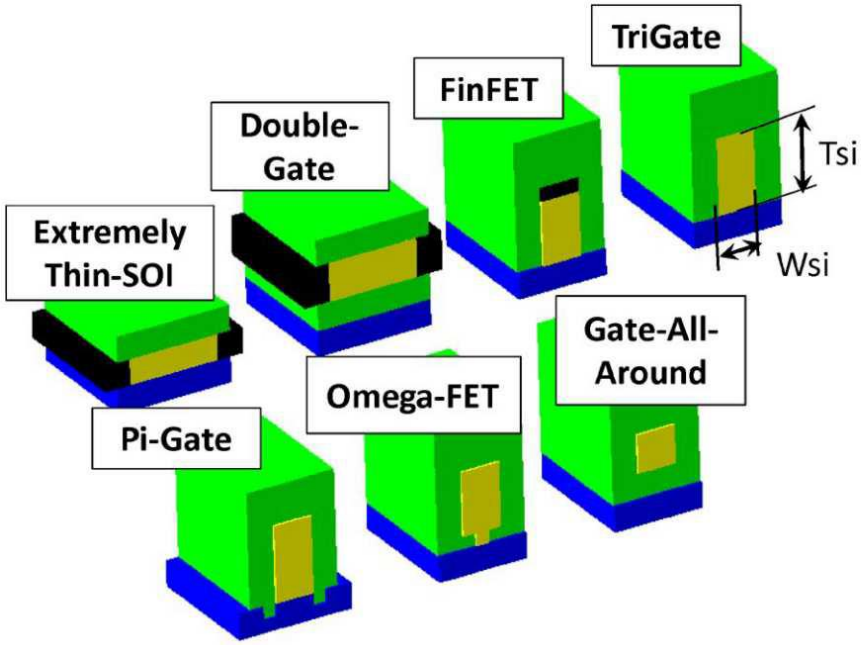


Figure 1.7: SOI and multi-gate architectures which reduce source-drain interaction

As the gate length is scaled down, the gate oxide needs to be thinned in order to control the short channel effects. Unfortunately, the gate tunneling current increases exponentially with decreasing thickness. For oxide thicknesses around 1-1.5 nm, depending on application, the gate leakage current become intolerable high A high gate leakage current causes problems such as increased standby power consumption, deteriorated reliability and lifetime, and can ruin the whole device operation. By replacing the SiO2, which has a dielectric constant k of 3.9, with a material with higher dielectric constant, a so called high-k material, a physically thicker gate dielectric is allowed to achieve the same capacitance.

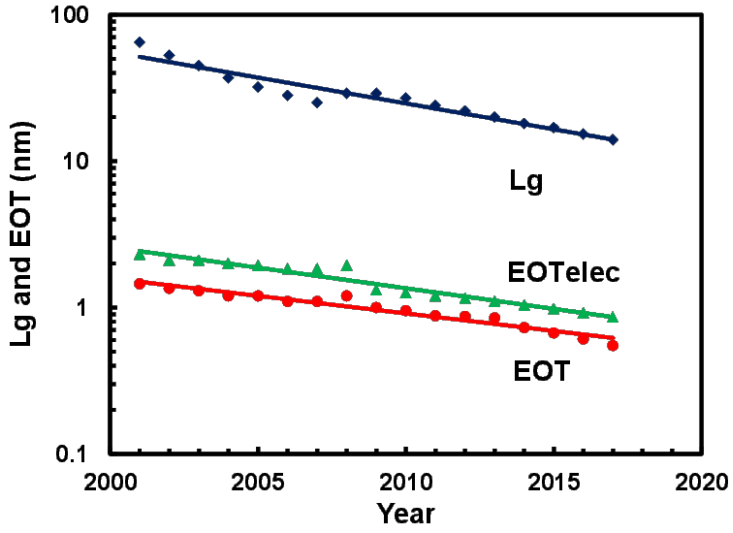


Figure 1.8: Scaling trend of the physical length L and effective oxide thickness (EOT)

One of the reasons for the big success with CMOS technology is that an excellent insulator, SiO2, has been available. To replace the silicon dioxide is therefore an enormous challenge. The high-k materials that are to replace the SiO2 must satisfy various requirements.

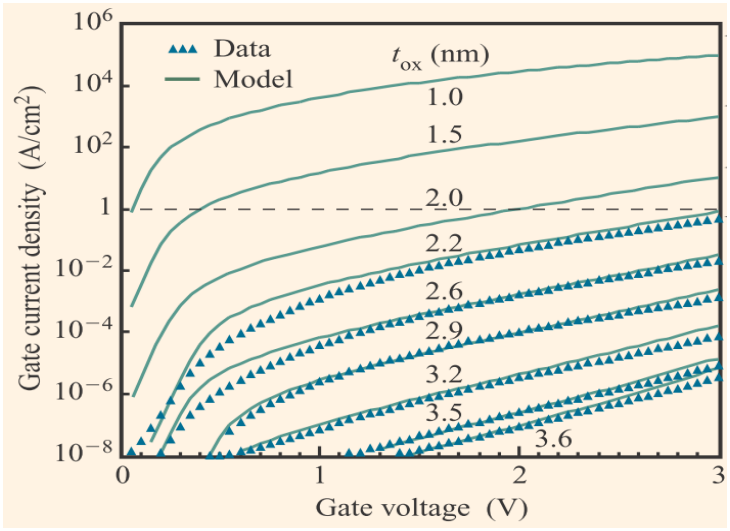


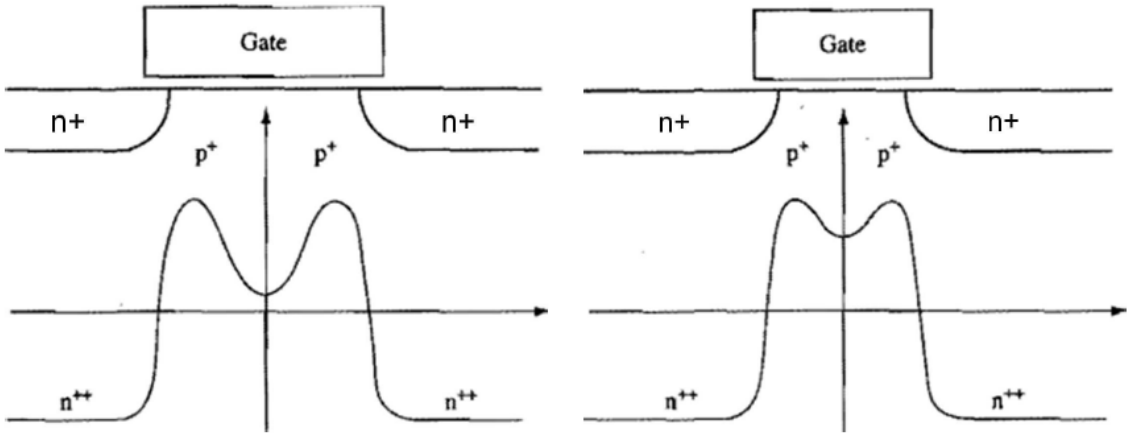
Figure 1.9: Measured and calculated oxide tunneling currents vs. gate voltage for different oxide thickness

When the oxide thickness goes to nanometer level, it is not easy to guarantee the oxide quality any longer. The solution to this dilemma was to increase the physical thickness of the gate insulator to inhibit the direct tunneling, yet as the same time decrease the electric thickness of the gate insulator. This was possible through the introduction of new gate insulators with higher relative dielectric constants. These insulators became known as high-K dielectrics. Compared to SiO2, high-K gate dielectrics exhibit a substantial flatband voltage shift due to positive fixed charges in the high-K film with associated charge trapping.

In modern MOS technology, the doping profile designing is focused on two aspects:

1) alleviating the short-channel effects
2) the threshold voltage adjustment implants.

The former is achieved by halo doping region and ultra-shallow junction, the latter is achieved by multi-step implants at different energy and dose and annealing steps which are carefully designed.



(a) Long Channel (b) Short Channel

Figure 1.10: Laterally nonuniform halo doping in nMOSFETs

For nanoscaled MOSFETs, to reduce the threshold voltage without significantly increasing the gate depletion width, the vertical doping profile is desired to be a low-high doping.

Methodology

In this dissertation, they interested in better understanding of 1/f mechanisms in scaled MOS transistors, both experimental and theoretical work. With surface roughness (β) taken into account, we extend the Unified Model to provide an understanding of the 1/f noise in scaled MOSFET devices with ultra-thin gate dielectrics.

They have also developed a theoretical treatment for the remote Coulomb scattering (α), which focuses on traps in the dielectrics and includes the charge centroid and the finite extension of the charge centroid into the silicon. The 1/f noise in scaled CMOS devices may be interpreted in terms of the remote Coulomb scattering (α) and the surface roughness scattering (β = q θ S/ μ 0Ceff), in addition to the number fluctuations.

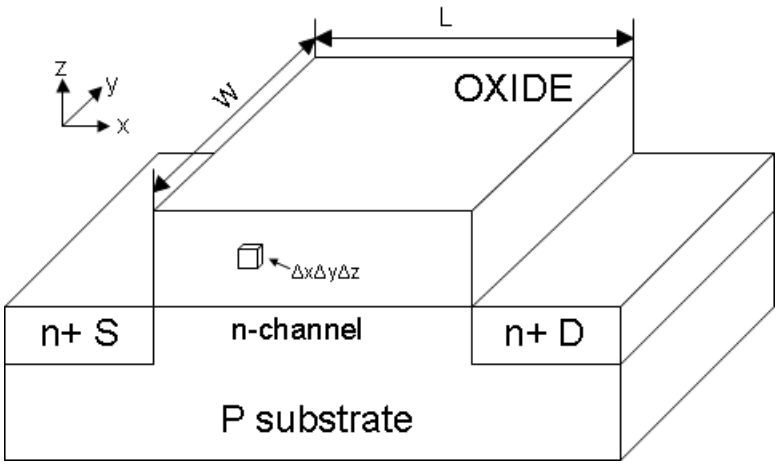


Figure 2.1: MOSFET structure showing the infinitesimal segment _x of the channel

The band bending at a semiconductor surface can be characterized by an electrostatic potential ϕ(z). Under the assumption that planar dimensions of the MOS transistor are much greater than the depth of the semiconductor potential well

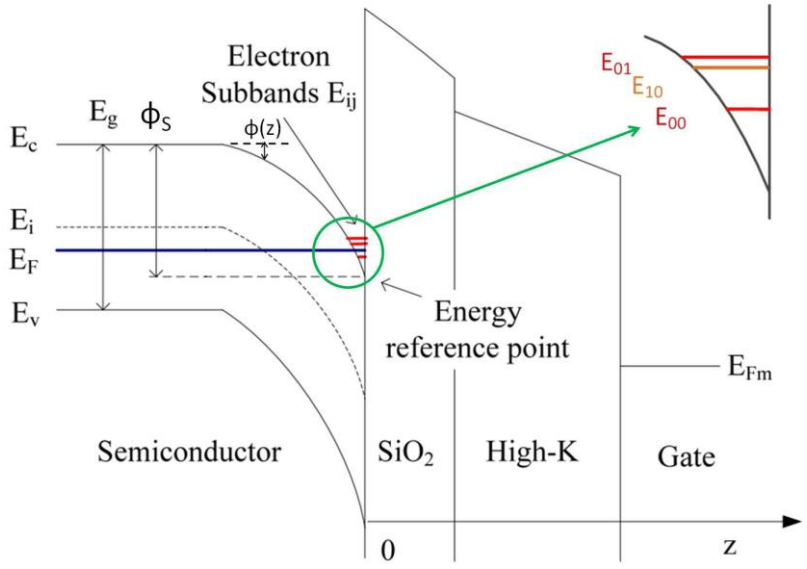


Figure 2.2: Energy band diagram for SiO_2/High-K structure at strong inversion

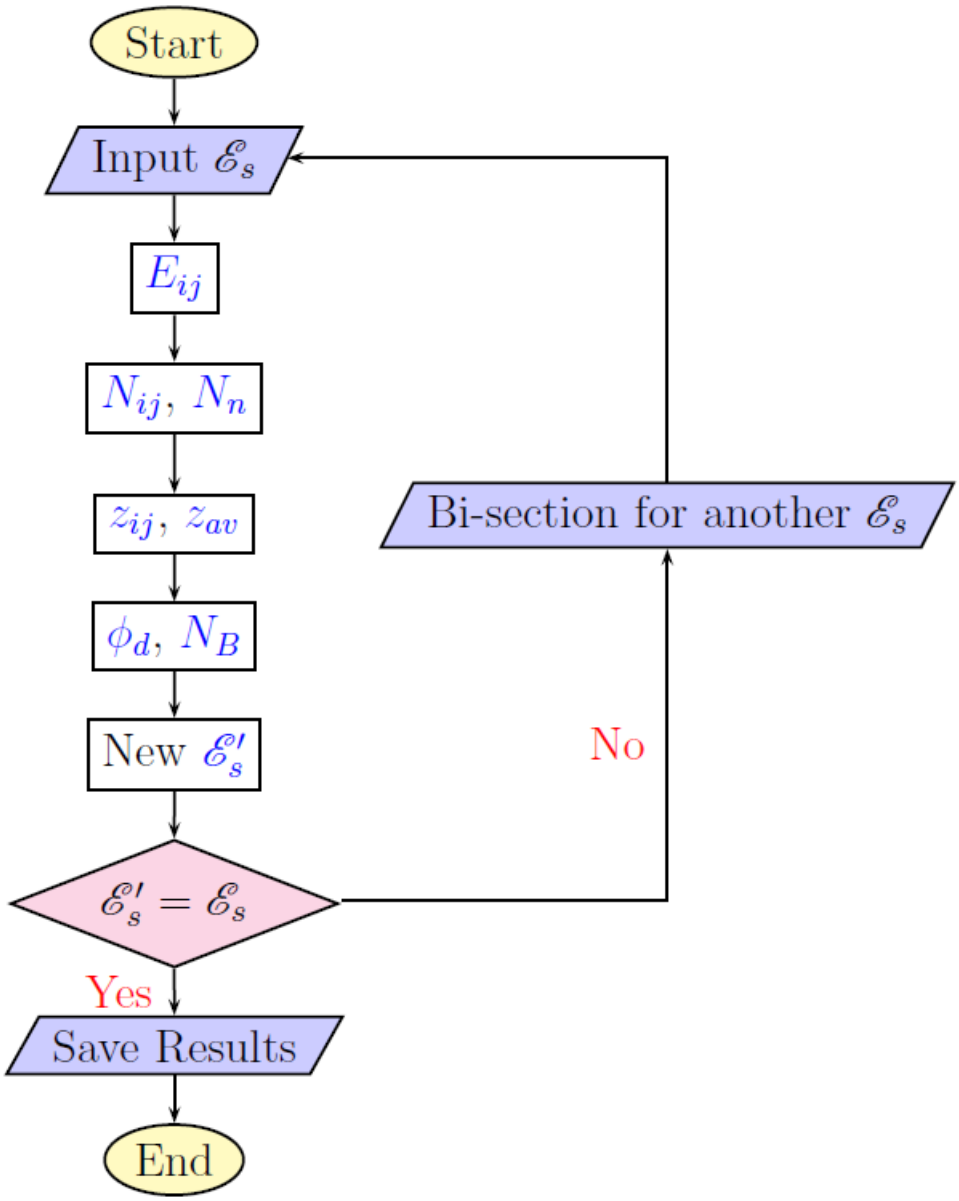


Figure 2.3: Triangular well code flow chart.

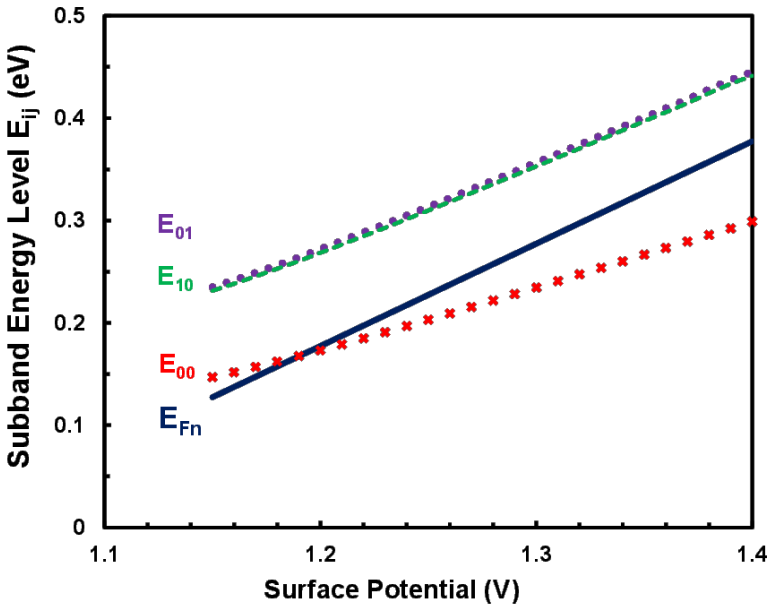


Figure 2.4: The first three quantized energy levels (E_{00}, E_{10} and E_{01}) and quasi-Fermi level E_{Fn} versus surface potential. E_{Fn} surpasses E_{00} at surface potential of around 1.2 V.

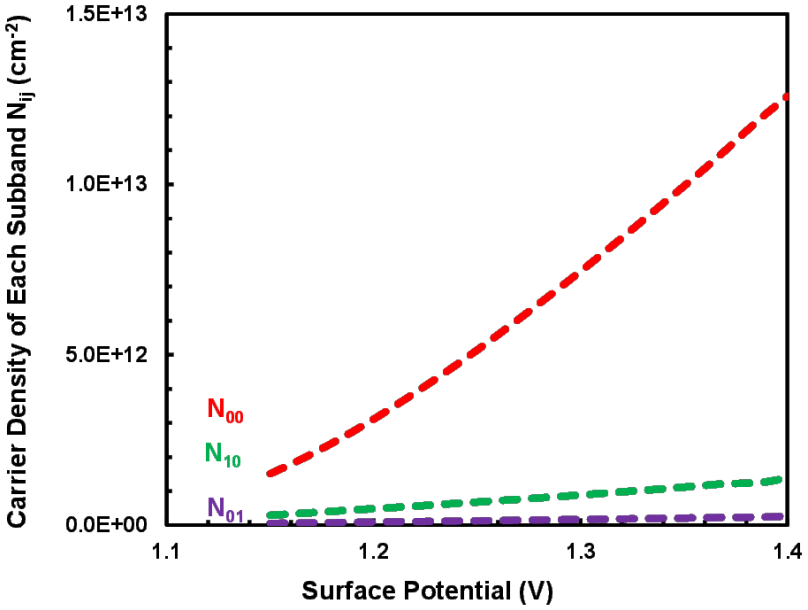


Figure 2.5: Inversion layer carrier density versus surface potential. Most of the carriers are located in the lowest subband E_{00}. As the surface potential get larger, the surface become more “inverted”.

In the simulation performed in this work, exponential distribution is chosen because it is shown to be a better fit to experimental findings.The following expression for the surface roughness mobility

$$\frac{1}{\mu_{sr}} = \frac{9\Delta^2 q m_t^{1/2} \mathscr{E}_{SH}^2}{2^{1/2} L_c (k_B T)^{3/2}} f(u_{kin}, Q_B, Q_n)$$

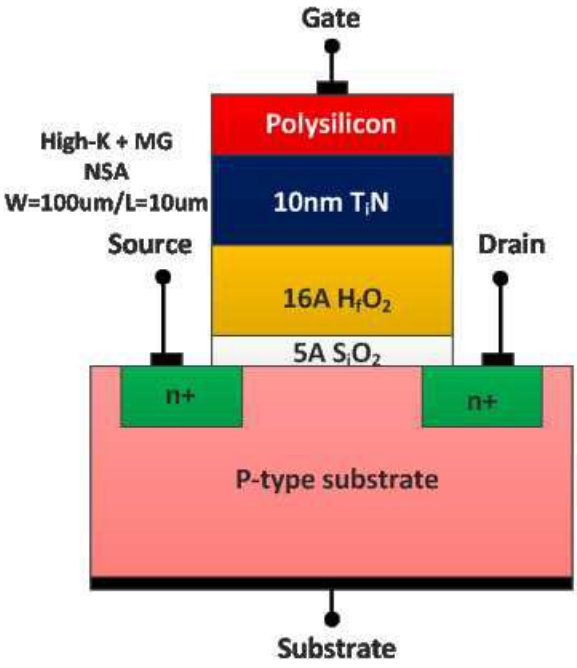


Figure 2.8: Cross-section of the scaled NMOS transistors with 0.5 nm SiO_2/1.6 nm HfO_2 gate dielectric and 10 nm TiN gate electrodes (non-self-aligned, W = 100 um, L = 10 um).

Experiments

Electrical measurements of modeling parameters from DC device modeling permits the extraction of α and β to correlated with noise measurements.

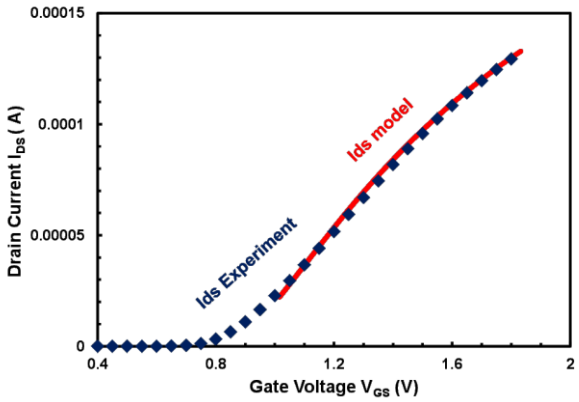


Figure 2.9: Comparison of the simulated and experimental I_{DS} versus V_{GS} curve. The solid line represents simulation results, while the diamond symbols represent experimental results.

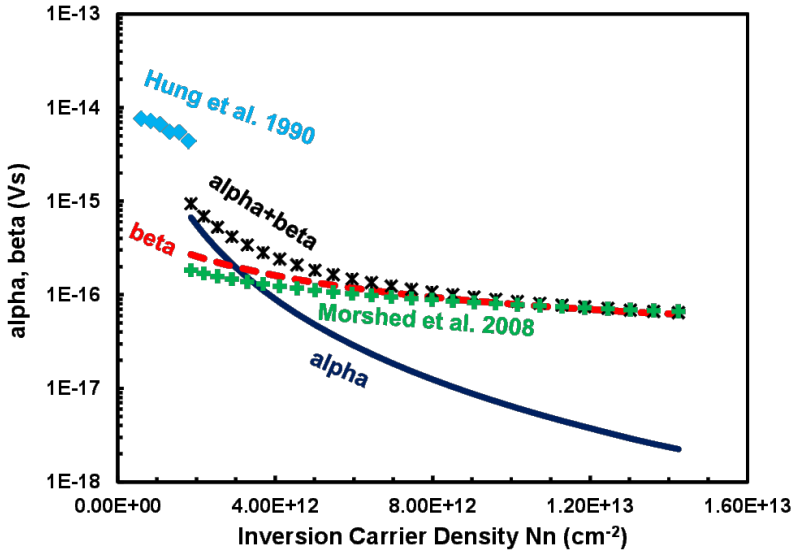


Figure 2.10: Modeled variation of α and β versus carrier density. The solid line represents α, while the dashed line represents β. The star symbols represent the sum of α and β. The diamond symbols represent the extracted scattering parameter, while the plus symbols represent the extracted scattering parameter for comparison with (α + β).

Since the gate oxide was much thicker back then and the carrier density is much lower than our device today, the reported value is expected to be higher than that in our device, which is the case shown in Figure 2.10. have extracted the «screened scattering coefficient», expressed as. −1 with µco as fitting parameters, from 1/f noise measurement on poly-HfSiON-SiON-Si MOSFETs with thin gate dielectrics. Note again that this so-called «screened scattering coefficient» is equivalent to the sum of and β in our model.

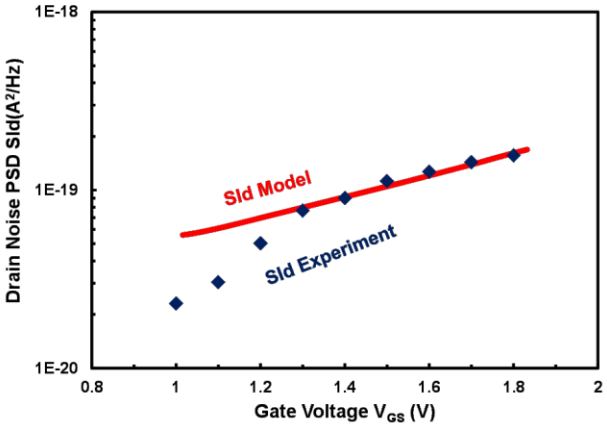


Figure 2.11: Drain current noise PSD versus gate voltage for high-K, NMOS device at V_{DS} = 50 mV (W = 100 um, L = 10 um), f = 4 Hz. The analytical expression for S_{Id} is given for low V_{DS} as well as the expression for mobility, which involves remote Coulomb scattering (α) and surface roughness β.

the experiment starts from VGS = 1.0 V, which ensures the surface is inverted. Meanwhile the applied gate voltage is kept below 1.8 V, so that the electric field in the ultra-thin dielectric will not be so large as to be near the breakdown region. The model shows good agreement with the experiments over higher VGS range and slightly overestimates the result at low VGS. This is due to the assumption to locate all the carriers in E00 when modeling the scattering parameters, similar to the description in previous: at higher VGS and Nn, more electrons are located in the lowest sub-band, which indicates that our model processes more accurate as the quasi Fermi level is moving up. Select the right SMU assignment in the LabVIEWç program, and set up the biasing conditions.

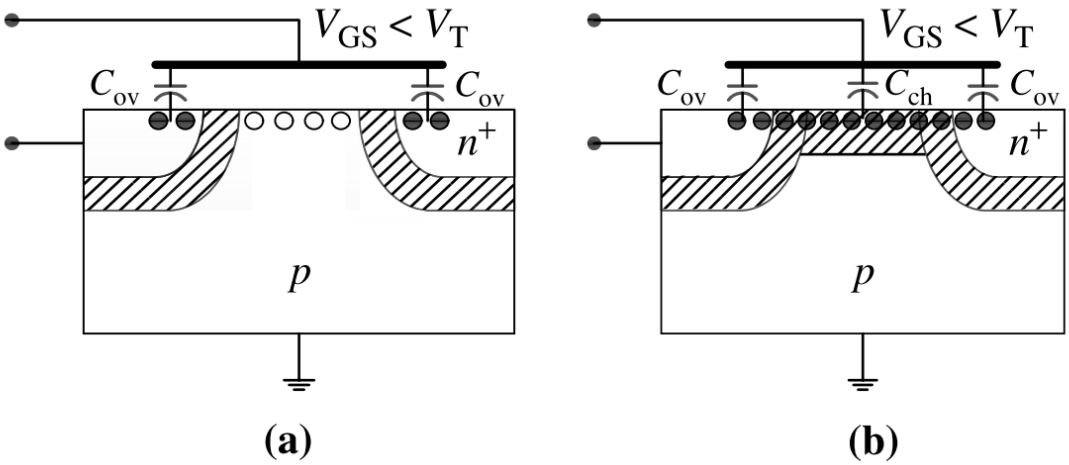


Figure 3.2: Schematic for gate-to-channel capacitance measurement

- Start measuring and save the data.

Measurement Setup The front panel for this measurement allows the user to specify the corresponding SMU for each terminal. Item B.2.1 lists the required inputs for making the measurement.

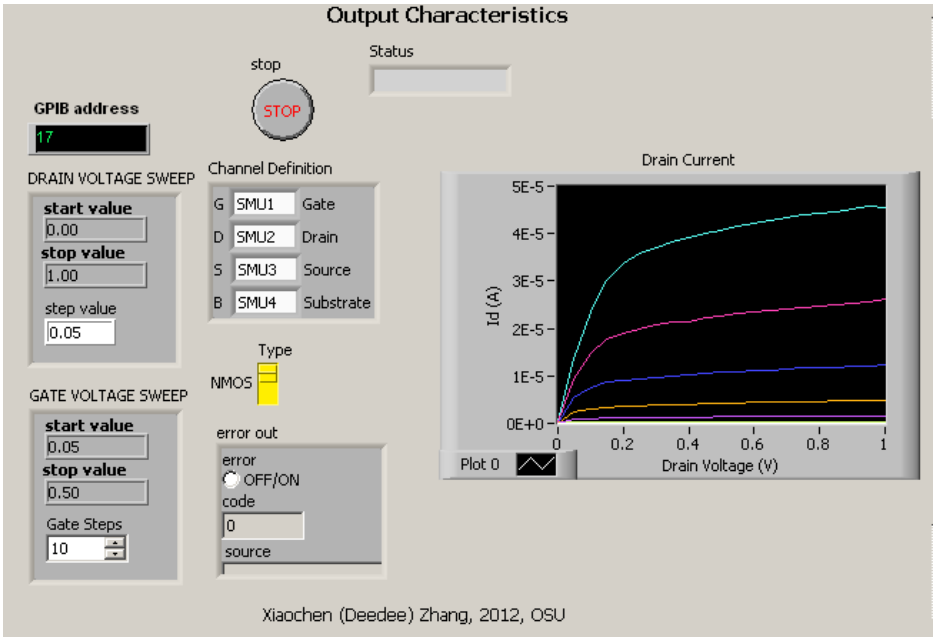


Figure B.4: The I_{DS}-V_{DS} characterization front panel for LabVIEW. Drain sweeps are made for a range gate biases. The displayed plot is an example of the output characteristics of a MOSFET device.

- The procedure is similar to the base sweep configuration as described previously.

  Measurement Setup The setup for parameters is listed in Figure B.4.1. Note that when varying base, one must follow the restrictions for the amplitude and offset values of the pulse generator, in this case, Agilent 33120A in which the absolute value of the offset voltage (middle point of the base and the peak) should be less than 2 times of the peak-to-peak amplitude (in our case, the amplitude specification itself).

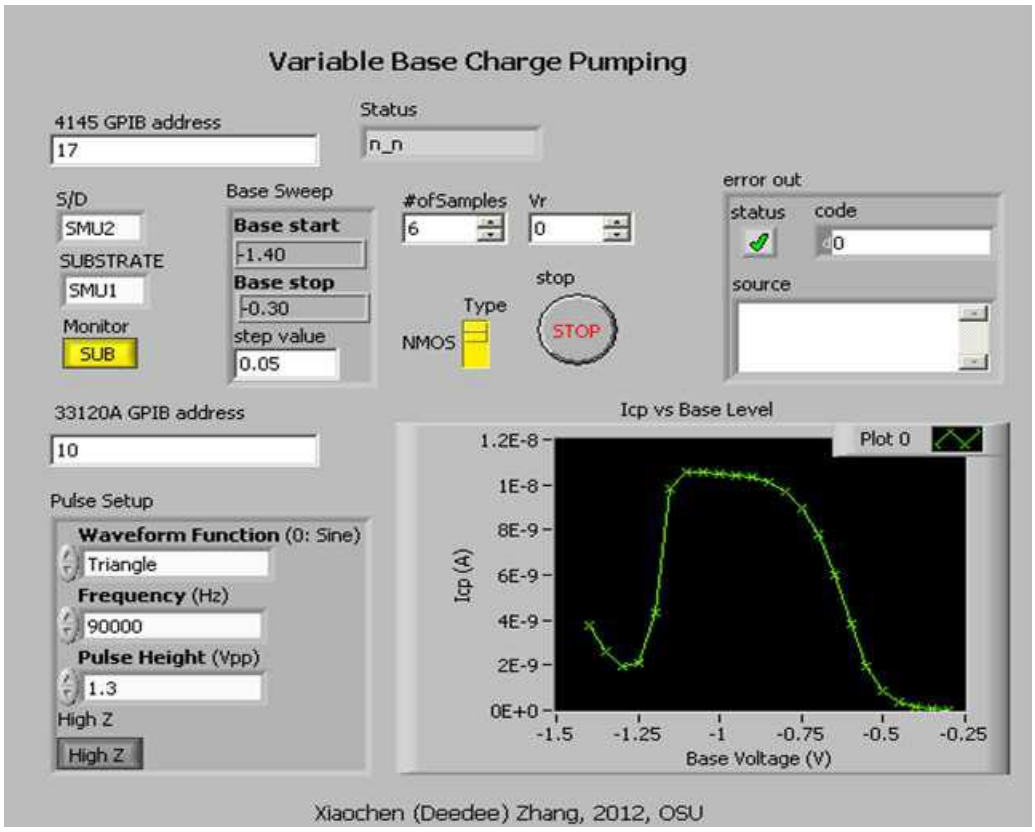


Figure B.10: The variable base charge pumping characterization front panel for Lab-VIEW. The trace shows the measured charge pumping current versus the base level of the applied waveform.

S/D SUBSTRATE Amp Sweep Fixed Base # of Samples Monitor Waveform Function Frequency High Z Vr

SMU connected to S/D SMU connected to bulk applied amplitude levels base level number of samples taken where the current is measured waveform shape waveform frequency output condition reversed bias on S/D select accordingly select accordingly

0.6 2 smaller than VF B

Table B.4: Front panel control definitions for the CPamp program.

Data Output Data is saved in ASCII to a file specified by the user upon completion of the measurement. The file contains a header and two column data. The header gives the measurement type and selected conditions. Data column one is the pulse amplitude and column two is the measured charge pumping current.

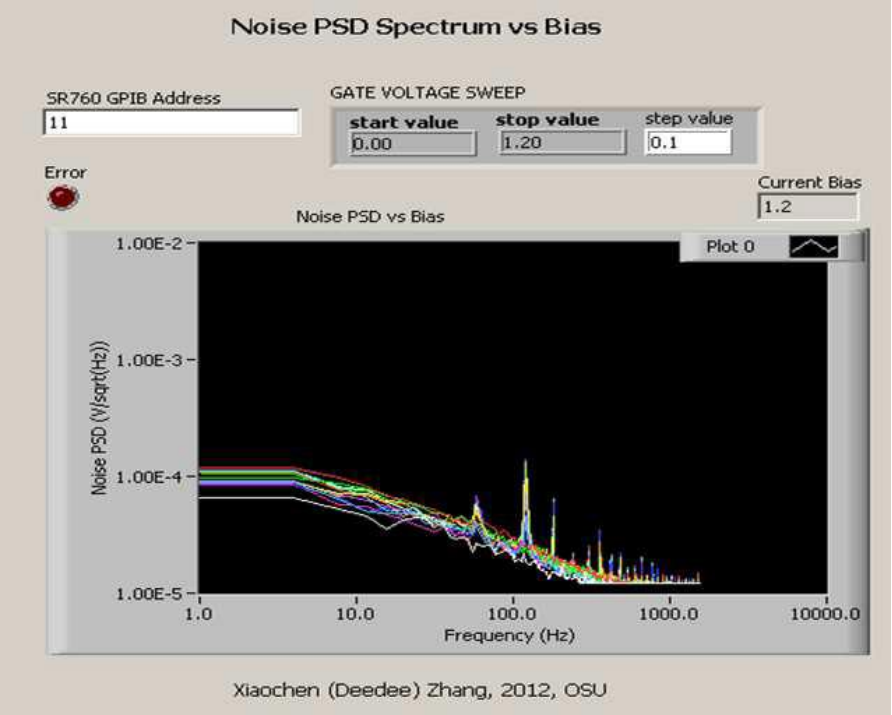


Figure B.11: The noise PSD spectrum versus bias front panel for LAbVIEW.

Results and Discussion

The net performance enhancement in channel carbon implanted NMOS devices can be explained by a lower concentration of active boron in the channel region. This improvement can be attributed to the combination of retarding effects on the boron diffusion and the deactivation of boron by Cii. It is very interesting to see that the PMOS performance is improved at the same time, which might be attributed to the action of the implanted carbon to block the source-drain, lateral boron diffusion under the gate electrode combined with a suppression of short-channel effects (SCE). We did observe an increased junction current (10 times) in the Cii samples, in agreement with [44]. However, we believe by carefully designing the implantation conditions, we could further optimized the doping profile and minimize this current.

In addition to the fabrication process described in Section 4.2, comparison splits have been made for which the Cii in introduced after the dummy interfacial oxide growth. In this case, there is no significant performance improvement for either the NMOS or PMOS devices. As consequent of these experiments, we believe most of the boron diffusion takes place in the dummy IL oxide

growth, which is done, as mentioned previously, with a thermal process. Thus, the dummy interfacial layer growth step should be performed after the Cii. In addition, this thermal process also helps to move the carbon into substitutional sites, which enhances the suppression of boron diffusion.

The modeled remote Coulomb scattering parameter and the surface roughness scattering parameter (β) show good agreement with the observed experimental values. Simulations, based on theoretical modeling, show good agreement with experimental data obtained from a high-K NMOS device with ultra-thin oxide, for both DC I-V transfer and noise characteristics. In this work, they found that the β value exceeds α at high inversion levels, therefore it is necessary to take into account the fluctuation in mobility induced by the variation in the normal electric field.
As the devices scaled further, the surface roughness scattering parameter (β) will become more important in the 1/f noise due to the increased normal field. The proposed model can be extended to other material systems such as III-V devices, given that the appropriate energy levels for carriers and parameters for the materials are utilized.
Several experimental setups, involving automatic data acquisition, have been built with the help of computer programming, which greatly enhances the functionality of the setups. With these setups we have evaluated device performance and certain physical parameters of both NMOS and PMOS SiON MOSFET devices.
For these devices, the gate leakage current does not have strong impact on the CV characteristics.
The equivalent oxide thickness (EOT) is obtained from a 1 MHz CV measurement as 2.4 nm (NMOS) and 2.6 nm (PMOS) at inversion, which is slightly larger than the physical thickness of the SiON layer due to poly-gate depletion and the charge centroid of carriers in the inversion layer. The substrate doping densities, extracted from transfer characteristics under different body bias conditions, are 3.8E17 cm−3 for NMOS and 2.0E17 cm−3 for PMOS. The effective mobility values, obtained by split-CV technique, are extracted to be 198 cm2/V-s for electron in NMOS and 70 cm2/V-s for hole in PMOS at around 0.5 V gate overdrive. With the exclusion of series resistance and surface roughness scattering, the mobility containing only bulk mobility and remote Coulomb scattering is 345 cm2/V-s and 144 cm2/V-s for N and P samples. This indicates, for these high quality SiON devices, the surface roughness imposes a great impact on the carrier mobility.
Variable frequency charge pumping measurement with a triangular waveform has been performed on both N and P SiON MOSFET, to study and compare the interface quality of these samples. After the gate current correction, the measured interface trap densities are 9.7E10 cm−2eV−1 and 5.8E10 cm−2eV−1 respectively in NMOS and PMOS samples. The geometric mean of the electron and hole capture cross section is also extracted to be 3.3E-17 cm2 and 9.1E-17 cm2 receptively for N and P devices.
The extracted results indicate an excellent interface quality between the SiON layer and the silicon substrate. Since the nitride concentration is not high, the interface quality is comparable with devices with pure SiO2 gate dielectrics.
Carbon ion-implantation (Cii) into CMOS device channels improves NMOS high-K, metal gate, device performance for replacement-gate, low power, technology. NMOS samples with Cii demonstrate a desirable decrease (-0.1 V) in Vt and improved electron mobility (10%) as compared with control samples without the Cii. This improvement has been attributed to the retarding effects of boron diffusion as well as deactivation of boron caused by the carbon, which results in a better-controlled retrograde boron channel profile and a lower active boron

concentration in the inversion region. Considering the overall benefits, channel Cii is good for controlling the vertical
doping profile.

Future work

The present models have some fail in several instances; either the modeling parameters have been physically incorrect or the models have not been able to satisfactorily predict the noise behavior. The 1/f noise performance is sensitive to the choice of gate dielectric material. Devices using gate dielectrics with a high dielectric constant (high-k) can exhibit up to three orders of magnitude higher 1/f noise than those with thermally grown SiO2.

In this dissertation some future works are recommended such as:

- The 1/f noise performance is sensitive to the choice of gate dielectric material. Devices using gate dielectrics with a high dielectric constant (high-k) can exhibit up to three orders of magnitude higher 1/f noise than those with thermally grown SiO2.
- For further enhancement of device speed, continued downscaling of the device dimensions is necessary including the use of high-k gate dielectrics.
- Improve a model for mobility fluctuations noise.
- Study the random telegraph signal (RTS) noise of MOSFET devices, then compare with 1/f noise.
- Develop quantum mechanical treatment of 1/f noise in PMOS devices.
- we can Incorporate temperature capability in the current setup, and study the temperature
  dependent behavior of 1/f noise in nanoscaled MOSFET devices.
- Extend the 1/f noise mechanisms and behavior in a single transistor to circuit and systems, and explore the noise benchmark methodology in modern VLSI systems.