MULTIMEDIA UNIVERSITY®

FACULTY OF ENGINEERING

PROJECT PROPOSAL

VETS 7016-1: Industrial Project Planning & Implementation

Project Title:
Failure Analysis and Yield Improvement Methodology on Structural Based Functional Test [SBFT] Design

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Program: Micro-credentials in M.Eng. Microelectronics

Declaration of originality:

I declare that all sentences, results, and data included in this report are from my own work. All work derived from other authors have been listed in the references. I understand that failure to do this is considered plagiarism and will be penalized.

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Signature: _____

Date: _____

Abstract

Yield is a key performance to measure in semiconductor manufacturing and has a dominant effect on semiconductor industry. In the dynamic landscape of semiconductor testing, the Structural Based Functional Test [SBFT] design represents a critical component in ensuring the reliability and functionality of integrated circuits. This project endeavors to conduct a cases study in-depth investigation into the causes of failure analysis within the SBFT framework and proposed a technical comprehensive Yield Improvement Methodology. The research will deploy advanced failure analysis techniques to scrutinize the intricacies of SBFT design failures, aiming to pinpoint root causes and vulnerabilities. In this industry project proposed plan, a systematic methodology of wait time optimization will be developed in SBFT design to enhance the yield of the testing process. This methodology will encompass innovative strategies for mitigating common failure modes, optimizing test parameters, and improving overall test efficiency. The outcomes are expected to contribute not only to the advancement of testing methodologies but also to the overall quality and reliability of semiconductor devices. As the semiconductor industry continues to evolve, the insights derived from this research have the potential to significantly impact the field of SBFT, contributing to advancements in semiconductor testing and electrical quality assurance towards Yield enhancement.

1.0 Introduction

SBFT can be defined as “Structural Based Functional Test”. It is involving functional tests on a chip outside of a system by loading data and content pattern string into a cache internally to run useful code. Functional test is an important part of the overall testing methodology of a modern SOC (System-On-Chip), which usually consist one of more CPUs, large and several memory structures, and many logic interfaces like for example Finite State Machine (FSM), Instruction Register (IR), Instruction Decode Logic (IDL), Data Register (DR) and Test Data Output Multiplexer [TDO MUX] which involve Scan Test. Furthermore, SBFT is functional testing where the results output will be executed through chips pin. Once the test is completed, we can read the core string and iteration results of the chips with performing analysis of shmoo plot that run on automated test equipment (ATE) known as High Density Modular Test (HDMT) tools.

1.1 Problem Statement(s)

There are many reasons why SBFT design cannot be avoided even in a full-scan design to achieve high quality levels of chips architecture. The main benefits of SBFT Design are the ability to test the chip at the "Silicon Wafer Sorting" stage which is before the chips is packaging in manufacturing. This upfront testing SBFT analysis helps to identify the defective chips before they are packaged, ultimately help saving costs for the semiconductor manufacturing industry example like Intel, AMD, Lattice etc.

- SBFT design serve as a complementary test suite to stuck-at tests also the pattern content known as "ca1tf" by significantly increasing defect coverage since not all defects can be modeled well by the stuck-at fault model.
- The activity caused inside a chip by SBFT design is proximity to the conditions that will be observed in its system operation which can results in localized VDD drops and certain crosstalk conditions, which, in turn can stress pattern content propagations paths more than scan-based at-speed tests. Functional test can be particularly useful for speed testing.
- The SOC architecture of logic usually untestable during scan-testing mode to satisfy certain design rules for ATPG [Automatic Test Pattern Generation] tools. These blocks of logic can be exercised by functional test. And finally, some custom CPU design may still not be full scan, which makes that SBFT design architecture is an essential part of their testing methodology.

1.2 Project Objectives

- To conduct the first cut standard high level of failure analysis debugging steps in SBFT design flow towards Yield enhancement.
- To perform and implement the experiment on the duty cycle optimization for the SBFT Chipsets pattern modification which can help on the test time reduction in SBFT content. The SBFT design verification test and outcome of the shmoo plot comparison before and after the propose technical fix plan can be demonstrated by using the Automated Test Equipment (ATE).
- The final objective is to analysis the Yield data percentage graph comparison between Initial and after the implement of the Methodology based on the second objectives achievement.

1.3 Project Scope

In this industry projects, the main scope we going to target performing the high level of debugging and validation methodology for SBFT design and propose some experiment the implementation technical fix plan on the test module and pattern content inside the chips architecture.

- Based on the defective chips to understand the Root Cause failure with 1st cut analysis of SBFT data which is causing by design flow, environment factors, electrical stresses, or manufacturing defects.
- We going to collect the shmoo graphical plot to visualize the performance of the integrated circuit under various combination of input timing and voltage. Thirdly, based on the behavior of shmoo plot we can understand the acceptable operating range for integrated circuit to meet the correct timing margin and vmin testpoint to achieve the passing range.
- To propose some technical experiment for example with change the pattern ordering, wait time modification and voltage incrementation setup to have the disposition plan to the defective chipsets.

Hence, all the simulation experiment will be carried out in the Automated Test Equipment (ATE) and in final objectives we going to use the JMP and Excel Software to perform the line and bar chart on comparison the Yield percentage after the experiment being implemented. This industry project proposes fix plan experiment had been carried out and it able to help disposition for the weekly monitoring defective chips towards save cost in manufacturing semiconductor industry.

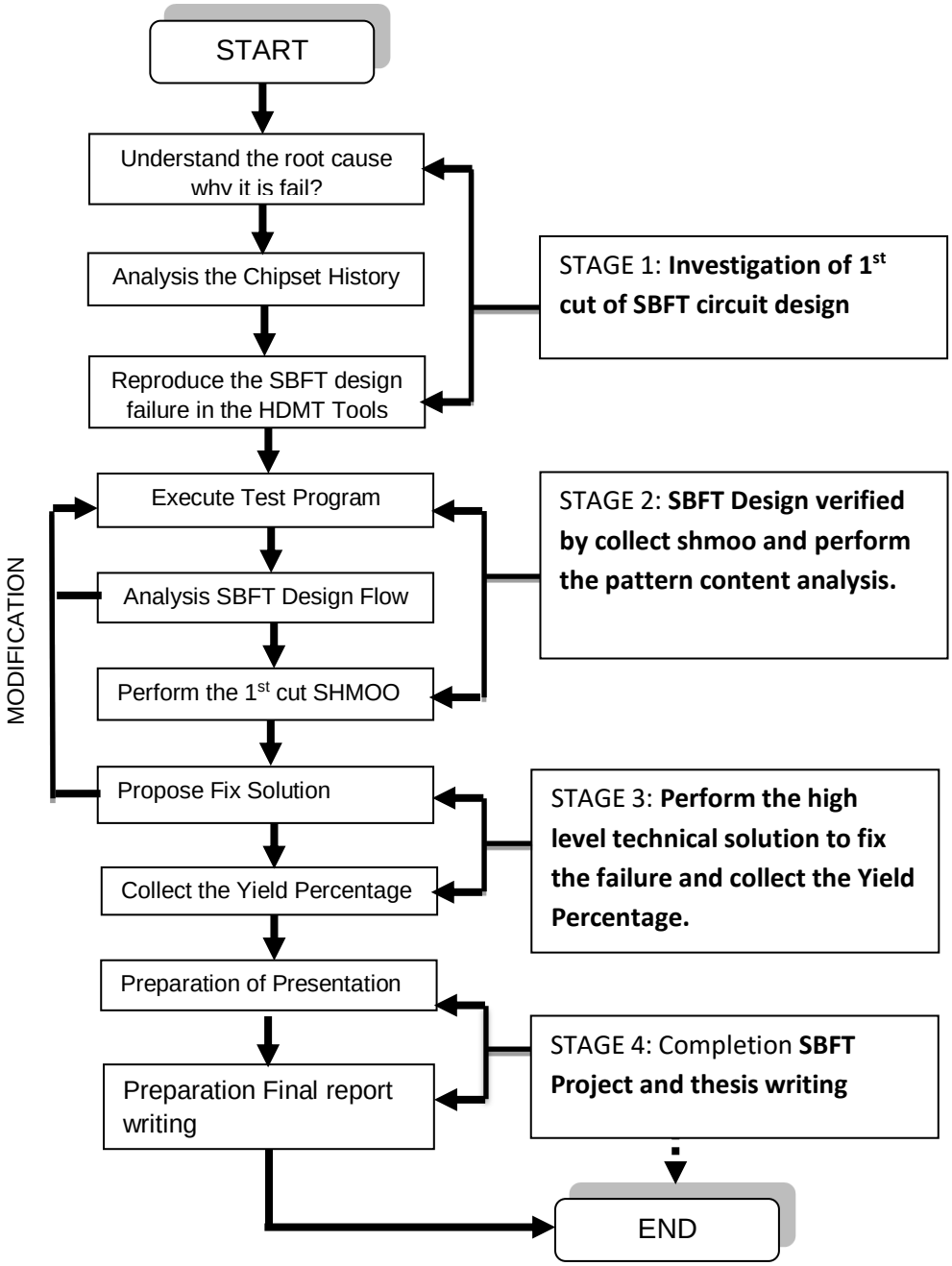


Fig. 2 Design of Flow Diagram

2.0 Literature Review

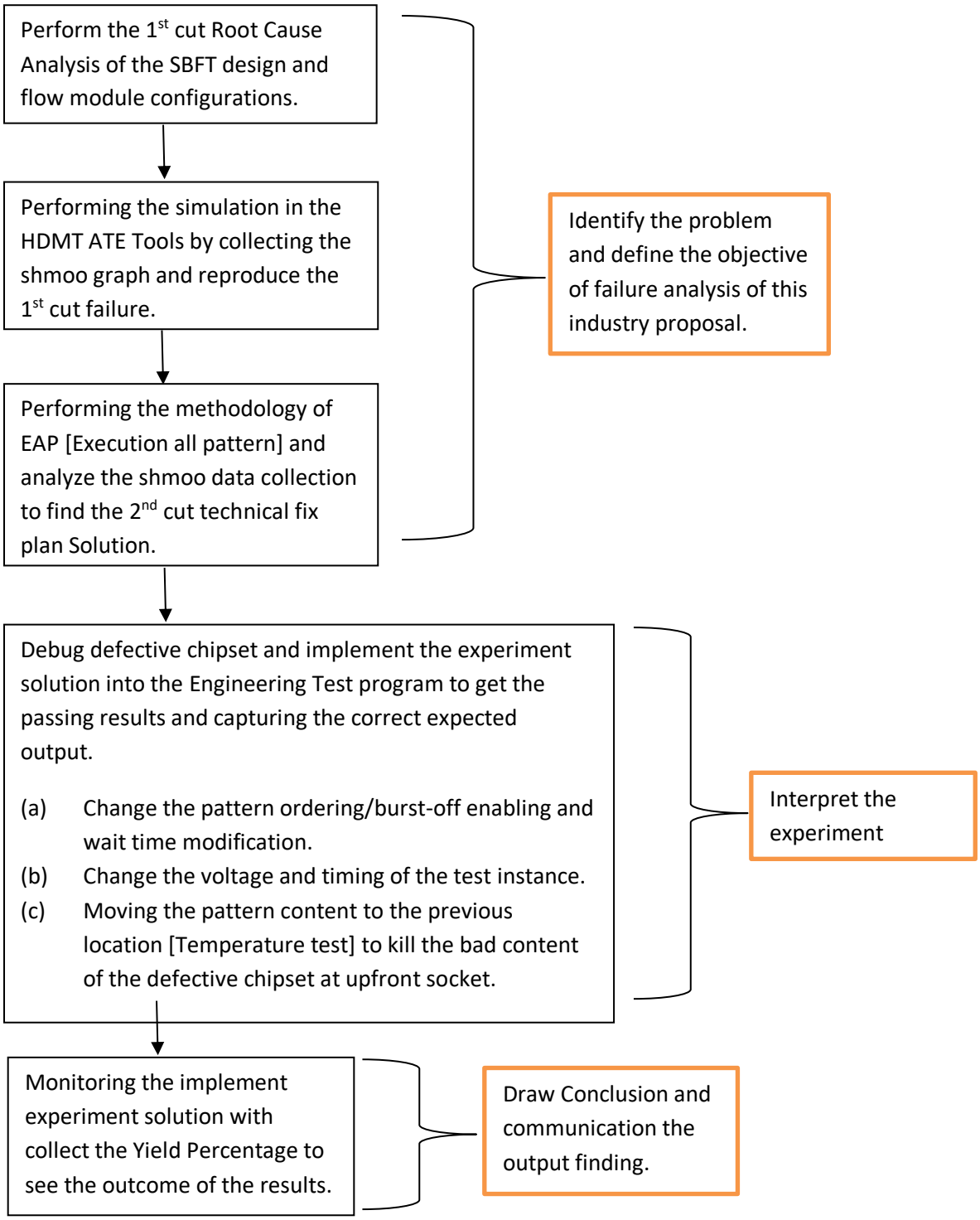
Based on my industry proposal, Failure Analysis and Yield Improvement Methodology of SBFT design being discussed. These literature review below are the citing and references which relate to my project title. There will be more studies of journal and paper may need to further review in order to understand further the improvement we can be implementing into future work.

Reference Number	Journal Title and Year	Method	Advantage	Disadvantage	Improvement needed to perform
1.	DFFT design for functional stability, 2004	Propose the new design of RTL mechanisms for functional test for example like clock domain crossing and adding new chip pins design inside the reset content help to indicate pass on the ATE.	Improve the speed and frequency of the RTL design towards increase the memory with RAM which help smooth debugging process during the transition to an ATE.	More RTL and flip-flops being added into the functional design will cause miss-match communication of the Chip pins architecture.	Split out the rising clock/reset edges into two clock domains in parallel to achieve the stabilize asynchronous interface of processors.
2.	Realizing the Benefits of Structural Test for Intel Microprocessor, 2002	Design a narrow bus logic to detect a timing glitch and speed path	Reduce the test costs and increase the device complexity.	Required high temperature of voltage to stress the scan-based logic test	Enabled the single structural socket test towards optimize tester capability and pattern content distribution.

3.	Automated Shmoo Data Analysis: A Machine Learning Approach, 2014	A Machine Learning AI method being proposed to shmoo for HVM test content development	More accuracy to discover VMIN and smoother to detect new issue quicker	Very high cost to labeling the process of Vector Machine and Neural Networks	We can tune the algorithm to utilize the data from neighboring test points with implement more accurate of frequency and bus ratio
4.	Yield Improvement Methodology with addressing Design Systematics during Production Ramp-up, 2022	Design features Extraction based on technology pinch point, NPI Characterization signals & WPs from historic learning	All the layout analysis and pattern are matching was performed very detailing inline margins	Pinpoint diagnosis of the chip weak due to complicated design	Can proposed more systematic Metal Void design to achieve more Yield percentage
5.	Scan based testing: the only practical solution for testing ASIC/consumer products, 2002	Apply SBFT combination with Scan ATPG test to enlarge the stability of the Chipsets architecture.	High coverage for the all-digital embedded system	Take longer time to debug the test development which may cause the chip testing cost increase before release to customer.	Reduce the number of IO pins and implement in the more stabilize pattern content

3.0 Proposed Methodology and/or Materials

Below summary of flowchart will be the overall methodology of the industry of my project. The project task involved the SBFT design analysis and simulation of the SBFT design will be carried out in the ATE tools. The simulation works are emphasizing on obtaining the experiment being listed and review the outcome of the Yield percentage going to achieve the minimum passing score 80% of the SBFT design performance.



3.1 Gantt Chart

Attach table schedule plan below are the 5 months duration of preparation the industry project.

Activity	Start Date	End Data	Duration (Days)
Propose the Industry Project Title	4/11/2023	28/11/2023	24
Assigned of Project Supervisor	28/11/2023	13/12/2023	15
Literature Review	13/12/2023	5/1/2024	23
Industry Proposal Softcopy Submission	5/1/2024	21/1/2024	16
Experiment & Design Flow with Simulation	21/1/2024	11/2/2024	21
Data collection of the experiment	11/2/2024	17/3/2024	35
Data Analysis of the Experiment	17/3/2024	31/3/2024	14
Draft Report softcopy submission	31/3/2024	24/4/2024	24
Project Presentation Physical	24/4/2024	27/4/2024	3
Final Report & Conclusion	27/4/2024	10/5/2024	13

The Estimation of the Gantt Chart Week.

Milestones vs Week	W1	W2	W3	W4	W5	W6	W7	W8	W9	W10	W11	W12	W13	W14	W15	W16	W17	W18	W19	W20	W21	W22	W23	W24	W25	W26	W27
Propose the Industry Project Title																											
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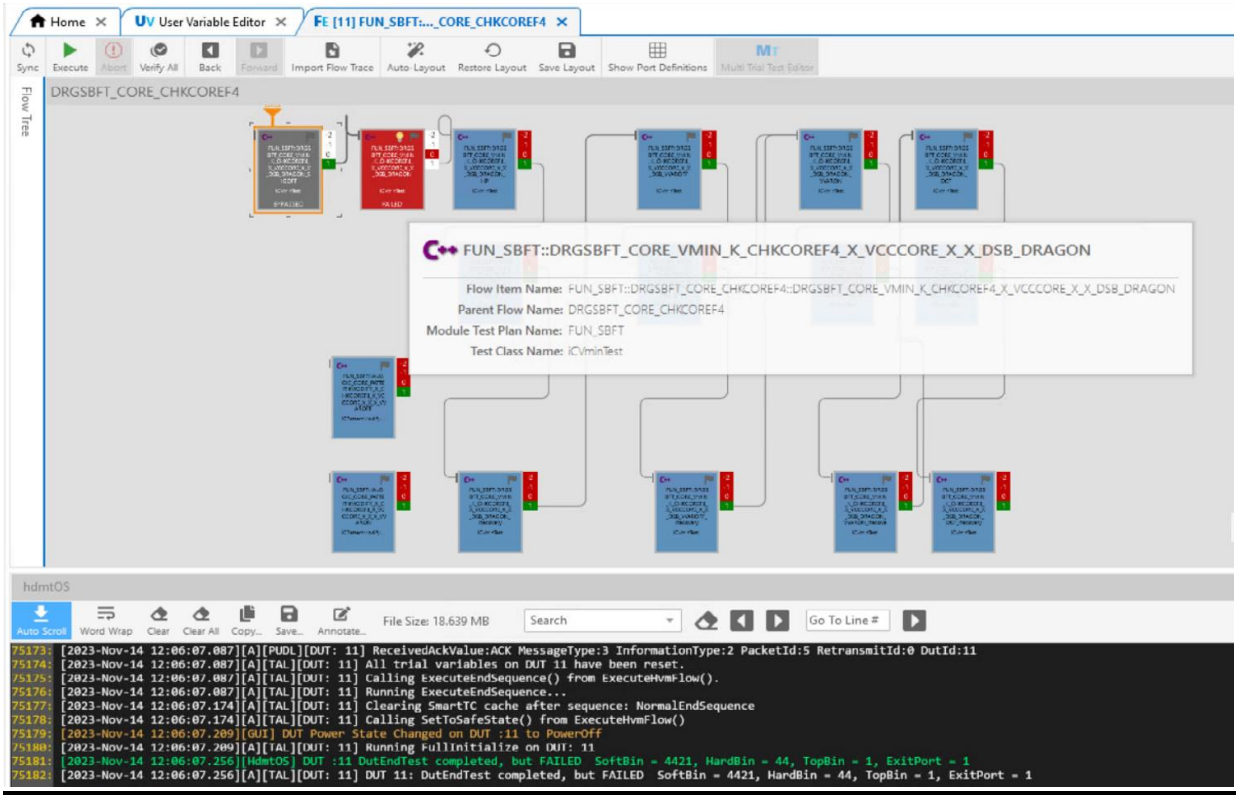
4.0 Preliminary Results (if any)

Example 1: Case of Experiment this defective chipset failing at temperature of 92'C during development milestone and ramp-up stage.

At Intel, we do monitor a bunch of approximately 6 thousand of chipset weekly to monitor the electric quality assurance (EQA) defective unit and performing the validation error before the product being stabilized released to our customer with good quality and save the cost of production.

Step 1: Perform the simulation in HDMT [High Density Modular Tester] to reproduce the error.



Step 2: Perform the analysis of the chipset history results.

LOT	OPER	SSPEC	FB	BINID	VISUAL_ID	PROGRAM_NAME	TESTER_ID	TEMPERATURE	TIUID	UNIT_START_DATE	UNIT_END_DATE
7340G735	7652	----	142	10014200	735S48C600050	EMRSVSPA1B19F00S339	HBI102	75	SPRXBM01163-0-A	10/15/2023 13:21	10/15/2023 14:16
7340G735	6261	----	100	79110000	735S48C600050	EMRXXXXAXH40T10S342	HXV015	100	EMRXCC10T4862	10/23/2023 1:41	10/23/2023 1:51
7340G735	6212	----	100	79110000	735S48C600050	EMRXXXXAXH40T10S342	HXV024	-5	EMRXCC10T4688	10/23/2023 8:22	10/23/2023 8:30
J340F875	6197	RN5A	100	79110000	735S48C600050	EMRXXXXAXH40T10S342	HXV015	25	EMRXCC10T1220	10/24/2023 13:41	10/24/2023 13:42
J340F875	8747	RN5A	8888	88888888	735S48C600050	EMRA1X3B10F2339	HSX118			10/25/2023 22:31	10/25/2023 22:31
J340F875	8747	RN5A	7062	70629338	735S48C600050	EMRA1X3B10F2339A	HSX124			10/25/2023 22:58	10/25/2023 23:25
J340F875	7686	RN5A	9300	93000000	735S48C600050	EMRA1X2JF2342A	HSX141			10/27/2023 7:10	10/27/2023 7:10
J340F875	6208	RN5A	4424	90444424	735S48C600050	EMRXXXXAXH40T10S342	HXV020	92	EMRXCC10T4705	10/27/2023 18:27	10/27/2023 18:29
J340F875	6208	RN5A	4424	90444424	735S48C600050	EMRXXXXAXH40T10S342	HXV020	92	EMRXCC10T1492	10/27/2023 18:54	10/27/2023 18:56
J340F875AA	5208	RN5A	9901	90999901	735S48C600050	EMRXXXXAXH40T10S342	HXV015	92	EMRXCC10T0753	10/31/2023 0:08	10/31/2023 0:20
J340F875QZ1	5208	RN5A	4422	90444422	735S48C600050	EMRXXXXAXH40U00S343	HMV111	92	EMRXCC10T4853	11/9/2023 5:14	11/9/2023 5:17
J340F875QZ1	5208	RN5A	4421	90444421	735S48C600050	EMRXXXXAXH40U00S343	HMV111	92	EMRXCC10T2837	11/9/2023 5:17	11/9/2023 5:19
J340F875QZ2	5208	RN5A	4422	90444422	735S48C600050	EMRXXXXAXH40U00S343	HMV111	92	EMRXCC10T4853	11/9/2023 5:26	11/9/2023 5:29
J340F875QZ2	5208	RN5A	4421	90444421	735S48C600050	EMRXXXXAXH40U00S343	HMV111	92	EMRXCC10T2837	11/9/2023 5:29	11/9/2023 5:32
J340F875DOE	5208	RN5A	6282	90626282	735S48C600050	EMRXXXXAXH40U00SBFT	HMV111	92	EMRXCC10T4853	11/22/2023 10:29	11/22/2023 10:34
J340F875DOE	5208	RN5A	100	79110000	735S48C600050	EMRXXXXAXH40U00SBFT	HMV111	92	EMRXCC10T2837	11/22/2023 10:34	11/22/2023 10:42

Step 3: Analyze the Vmin Testpoint for the Core/RAM that fail inside the chipsets.

0_tname_FUN_SBFT::DRGSBFT_CORE_VMIN_K_CHKCOREF4_X_VCCCORE_X_X_DSB_DRAGON_REFCORES
0_strgval_1010101010101001001001010101010101010101010101101011010101010101010:0000001000000000000000001000000000100000000000000000000000000::DIE1=13,25,31:DIE0=6,32,24
0_tname_FUN_SBFT::DRGSBFT_CORE_VMIN_K_CHKCOREF4_X_VCCCORE_X_X_DSB_DRAGON_REFCORES
0_strgval_0101010101010110101101010101010101010101010010010010101010101:0000001000000000000000001000000000100000000000000000000000000::DIE1=6,32,24:DIE0=13,25,31
0_tname_FUN_SBFT::DRGSBFT_CORE_VMIN_K_CHKCOREF4_X_VCCCORE_X_X_DSB_DRAGON
0_strgval_

Final Vmin Testpoint
0.757_0.756_0.745_0.747_0.745_0.755_-8888_0.757_0.765_0.747_0.747_0.747_0.747_0.745_0.755_0.747_0.745_0.737_0.737_0.737_0.747_0.746_0.747_0.755_0.747_-8888_0.747_0.747_0.747_0.747_0.837_0.737_0.737_ DIE1
0.783_0.783_0.773_-8888_0.773_0.765_0.765_0.755_0.773_0.773_0.775_0.765_0.773_0.773_0.775_0.765_0.773_0.785_0.773_0.765_0.773_0.783_0.755_0.773_0.765_0.765_0.773_0.763_0.765_0.765_0.755_0.763_0.765| DIE0

Max Range of Vmin Testpoint
0.837_0.836_0.825_0.827_0.825_0.835_1.200_0.837_0.845_0.827_0.827_0.827_0.827_0.825_0.835_0.827_0.825_0.817_0.817_0.817_0.827_0.826_0.827_0.835_0.827_1.200_0.827_0.827_0.827_0.827_0.857_0.817_0.817_ DIE1
0.863_0.863_0.853_0.853_0.853_0.845_0.845_0.835_0.853_0.853_0.855_0.845_0.853_0.853_0.855_0.845_0.853_0.865_0.853_0.845_0.853_0.863_0.835_0.853_0.845_0.845_0.853_0.843_0.845_0.845_0.835_0.843_0.845| DIE0

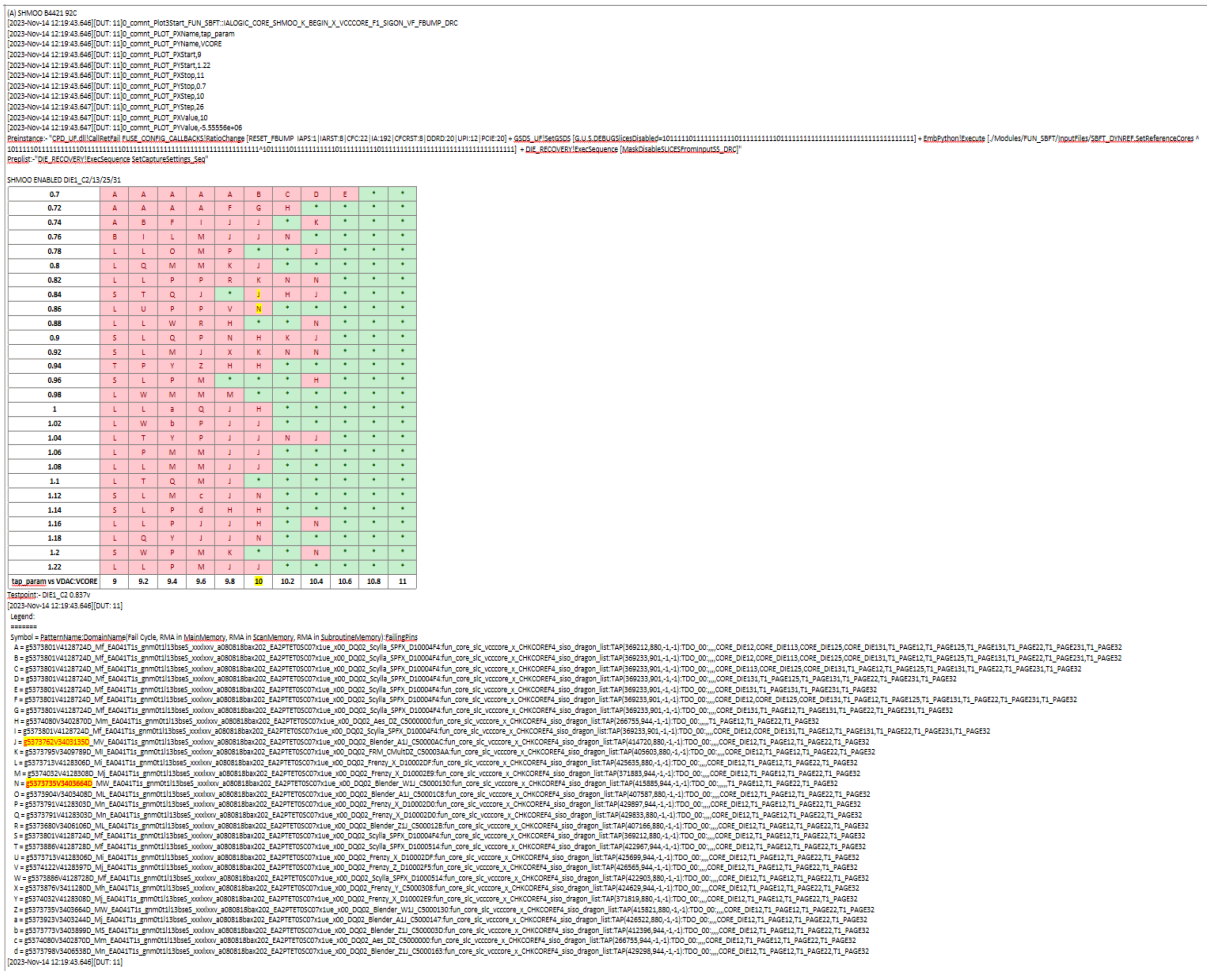
Initial Start of Vmin Testpoint
0.757_0.756_0.745_0.747_0.745_0.755_0.400_0.757_0.765_0.747_0.747_0.747_0.747_0.745_0.755_0.747_0.745_0.737_0.737_0.737_0.747_0.746_0.747_0.755_0.747_0.400_0.747_0.747_0.747_0.747_0.777_0.737_0.737_ DIE1
0.783_0.783_0.773_0.773_0.773_0.765_0.765_0.755_0.773_0.773_0.775_0.765_0.773_0.773_0.775_0.765_0.773_0.785_0.773_0.765_0.773_0.783_0.755_0.773_0.765_0.765_0.773_0.763_0.765_0.765_0.755_0.763_0.765_ DIE0
0_tname_FUN_SBFT::DRGSBFT_CORE_VMIN_K_CHKCOREF4_X_VCCCORE_X_X_DSB_DRAGON::sd
0_strgval_

Pattern String
na_na_na_na_na_na_na_na_na_na_na_na_na_na_na_na_na_na_na_na_na_na_na_na_na_na_na_na_na_na_na_3403664_na_na_ DIE1
na_na_na_na_na_na_na_na_na_na_na_na_na_na_na_na_na_na_na_na_na_na_na_na_na_na_na_na_na_na_na_na_na_na_na_na| DIE0

Core Iteration String
0_0_0_0_0_0_0_0_0_0_0_0_0_0_0_0_0_0_0_0_0_0_0_0_0_0_0_0_0_0_0_0_0_0_0_6_0_0_ DIE1
0_0_0_0_0_0_0_0_0_0_0_0_0_0_0_0_0_0_0_0_0_0_0_0_0_0_0_0_0_0_0_0_0_0_0_0_0_0_0_0|1_7 DIE0

Testpoint calculation of DIE1_Core2
Initial Start Vmin + (Core-Iteration * resolution stepping)
0.777+(6*0.01)=0.837

Step 4: Correlate the Vmin testpoint analysis in step3 and mapping with the shmoo plot below.



(A) SHMOO B4421 92C
[2023-Nov-14 12:19:43.646][DUT: 11]0_comnt_PlotSStart_FUN_SBFT::IALOGIC_CORE_SHMOO_K_BEGIN_X_VCCCORE_F1_SIGON_VF_FBUMP_DRC
[2023-Nov-14 12:19:43.646][DUT: 11]0_comnt_PLOT_PXName,tap_param
[2023-Nov-14 12:19:43.646][DUT: 11]0_comnt_PLOT_PYName,VCORE
[2023-Nov-14 12:19:43.646][DUT: 11]0_comnt_PLOT_PXStart,9
[2023-Nov-14 12:19:43.646][DUT: 11]0_comnt_PLOT_PYStart,1.22
[2023-Nov-14 12:19:43.646][DUT: 11]0_comnt_PLOT_PXStop,11
[2023-Nov-14 12:19:43.646][DUT: 11]0_comnt_PLOT_PYStop,0.7
[2023-Nov-14 12:19:43.646][DUT: 11]0_comnt_PLOT_PXStep,10
[2023-Nov-14 12:19:43.647][DUT: 11]0_comnt_PLOT_PYStep,26
[2023-Nov-14 12:19:43.647][DUT: 11]0_comnt_PLOT_PXValue,10
[2023-Nov-14 12:19:43.647][DUT: 11]0_comnt_PLOT_PYValue,-5.55556e+06
Preinstance= - "CPD_UF.dll!CallRetFail FUSE_CONFIG_CALLBACKS!RatioChange [RESET_FBUMP IAPS:1 |IARST:B |CFC:22 |IA:192 |CFCRST:B |DDRD:20 |UPI:12 |PCIE:20] + GSDS_UF!SetGSDS [G.U.S.DEBUGSlicesDisabled=10111110111111111101111111111101111111111111111111111111111111] + EmbPythonExecute [./Modules/FUN_SBFT/inputfiles/SBFT_DirNREF.SetReferenceCores ^
10111110111111111110111111111101111111111111111111111111111111^10111101111111111101111111111101111111111111111111111111111111] + DIE_RECOVERY!ExecSequence [MaskDisableSLICESFrominputSS_DRC]"
Preplist= - "DIE_RECOVERY!ExecSequence SetCaptureSettings_Seq"

SHMOO ENABLED DIE1_C2/13/25/31

0.7	A	A	A	A	A	B	C	D	E	*	*
0.72	A	A	A	A	F	G	H	*	*	*	*
0.74	A	B	F	I	J	J	*	K	*	*	*
0.76	B	I	L	M	J	J	N	*	*	*	*
0.78	L	L	O	M	P	*	*	J	*	*	*
0.8	L	Q	M	M	K	J	*	*	*	*	*
0.82	L	L	P	P	R	K	N	N	*	*	*
0.84	S	T	Q	J	*	J	H	J	*	*	*
0.86	L	U	P	P	V	N	*	*	*	*	*
0.88	L	L	W	R	H	*	*	N	*	*	*
0.9	S	L	Q	P	N	H	K	J	*	*	*
0.92	S	L	M	J	X	K	N	N	*	*	*
0.94	T	P	Y	Z	H	H	*	*	*	*	*
0.96	S	L	P	M	*	*	*	H	*	*	*
0.98	L	W	M	M	M	*	*	*	*	*	*
1	L	L	a	Q	J	H	*	*	*	*	*
1.02	L	W	b	P	J	J	*	*	*	*	*
1.04	L	T	Y	P	J	J	N	J	*	*	*
1.06	L	P	M	M	J	J	*	*	*	*	*
1.08	L	L	M	M	J	J	*	*	*	*	*
1.1	L	T	Q	M	J	*	*	*	*	*	*
1.12	S	L	M	c	J	N	*	*	*	*	*
1.14	S	L	P	d	H	H	*	*	*	*	*
1.16	L	L	P	J	J	H	*	N	*	*	*
1.18	L	Q	Y	J	J	N	*	*	*	*	*
1.2	S	W	P	M	K	*	*	N	*	*	*
1.22	L	L	P	M	J	J	*	*	*	*	*
tap_param vs VDAC:VCORE	9	9.2	9.4	9.6	9.8	10	10.2	10.4	10.6	10.8	11

Testpoint - DIE1_C2 0.837v
[2023-Nov-14 12:19:43.646][DUT: 11]
Legend:
=======
Symbol = Pattern:name:Domain:name:Fail Cycle, RMA in Main:Memory, RMA in Scan:Memory, RMA in Subroutine:Memory:Failing:Pins
A = g5373801v41287240_MF_EA0417:1s_gnm0t:1i13bse5_xxxlxxv_a080818bax202_EA2PTET05C07x1ue_x00_DQ02_Scylla_SPFX_D10004F4:fun_core_slc_vcccore_x_CHKCOREF4_siso_dragon_list:TAP[369212,880,-1,-1]:TDO_00:,,,,CORE_DIE12,CORE_DIE113,CORE_DIE125,CORE_DIE131,T1_PAGE12,T1_PAGE125,T1_PAGE131,T1_PAGE22,T1_PAGE231,T1_PAGE32
B = g5373801v41287240_MF_EA0417:1s_gnm0t:1i13bse5_xxxlxxv_a080818bax202_EA2PTET05C07x1ue_x00_DQ02_Scylla_SPFX_D10004F4:fun_core_slc_vcccore_x_CHKCOREF4_siso_dragon_list:TAP[369233,901,-1,-1]:TDO_00:,,,,CORE_DIE12,CORE_DIE113,CORE_DIE125,CORE_DIE131,T1_PAGE12,T1_PAGE125,T1_PAGE131,T1_PAGE22,T1_PAGE231,T1_PAGE32
C = g5373801v41287240_MF_EA0417:1s_gnm0t:1i13bse5_xxxlxxv_a080818bax202_EA2PTET05C07x1ue_x00_DQ02_Scylla_SPFX_D10004F4:fun_core_slc_vcccore_x_CHKCOREF4_siso_dragon_list:TAP[369233,901,-1,-1]:TDO_00:,,,,CORE_DIE113,CORE_DIE125,CORE_DIE131,T1_PAGE12,T1_PAGE125,T1_PAGE131,T1_PAGE22,T1_PAGE231,T1_PAGE32
D = g5373801v41287240_MF_EA0417:1s_gnm0t:1i13bse5_xxxlxxv_a080818bax202_EA2PTET05C07x1ue_x00_DQ02_Scylla_SPFX_D10004F4:fun_core_slc_vcccore_x_CHKCOREF4_siso_dragon_list:TAP[369233,901,-1,-1]:TDO_00:,,,,CORE_DIE131,T1_PAGE125,T1_PAGE131,T1_PAGE22,T1_PAGE231,T1_PAGE32
E = g5373801v41287240_MF_EA0417:1s_gnm0t:1i13bse5_xxxlxxv_a080818bax202_EA2PTET05C07x1ue_x00_DQ02_Scylla_SPFX_D10004F4:fun_core_slc_vcccore_x_CHKCOREF4_siso_dragon_list:TAP[369233,901,-1,-1]:TDO_00:,,,,CORE_DIE131,T1_PAGE131,T1_PAGE231,T1_PAGE32
F = g5373801v41287240_MF_EA0417:1s_gnm0t:1i13bse5_xxxlxxv_a080818bax202_EA2PTET05C07x1ue_x00_DQ02_Scylla_SPFX_D10004F4:fun_core_slc_vcccore_x_CHKCOREF4_siso_dragon_list:TAP[369233,901,-1,-1]:TDO_00:,,,,CORE_DIE12,CORE_DIE125,CORE_DIE131,T1_PAGE12,T1_PAGE125,T1_PAGE131,T1_PAGE22,T1_PAGE231,T1_PAGE32
G = g5373801v41287240_MF_EA0417:1s_gnm0t:1i13bse5_xxxlxxv_a080818bax202_EA2PTET05C07x1ue_x00_DQ02_Scylla_SPFX_D10004F4:fun_core_slc_vcccore_x_CHKCOREF4_siso_dragon_list:TAP[369233,901,-1,-1]:TDO_00:,,,,CORE_DIE131,T1_PAGE12,T1_PAGE131,T1_PAGE22,T1_PAGE231,T1_PAGE32
H = g5374080v54028700_Mm_EA0417:1s_gnm0t:1i13bse5_xxxlxxv_a080818bax202_EA2PTET05C07x1ue_x00_DQ02_Aes_02_C5000000:fun_core_slc_vcccore_x_CHKCOREF4_siso_dragon_list:TAP[266755,944,-1,-1]:TDO_00:,,,,T1_PAGE12,T1_PAGE22,T1_PAGE32
I = g5373801v41287240_MF_EA0417:1s_gnm0t:1i13bse5_xxxlxxv_a080818bax202_EA2PTET05C07x1ue_x00_DQ02_Scylla_SPFX_D10004F4:fun_core_slc_vcccore_x_CHKCOREF4_siso_dragon_list:TAP[369233,901,-1,-1]:TDO_00:,,,,CORE_DIE12,CORE_DIE131,T1_PAGE12,T1_PAGE131,T1_PAGE22,T1_PAGE231,T1_PAGE32
J = g5373762v54031350_MV_EA0417:1s_gnm0t:1i13bse5_xxxlxxv_a080818bax202_EA2PTET05C07x1ue_x00_DQ02_Blender_A1i_C50000AC:fun_core_slc_vcccore_x_CHKCOREF4_siso_dragon_list:TAP[414720,880,-1,-1]:TDO_00:,,,,CORE_DIE12,T1_PAGE12,T1_PAGE22,T1_PAGE32
K = g5373795v53409789Q_Mi_EA0417:1s_gnm0t:1i13bse5_xxxlxxv_a080818bax202_EA2PTET05C07x1ue_x00_DQ02_PRM_CMultD2_C50003AA:fun_core_slc_vcccore_x_CHKCOREF4_siso_dragon_list:TAP[405803,880,-1,-1]:TDO_00:,,,,CORE_DIE12,T1_PAGE12,T1_PAGE22,T1_PAGE32
L = g5373713v41288060_Mi_EA0417:1s_gnm0t:1i13bse5_xxxlxxv_a080818bax202_EA2PTET05C07x1ue_x00_DQ02_Frenzy_X_D10002DF:fun_core_slc_vcccore_x_CHKCOREF4_siso_dragon_list:TAP[425635,880,-1,-1]:TDO_00:,,,,CORE_DIE12,T1_PAGE12,T1_PAGE22,T1_PAGE32
M = g5374032v41285080_Mi_EA0417:1s_gnm0t:1i13bse5_xxxlxxv_a080818bax202_EA2PTET05C07x1ue_x00_DQ02_Frenzy_X_D10002E9:fun_core_slc_vcccore_x_CHKCOREF4_siso_dragon_list:TAP[371885,944,-1,-1]:TDO_00:,,,,CORE_DIE12,T1_PAGE12,T1_PAGE22,T1_PAGE32
N = g5373735V54036640_MW_EA0417:1s_gnm0t:1i13bse5_xxxlxxv_a080818bax202_EA2PTET05C07x1ue_x00_DQ02_Blender_W1i_C5000190:fun_core_slc_vcccore_x_CHKCOREF4_siso_dragon_list:TAP[415885,944,-1,-1]:TDO_00:,,,,T1_PAGE12,T1_PAGE22,T1_PAGE32
O = g5373904V54034080_ML_EA0417:1s_gnm0t:1i13bse5_xxxlxxv_a080818bax202_EA2PTET05C07x1ue_x00_DQ02_Blender_A1i_C50001C8:fun_core_slc_vcccore_x_CHKCOREF4_siso_dragon_list:TAP[407587,880,-1,-1]:TDO_00:,,,,CORE_DIE12,T1_PAGE12,T1_PAGE22,T1_PAGE32
P = g5373791v41288030_Mh_EA0417:1s_gnm0t:1i13bse5_xxxlxxv_a080818bax202_EA2PTET05C07x1ue_x00_DQ02_Frenzy_X_D10002DC:fun_core_slc_vcccore_x_CHKCOREF4_siso_dragon_list:TAP[429897,944,-1,-1]:TDO_00:,,,,CORE_DIE12,T1_PAGE12,T1_PAGE22,T1_PAGE32
Q = g5373791v41288030_Mi_EA0417:1s_gnm0t:1i13bse5_xxxlxxv_a080818bax202_EA2PTET05C07x1ue_x00_DQ02_Frenzy_X_D10002D0:fun_core_slc_vcccore_x_CHKCOREF4_siso_dragon_list:TAP[429833,880,-1,-1]:TDO_00:,,,,CORE_DIE12,T1_PAGE12,T1_PAGE22,T1_PAGE32
R = g5373680V54061060_ML_EA0417:1s_gnm0t:1i13bse5_xxxlxxv_a080818bax202_EA2PTET05C07x1ue_x00_DQ02_Blender_Z1i_C5000128:fun_core_slc_vcccore_x_CHKCOREF4_siso_dragon_list:TAP[407166,880,-1,-1]:TDO_00:,,,,CORE_DIE12,T1_PAGE12,T1_PAGE22,T1_PAGE32
S = g5373801v41287240_MF_EA0417:1s_gnm0t:1i13bse5_xxxlxxv_a080818bax202_EA2PTET05C07x1ue_x00_DQ02_Scylla_SPFX_D10004F4:fun_core_slc_vcccore_x_CHKCOREF4_siso_dragon_list:TAP[369212,880,-1,-1]:TDO_00:,,,,CORE_DIE12,T1_PAGE12,T1_PAGE22,T1_PAGE32
T = g5373886V41287280_MF_EA0417:1s_gnm0t:1i13bse5_xxxlxxv_a080818bax202_EA2PTET05C07x1ue_x00_DQ02_Scylla_SPFX_D10005E4:fun_core_slc_vcccore_x_CHKCOREF4_siso_dragon_list:TAP[422967,944,-1,-1]:TDO_00:,,,,CORE_DIE12,T1_PAGE12,T1_PAGE22,T1_PAGE32
U = g5373713V41288060_Mi_EA0417:1s_gnm0t:1i13bse5_xxxlxxv_a080818bax202_EA2PTET05C07x1ue_x00_DQ02_Frenzy_X_D10002DF:fun_core_slc_vcccore_x_CHKCOREF4_siso_dragon_list:TAP[425689,944,-1,-1]:TDO_00:,,,,CORE_DIE12,T1_PAGE12,T1_PAGE22,T1_PAGE32
V = g5374122V41283970_MJ_EA0417:1s_gnm0t:1i13bse5_xxxlxxv_a080818bax202_EA2PTET05C07x1ue_x00_DQ02_Frenzy_Z_D10002F5:fun_core_slc_vcccore_x_CHKCOREF4_siso_dragon_list:TAP[426565,944,-1,-1]:TDO_00:,,,,CORE_DIE12,T1_PAGE12,T1_PAGE22,T1_PAGE32
W = g5373886V41287280_MF_EA0417:1s_gnm0t:1i13bse5_xxxlxxv_a080818bax202_EA2PTET05C07x1ue_x00_DQ02_Scylla_SPFX_D10005E4:fun_core_slc_vcccore_x_CHKCOREF4_siso_dragon_list:TAP[423903,880,-1,-1]:TDO_00:,,,,CORE_DIE12,T1_PAGE12,T1_PAGE22,T1_PAGE32
X = g5373876V54112800_Mh_EA0417:1s_gnm0t:1i13bse5_xxxlxxv_a080818bax202_EA2PTET05C07x1ue_x00_DQ02_Frenzy_Y_C5000308:fun_core_slc_vcccore_x_CHKCOREF4_siso_dragon_list:TAP[414628,944,-1,-1]:TDO_00:,,,,CORE_DIE12,T1_PAGE12,T1_PAGE22,T1_PAGE32
Y = g5374032V41283080_Mj_EA0417:1s_gnm0t:1i13bse5_xxxlxxv_a080818bax202_EA2PTET05C07x1ue_x00_DQ02_Frenzy_X_D10002E9:fun_core_slc_vcccore_x_CHKCOREF4_siso_dragon_list:TAP[371819,880,-1,-1]:TDO_00:,,,,CORE_DIE12,T1_PAGE12,T1_PAGE22,T1_PAGE32
Z = g5373735V53409664Q_MW_EA0417:1s_gnm0t:1i13bse5_xxxlxxv_a080818bax202_EA2PTET05C07x1ue_x00_DQ02_Blender_W1i_C5000190:fun_core_slc_vcccore_x_CHKCOREF4_siso_dragon_list:TAP[415821,880,-1,-1]:TDO_00:,,,,CORE_DIE12,T1_PAGE12,T1_PAGE22,T1_PAGE32
a = g5373923V53403244Q_Mj_EA0417:1s_gnm0t:1i13bse5_xxxlxxv_a080818bax202_EA2PTET05C07x1ue_x00_DQ02_Blender_A1i_C5000147:fun_core_slc_vcccore_x_CHKCOREF4_siso_dragon_list:TAP[426522,880,-1,-1]:TDO_00:,,,,CORE_DIE12,T1_PAGE12,T1_PAGE22,T1_PAGE32
b = g5373773V53403899Q_Mi_EA0417:1s_gnm0t:1i13bse5_xxxlxxv_a080818bax202_EA2PTET05C07x1ue_x00_DQ02_Blender_Z1i_C5000010:fun_core_slc_vcccore_x_CHKCOREF4_siso_dragon_list:TAP[412396,944,-1,-1]:TDO_00:,,,,CORE_DIE12,T1_PAGE12,T1_PAGE22,T1_PAGE32
c = g5374080V54028700_MW_EA0417:1s_gnm0t:1i13bse5_xxxlxxv_a080818bax202_EA2PTET05C07x1ue_x00_DQ02_Aes_02_C5000000:fun_core_slc_vcccore_x_CHKCOREF4_siso_dragon_list:TAP[266755,944,-1,-1]:TDO_00:,,,,CORE_DIE12,T1_PAGE12,T1_PAGE22,T1_PAGE32
d = g5373798V53406538D_Mh_EA0417:1s_gnm0t:1i13bse5_xxxlxxv_a080818bax202_EA2PTET05C07x1ue_x00_DQ02_Blender_Z1i_C5000165:fun_core_slc_vcccore_x_CHKCOREF4_siso_dragon_list:TAP[429298,944,-1,-1]:TDO_00:,,,,CORE_DIE12,T1_PAGE12,T1_PAGE22,T1_PAGE32
[2023-Nov-14 12:19:43.646][DUT: 11]

4.1 Expected Outcomes

We do expect to propose an technical fix plan by modified the wait timing for the particular failure pattern content to achieve the passing vmin testpoint for the defective unit.

Initial Failing Timing String for the pattern content
+ SBFT_WAITTIME MAIN PAT g5373735V3403664D_MW_EA041T1s_gnm0t1l13bseS_xxxlxxv_a080818bax202_EA2PTET0SC07x1ue_x00_DQ02_Blender_W1J_C5000130:STF STF_TEST_WAIT_END -10 OPCODE_OPERAND IT_LOOPSET 20000 + SBFT_WAITTIME MAIN PAT g5373735V3403664D_MW_EA041T1s_gnm0t1l13bseS_xxxlxxv_a080818bax202_EA2PTET0SC07x1ue_x00_DQ02_Blender_W1J_C5000130:TAP TAP_TEST_WAIT_END -5 OPCODE_OPERAND IT_LOOPSET 5000 + SBFT_WAITTIME MAIN PAT g5373762V3403135D_MV_EA041T1s_gnm0t1l13bseS_xxxlxxv_a080818bax202_EA2PTET0SC07x1ue_x00_DQ02_Blender_A1J_C50000AC:STF STF_TEST_WAIT_END -10 OPCODE_OPERAND IT_LOOPSET 20000 + SBFT_WAITTIME MAIN PAT g5373762V3403135D_MV_EA041T1s_gnm0t1l13bseS_xxxlxxv_a080818bax202_EA2PTET0SC07x1ue_x00_DQ02_Blender_A1J_C50000AC:TAP TAP_TEST_WAIT_END -5 OPCODE_OPERAND IT_LOOPSET 5000 + SBFT_WAITTIME MAIN PAT g5373818V3406013D_Ma_EA041T1s_gnm0t1l13bseS_xxxlxxv_a080818bax202_EA2PTET0SC07x1ue_x00_DQ02_Blender_Z1J_C500011E:STF STF_TEST_WAIT_END -10 OPCODE_OPERAND IT_LOOPSET 6000 + SBFT_WAITTIME MAIN PAT g5373818V3406013D_Ma_EA041T1s_gnm0t1l13bseS_xxxlxxv_a080818bax202_EA2PTET0SC07x1ue_x00_DQ02_Blender_Z1J_C500011E:TAP TAP_TEST_WAIT_END -5 OPCODE_OPERAND IT_LOOPSET 1500 + SBFT_WAITTIME MAIN PAT g5374080V3402870D_Mm_EA041T1s_gnm0t1l13bseS_xxxlxxv_a080818bax202_EA2PTET0SC07x1ue_x00_DQ02_Aes_DZ_C5000000:STF STF_TEST_WAIT_END -10 OPCODE_OPERAND IT_LOOPSET 8000 + SBFT_WAITTIME MAIN PAT g5374080V3402870D_Mm_EA041T1s_gnm0t1l13bseS_xxxlxxv_a080818bax202_EA2PTET0SC07x1ue_x00_DQ02_Aes_DZ_C5000000:TAP TAP_TEST_WAIT_END -5 OPCODE_OPERAND IT_LOOPSET 2000

After the New Experiment Implementation of Timing String for the pattern content
+ SBFT_WAITTIME MAIN PAT g5373735V3403664D_MW_EA041T1s_gnm0t1l13bseS_xxxlxxv_a080818bax202_EA2PTET0SC07x1ue_x00_DQ02_Blender_W1J_C5000130:STF STF_TEST_WAIT_END -10 OPCODE_OPERAND IT_LOOPSET **60000** + SBFT_WAITTIME MAIN PAT g5373735V3403664D_MW_EA041T1s_gnm0t1l13bseS_xxxlxxv_a080818bax202_EA2PTET0SC07x1

ue_x00_DQ02_Blender_W1J_C5000130:TAP TAP_TEST_WAIT_END -5 OPCODE_OPERAND IT_LOOPSET **15000**
+ SBFT_WAITTIME MAIN PAT g5373762V3403135D_MV_EA041T1s_gnm0t1l13bseS_xxxlxxv_a080818bax202_EA2PTET0SC07x1ue_x00_DQ02_Blender_A1J_C50000AC:STF STF_TEST_WAIT_END -10 OPCODE_OPERAND IT_LOOPSET **60000**
+ SBFT_WAITTIME MAIN PAT g5373762V3403135D_MV_EA041T1s_gnm0t1l13bseS_xxxlxxv_a080818bax202_EA2PTET0SC07x1ue_x00_DQ02_Blender_A1J_C50000AC:TAP TAP_TEST_WAIT_END -5 OPCODE_OPERAND IT_LOOPSET **15000**
+ SBFT_WAITTIME MAIN PAT g5373818V3406013D_Ma_EA041T1s_gnm0t1l13bseS_xxxlxxv_a080818bax202_EA2PTET0SC07x1ue_x00_DQ02_Blender_Z1J_C500011E:STF STF_TEST_WAIT_END -10 OPCODE_OPERAND IT_LOOPSET **24000**
+ SBFT_WAITTIME MAIN PAT g5373818V3406013D_Ma_EA041T1s_gnm0t1l13bseS_xxxlxxv_a080818bax202_EA2PTET0SC07x1ue_x00_DQ02_Blender_Z1J_C500011E:TAP TAP_TEST_WAIT_END -5 OPCODE_OPERAND IT_LOOPSET **6000**
+ SBFT_WAITTIME MAIN PAT g5374080V3402870D_Mm_EA041T1s_gnm0t1l13bseS_xxxlxxv_a080818bax202_EA2PTET0SC07x1ue_x00_DQ02_Aes_DZ_C5000000:STF STF_TEST_WAIT_END -10 OPCODE_OPERAND IT_LOOPSET **16000**
+ SBFT_WAITTIME MAIN PAT g5374080V3402870D_Mm_EA041T1s_gnm0t1l13bseS_xxxlxxv_a080818bax202_EA2PTET0SC07x1ue_x00_DQ02_Aes_DZ_C5000000:TAP TAP_TEST_WAIT_END -5 OPCODE_OPERAND IT_LOOPSET **4000**

Expected of output results will be passing at the good range of test point.

```
[2023-Nov-15 16:02:22.907][DUT: 11]0_comnt_Plot3Start_FUN_SBFT::IALOGIC_CORE_SHMOO_K_BEGIN_X_VCCCORE_F1_SIGON_VF_FBUMP_DRC
[2023-Nov-15 16:02:22.907][DUT: 11]0_comnt_PLOT_PXName,tap_param
[2023-Nov-15 16:02:22.907][DUT: 11]0_comnt_PLOT_PYName,VCORE
[2023-Nov-15 16:02:22.907][DUT: 11]0_comnt_PLOT_PXStart,9
[2023-Nov-15 16:02:22.907][DUT: 11]0_comnt_PLOT_PYStart,1.2
[2023-Nov-15 16:02:22.907][DUT: 11]0_comnt_PLOT_PXStop,11
[2023-Nov-15 16:02:22.907][DUT: 11]0_comnt_PLOT_PYStop,0.5
[2023-Nov-15 16:02:22.907][DUT: 11]0_comnt_PLOT_PXStep,10
[2023-Nov-15 16:02:22.907][DUT: 11]0_comnt_PLOT_PYStep,35
[2023-Nov-15 16:02:22.907][DUT: 11]0_comnt_PLOT_PXValue,10
[2023-Nov-15 16:02:22.907][DUT: 11]0_comnt_PLOT_PYValue,-5.55556e+06
Preinstance:- "CPD_UF.dll!CallRetFail FUSE_CONFIG_CALLBACKS!RatioChange [RESET_FBUMP  IAPS:1|IARST:8|CFC:22|IA:192|CFCRST:8|DDRD:20|U
10111110111111111101111111111011111111111111111111111111111111111111^10111110111111111110111111111101111111111111111111
Preplist:-"DIE_RECOVERY!ExecSequence SetCaptureSettings_Seq"

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```

0.5	A	A	B	C	A	B	B	C	C	D	E
0.52	D	F	C	E	C	B	C	A	C	C	D
0.54	E	A	E	C	B	D	G	G	G	G	H
0.56	D	G	G	H	G	H	H	H	H	H	H
0.58	G	H	H	H	H	H	H	H	H	H	H
0.6	H	H	H	H	H	H	H	H	I	B	C
0.62	H	H	G	H	H	I	C	C	C	C	C
0.64	H	I	I	C	C	C	C	D	D	H	H
0.66	I	C	C	C	D	G	H	H	H	H	H
0.68	C	C	G	G	H	H	H	H	J	K	L
0.7	G	H	H	H	H	H	K	L	M	*	*
0.72	H	H	H	J	K	L	N	*	*	*	*
0.74	H	H	J	O	P	*	*	*	*	*	*
0.76	H	Q	R	P	S	*	*	*	*	*	*
0.78	O	T	U	V	*	*	*	*	*	*	*
0.8	T	W	W	S	*	*	*	*	*	*	*
0.82	T	T	X	P	*	*	*	*	*	*	*
0.84	T	T	T	Y	X	*	*	*	*	*	*
0.86	T	Z	R	P	S	*	*	*	*	*	*
0.88	T	T	a	b	S	*	*	*	*	*	*
0.9	c	T	Z	R	V	*	*	*	*	*	*
0.92	T	R	a	P	d	*	*	*	*	*	*
0.94	T	T	R	P	*	*	*	*	*	*	*
0.96	c	R	b	S	*	*	*	*	*	*	*
0.98	e	T	R	f	*	S	*	*	*	*	*
1	T	T	R	P	*	*	*	*	*	*	*
1.02	T	a	R	d	S	*	*	*	*	*	*
1.04	a	W	R	X	*	*	*	*	*	*	*
1.06	T	T	R	P	g	*	*	*	*	*	*
1.08	T	T	R	f	S	*	*	*	*	*	*
1.1	T	T	a	b	*	S	*	*	*	*	*
1.12	a	Z	a	d	*	*	*	*	*	*	*
1.14	T	Z	a	d	*	*	*	*	*	*	*
1.16	T	T	T	P	P	g	*	*	*	*	*
1.18	T	T	a	P	d	*	*	*	*	*	*
1.2	T	Z	Z	V	g	*	*	*	*	*	*
tap_param vs VDAC:VCORE	9	9.2	9.4	9.6	9.8	10	10.2	10.4	10.6	10.8	11

Testpoint:- DIE1_C2 0.767v

5.0 Conclusion

To conclude this industry project proposal is the SBFT flow configuration overview had been developed and designed and the simulation work need to be further executed and bring into the tools to test to achieve the objectives. The evaluation of the results implementation needs to be further analysis and the Yield percentage graph will need to be sketching out in the graphical plot to show the acceptable percentage which fulfill the passing range. Hence, the extension more journal review needs to continue in order to have more methodology to be carried out in simulation experiment.

6.0 References

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End of Project Proposal