REVA UNIVERSITY

BENGALURU, INDIA

Analog and Digital Electronics Lab

B20CS0301

Third Semester AI&ML

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SCHOOL OF COMPUTING AND INFORMATION TECHNOLOGY

Name	
Srn	
Branch	
Semester	
Section	
Academic Year	

CONTENTS

Experiment No. 1

CLIPPING & CLAMPING CIRCUITS

Aim: To simulate a positive clipper, double ended clipper & positive clamper circuits using diodes.

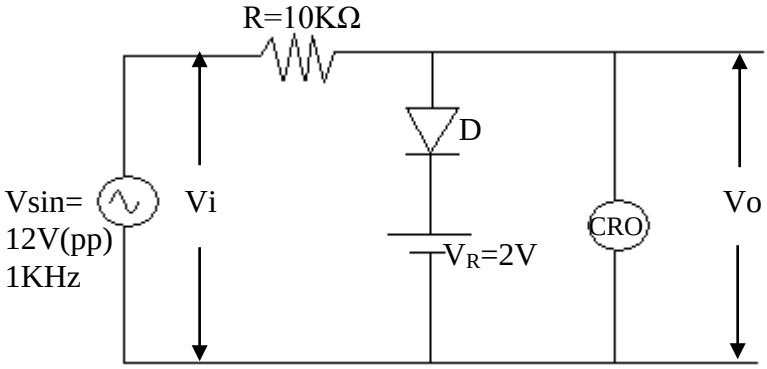
Theory: An electronic device that is used to evade the output of a circuit to go beyond the preset value (voltage level) without varying the remaining part of the input waveform is called as **Clipper circuit.** An electronic circuit that is used to alter the positive peak or negative peak of the input signal to a definite value by shifting the entire signal up or down to obtain the output signal peaks at desired level is called as **Clamper circuit**.

Components Required:

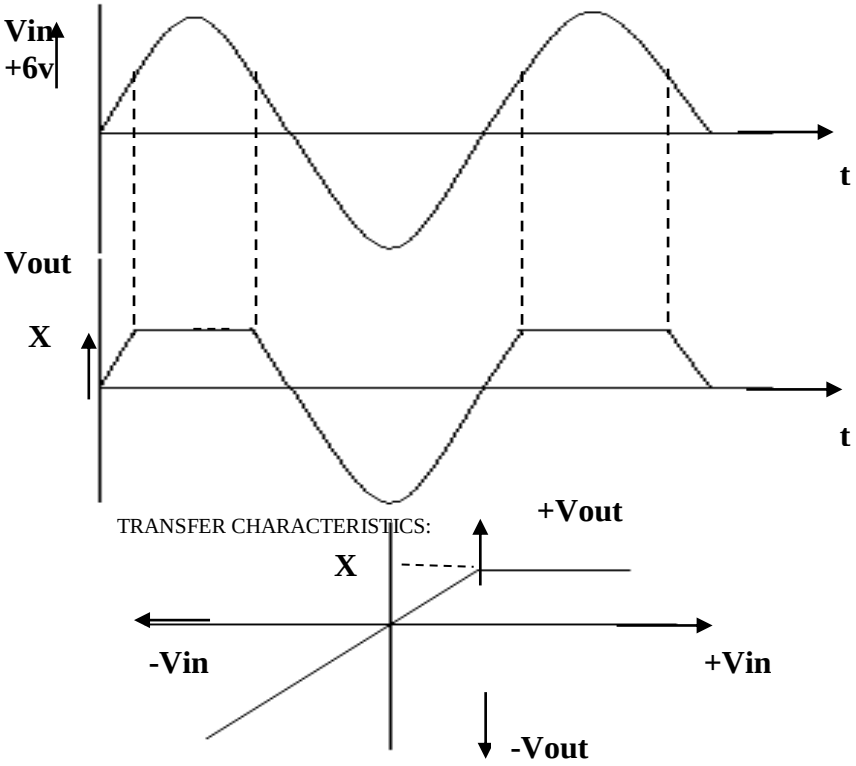
1) Diodes - D1N4007 - 2 Nos.
2) Resistor – 10K
3) Power supply VDC - 2 Nos.
4) Sinusoidal signal generator(VAC) 12V(PP), 1 KHz

A) <u>Positive clipping</u>

CIRCUIT DIAGRAM:



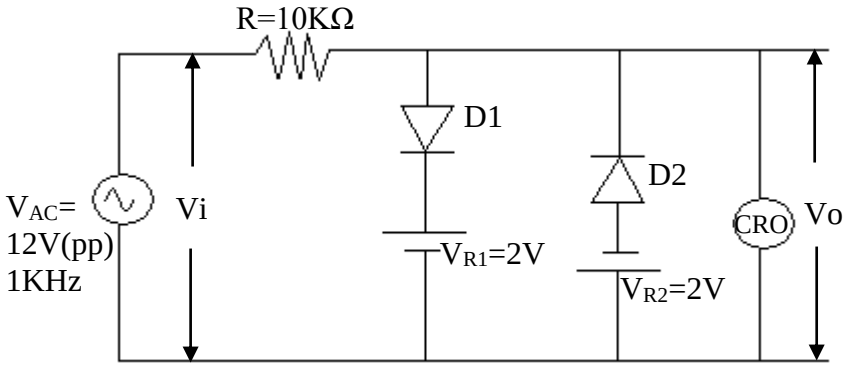
WAVEFORMS:



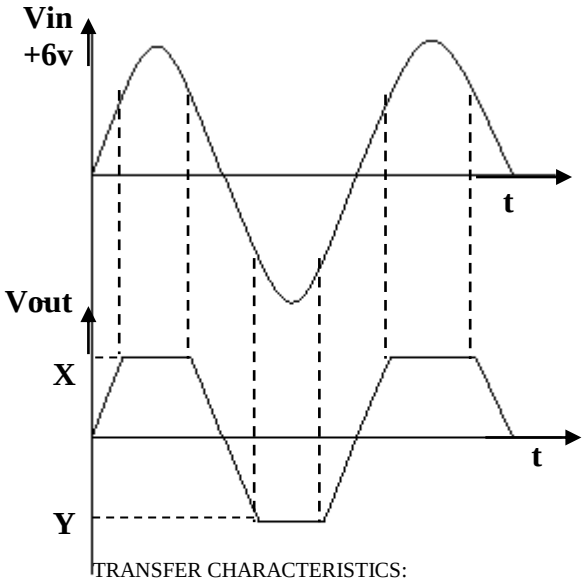
TRANSFER CHARACTERISTICS:

B) <u>DOUBLE ENDED CLIPPER</u>

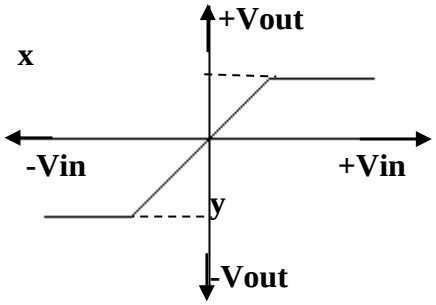
CIRCUIT DIAGRAM:



WAVEFORMS:



TRANSFER CHARACTERISTICS:



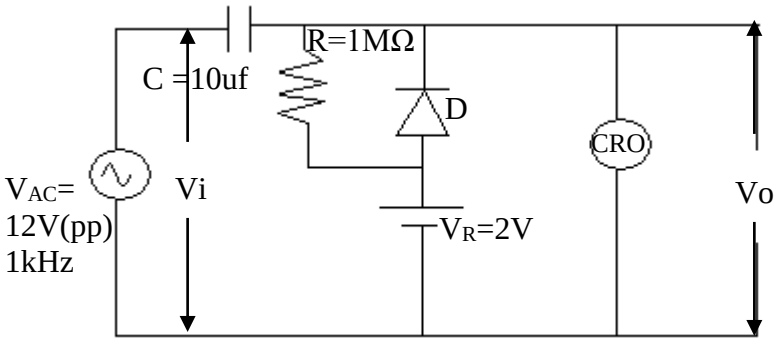
1. POSITIVE CLAMPING CIRCUIT

Components/Apparatus required:

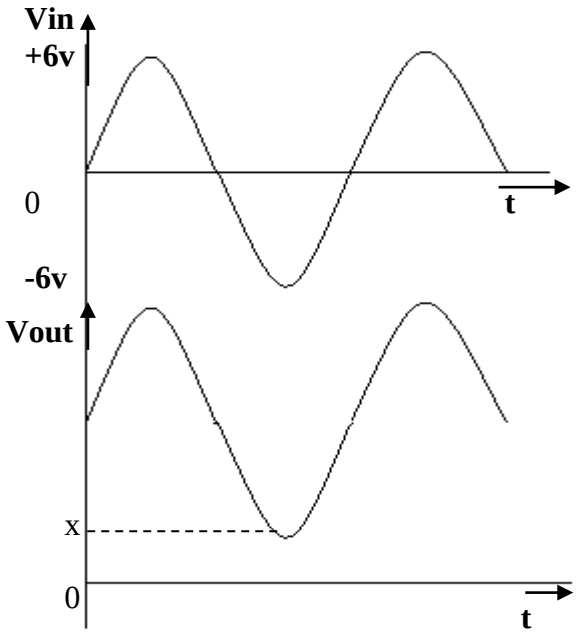
1) Diodes - D1N4007
2) Resistor – 1MΩ
3) Capacitor – 10uf
4) Power supply VDC
5) Sinusoidal signal generator(VAC) 12V(PP), 1 KHz

C) Positive clamping

CIRCUIT DIAGRAM:



WAVEFORMS:



Procedure:

1. Follow the simulation steps given in Expt No 6
2. Use the available cursor on the simulated window to note down the clipped voltage level.
3. Repeat the above steps for the clamping circuits.

Results:

Quantity/Circuit	**Positive cilpper**	**Double-ended clipper**	**Clamper**
X			
Y	---		---------

Experiment No. 2

RELAXATION OSCILLATOR USING OP - AMP

Aim: To simulate a rectangular wave form generator (Opamp relaxation oscillator) and compare the frequency and duty cycle with the design specifications

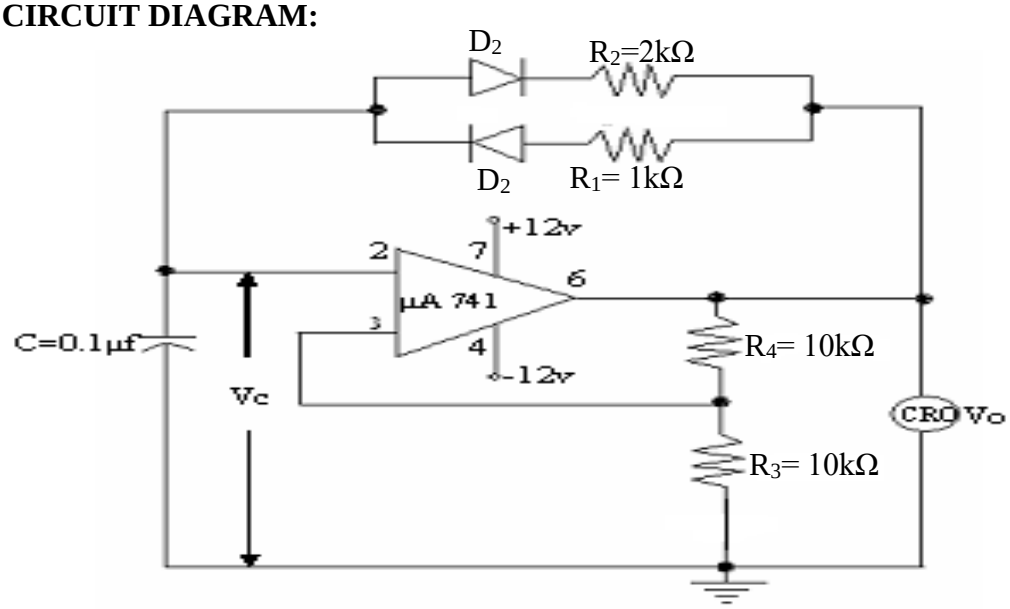
Theory:

The circuits generate rectangular waveform of specified frequency. Op-Amp is used as comparator which compares the voltage at non inverting terminal with capacitor voltage. When the voltage at the output is +βVsat, the capacitor charges to this voltage through R1 during which output remains at +βVsat. When the capacitor voltage exceeds +βVsat output switches to –βVsat and the capacitor starts discharging through R2 to –βVsat. When the capacitor voltage goes below –βVsat, the output again switches back to +βVsat. Thus oscillations are generated, and the time period of oscillation depends on R1, R2, R3, Rf and C.

Components and Equipments required:

1) Op-Amp – μA741
2) Resistors - 1K, 2K, 10K, 20K.
3) Capacitor – 0.1uf
5) Power supply (±15V) DC voltage
6) Diodes – D1N4007 – 2Nos.

CIRCUIT DIAGRAM:



CALCULATION:

$$\beta = \frac{R_3}{R_3 + R_4} = \frac{10k}{10k + 10k} = 0.5$$

For the above circuit

$T_{ON} = R_1 C \ln\left[\frac{1+\beta}{1-\beta}\right]$

$= 1k * 0.1uf * 1.1$

T_{ON} = 0.11mSec

$T_{OFF} = R_2 C \ln\left[\frac{1+\beta}{1-\beta}\right]$

$= 2k * 0.1uf * 1.1$

T_{OFF} = 0.22mSec

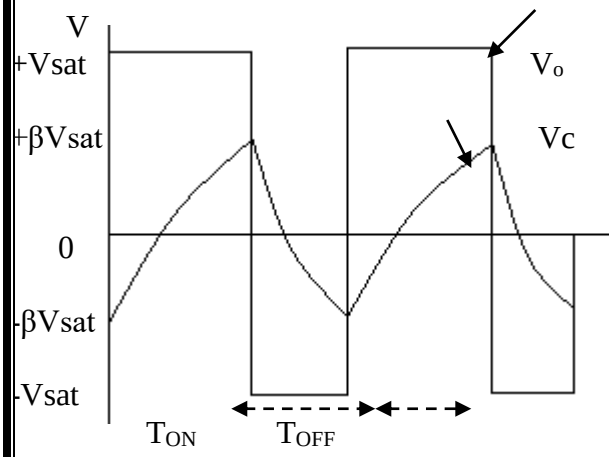
Total time period $T = T_{ON} + T_{OFF} = 0.11mSec + 0.22mSec$

T = 0.33mSec

Duty cycle (D) = $\frac{T_{ON}}{T} = \frac{0.11m\sec}{0.33m\sec} = 0.33 * 100 = 33\%$

$F = \frac{1}{T} = \frac{1}{0.33m\sec} = 3kHz$

WAVEFORMS:



Procedure:

1. Follow the simulation steps given in Expt No 6.
2. Use the available cursor on the simulated window to measure the frequency and duty cycle and compare with the theoretical value.

Results:
The practical time periods are measured and compared with theoretical values and tabulated as shown below:

	T_{ON}	T_{OFF}	V_{OMAx}	$V_{O\ MIN}$	$V_{C\ MAX}$	$V_{C\ MIN}$	**Duty Cycle**
Theoretical value	0.11m Sec	0.22m Sec	+Vsat = 12v	–Vsat = -12v	+βVsat = 6v	–βVsat =-6v	33%
Practical Value							

Experiment No. 3

SCHMITT TRIGGER

Aim: To simulate a Schmitt trigger using Op-amp and compare the UTP andLTP values with the given specification.

Theory:

A Schmitt trigger is a circuit which converts any slow varying waveform into a waveform having abrupt transitions. In the Schmitt trigger circuit op-amp is used as a comparator. A Schmitt trigger is characterized by two voltage levels :

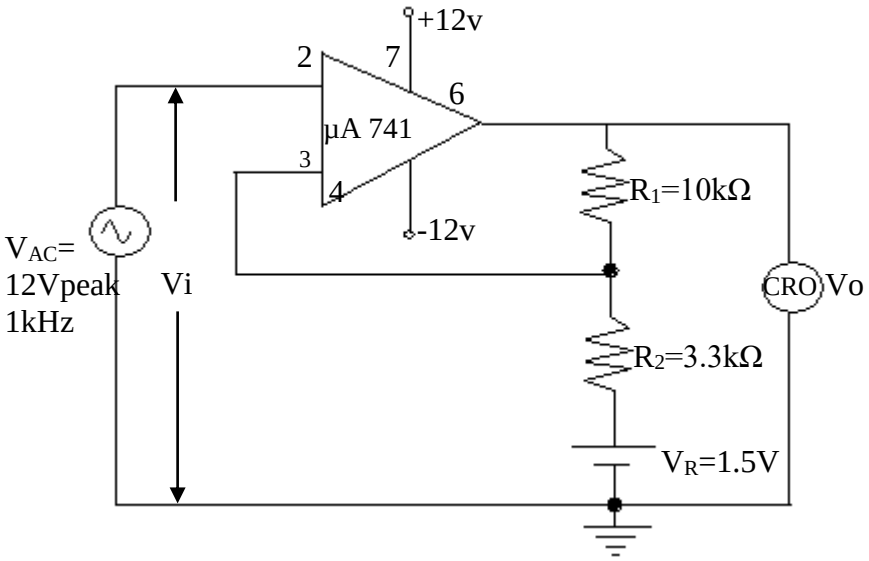
1. UTP – Upper Trigger Point
2. LTP - Lower Trigger Point

The circuits can be realized to have equal UTP and LTP values or with unequal values using a reference voltage.

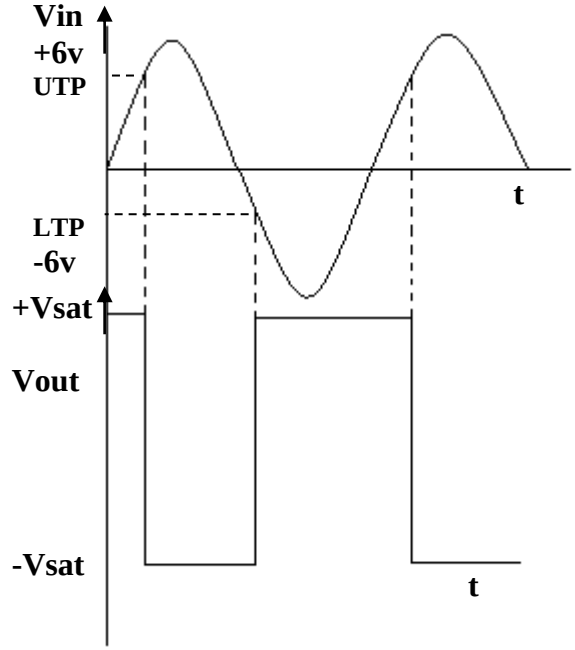
Components/ Apparatus Required:

1) OP-AMP - μA74l
2) Resistors l0KΩ, 3.3KΩ
3) Power supply l2V DC voltage – 2 no.
4) Sinusoidal signal generator(VAC) 12V, 1kHz.

CIRCUIT DIAGRAM:



WAVEFOREMS:



CALCULATIONS:

For the above circuit:

$$\text{UTP} = \frac{+V_{sat}R_2}{R_1+R_2} + \frac{V_R R_1}{R_1+R_2}$$

$$= \frac{12V * 3.3K}{10K+3.3K} + \frac{1.5V * 10K}{10K+3.3K}$$

UTP = 4.32v

$$\text{LTP} = \frac{-V_{sat}R_2}{R_1+R_2} + \frac{V_R R_1}{R_1+R_2}$$

$$= \frac{-12V * 3.3K}{10K+3.3K} + \frac{1.5V * 10K}{10K+3.3K}$$

LTP = -1.62v

Procedure:

1. Follow the simulation steps given in Expt No 6
2. Use the available cursor on the simulated window to measure the UTP and LTP values and compare with the theoretical values.

Result:

Theoretical UTP : _____ Theoretical LTP : _____

Practical UTP : _____ Practical LTP : _____

Experiment No. 4

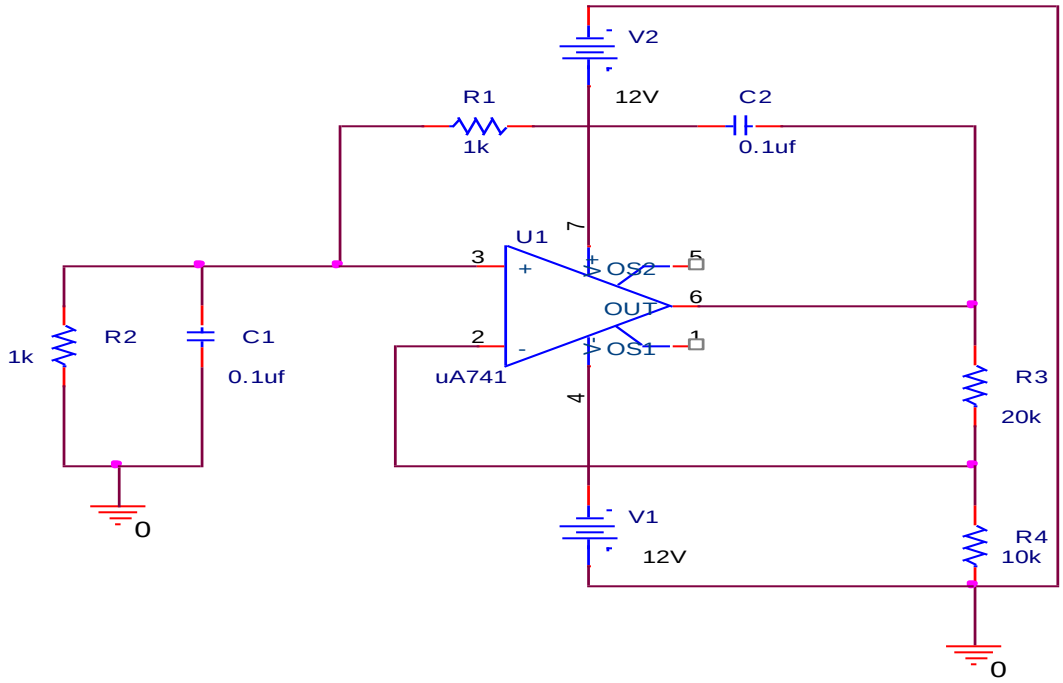
WEIN BRIDGE OSCILLATOR

Aim: To simulate Wein Bridge Ocsillator circuit and verify the frequency generated.

Theory:
The Wien bridge oscillator is developed by Maxwien in the year 1981. The Wien bridge oscillator is based on the bridge circuit it consists of four resistors and two capacitors and it is used for the measurement of impedance.The feedback circuit is used by the Wien bridge oscillator and the circuit consists of a series RC circuit which is connected to the parallel RC circuit. The Wien bridge oscillator is also called as a Wheatstone bridge circuit.

Components and Equipments required:
1) Op-Amp – μA741
2) Resistors - 1k,1k,10k,20k
3) Capacitor – 0.1uf(2 no.)
5) Power supply (±12V) DC voltage

CIRCUIT DIAGRAM:

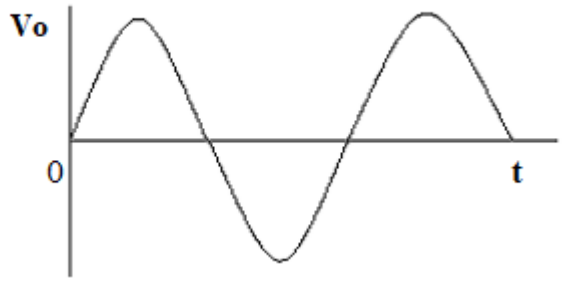


CALCULATION:

Frequency of Oscillation $f_o = \frac{1}{2 * \Pi * R * C} = 1.59$ K Hz

Where R=1K, C=0.1uf

WAVEFORM:



Procedure:

1. Follow the simulation steps given in Expt No 6
2. Use the available cursor on the simulated window to note down the frequency of oscillation.

Results:

Observations/ Quantity	**Time Period(T)**	**Voltage(V)**
Theoretical:		
Practical:		

Experiment No. 5

POWER SUPPLY

Aim: To determine the working of a power supply and observe the waveforms.

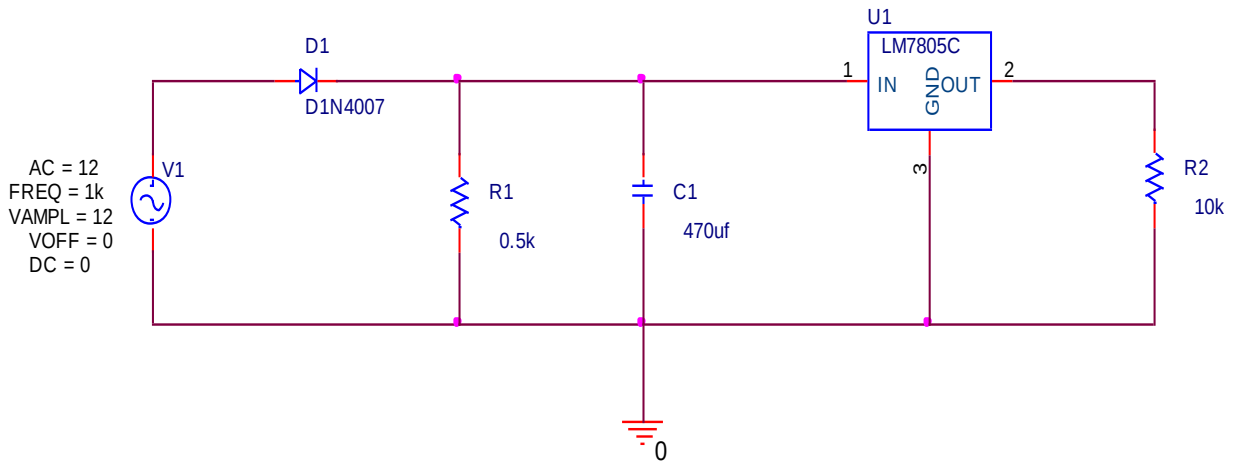
Theory:

Regulated power supply is necessary in some electronic circuits especially in Amplifier circuits. Poorly regulated power may cause buzzing and unwanted noise in RF and amplifier circuits.Rectifier is an electronic circuit consisting of diodes which carries out the rectification process. Rectification is the process of converting an alternating voltage or current into corresponding direct (DC) quantity. The input to a rectifier is AC whereas its output is unidirectional pulsating DC.Although a half wave rectifier could technically be used, its power losses are significant compared to a full wave rectifier. As such, a full wave rectifier or a bridge rectifier is used to rectify both the half cycles of the ac supply (full wave rectification). The rectified voltage from the rectifier is a pulsating DC voltage having very high ripple content. But this is not we want, we want a pure ripple free DC waveform. Hence a filter is used. Different types of filters are used such as capacitor filter, LC filter, Choke input filter, π type filter. The figure shows a capacitor filter connected along the output of the rectifier and the resultant output waveform.The output voltage or current will change or fluctuate when there is a change in the input from ac mains or due to change in load current at the output of the regulated power supply or due to other factors like temperature changes. This problem can be eliminated by using a regulator. A regulator will maintain the output constant even when changes at the input or any other changes occur. Transistor series regulator, Fixed and variable IC regulators or a zener diode operated in the zener region can be used depending on their applications. IC's like 78XX and 79XX (such as the IC 7805) are used to obtained fixed values of voltages at the output.

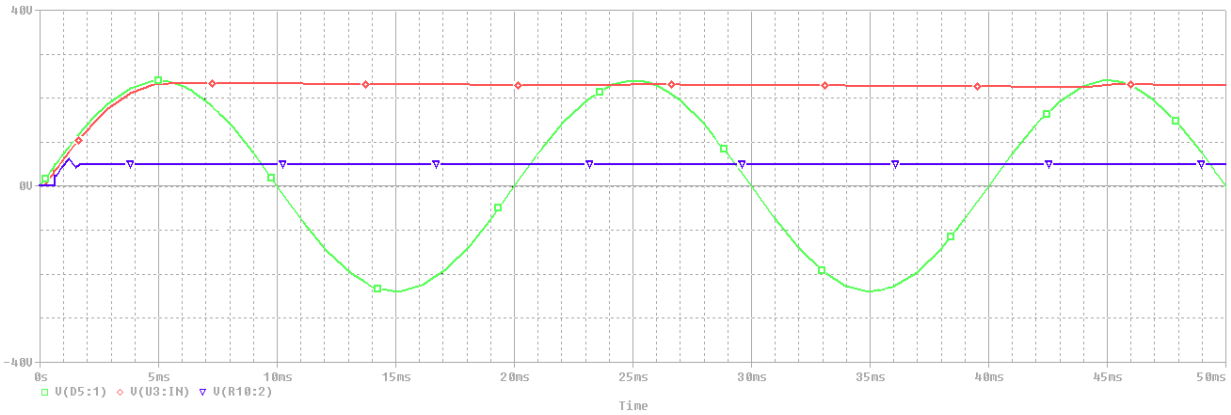
Components and Equipment's required:

1) Diodes-DIN4007(1 Nos)
2) Resistor 0.5K,10k
3) Capacitor 470uf
4) Sinusoidal signal generator(Vsin) 12V(PP), 1 kHz
5) LM 7805 IC

Circuit diagram:



Waveform:



Procedure:

1. Use the available cursor on the simulated window to observe different waveform at various output points.

Results:

Experiment No. 6

RC COUPLED AMPLIFIER

Aim: To build and simulate CE amplifier (RC coupled amplifier) for its frequency response and measure the bandwidth.

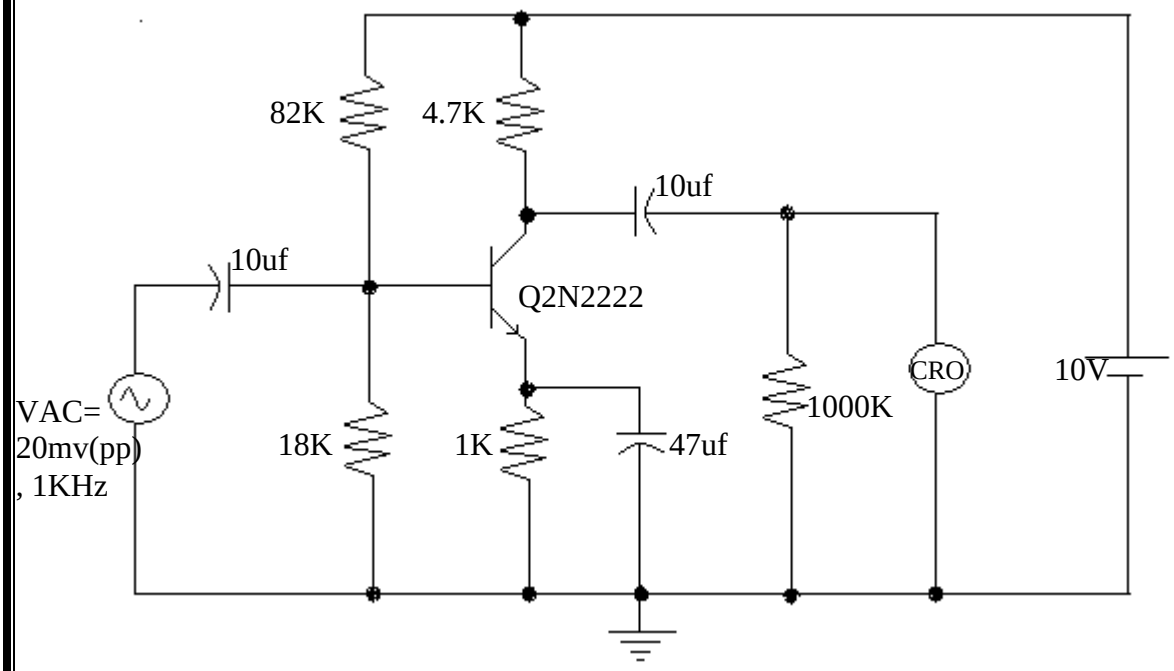
Theory:

RC Coupled Amplifier is an audio frequency amplifier. It is an amplifier that couples input signal to the output by coupling capacitors and collector resistance. The amplifier is biased using voltage divider bias which provides highest stability. The 3db point helps on determining the Bandwidth of the amplifier. The Amplifier has a bypass capacitor which avoids negative feedback and thus increases the amplifier gain.

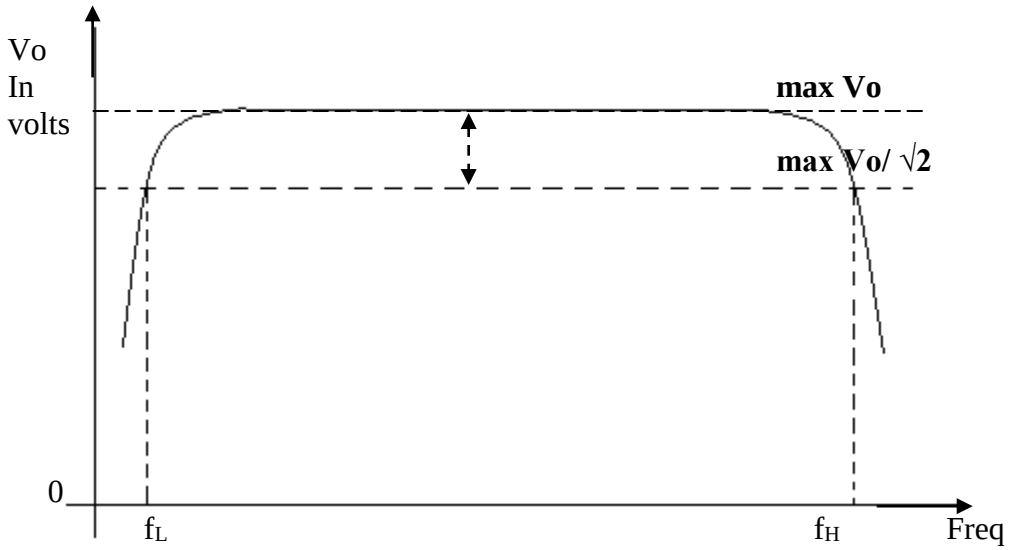
Components and Equipment's required:

1) Transistor (BJT) – Q2N2222
2) Resistors – 82K, 18K, 4.7K, 1K and 1000K
3) Capacitors – 0.1uf (2 each), 10uf(2 each), 47uf
4) Sinusoidal signal generator(VAC) 20mV(PP), 1 kHz
5) Power supply 10V (VDC)

CIRCUIT DIAGRAM:



FREQUENCY RESPONSE:



$$BW = f_H - f_L$$

Procedure:

1. Create the schematic shown above using the following steps.
    - Double click on "**capture CIS**" icon on the desktop
    - Click on **file – New – Project** to create a new project
    - Name the project (Preferably same name as of the circuit)
    - Create the schematic on the schematic window by selecting the parts from the library and inter connecting them using wires.
    - The parts will have default values and are to be changed to the required design values
    - Place voltage markers on the input and output ends of the circuit
2. Apply parameters for simulation in the new simulation profile window and click on **Run**
3. Use the available cursor on the simulated window to note down the bandwidth

Results:

The response of the RC coupled amplifier is simulated and the Bandwidth is _____ Hz

Experiment No 7.

HALF/FULL ADDER AND HALF/FULL SUBTRACTORS

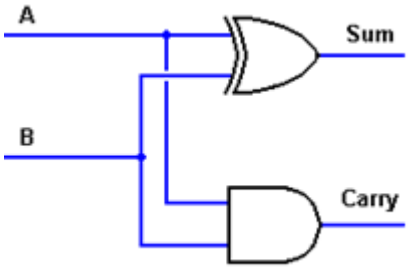
Aim: Realization of Half/Full adder and Half/Full Subtractors using logic gates.

Components/Apparatus required:

1) AND, OR, NOT, EX-OR gates -02 Nos. each
2) Digital trainer kit.
3) Patch chords.

1) Half adder

Circuit diagram:

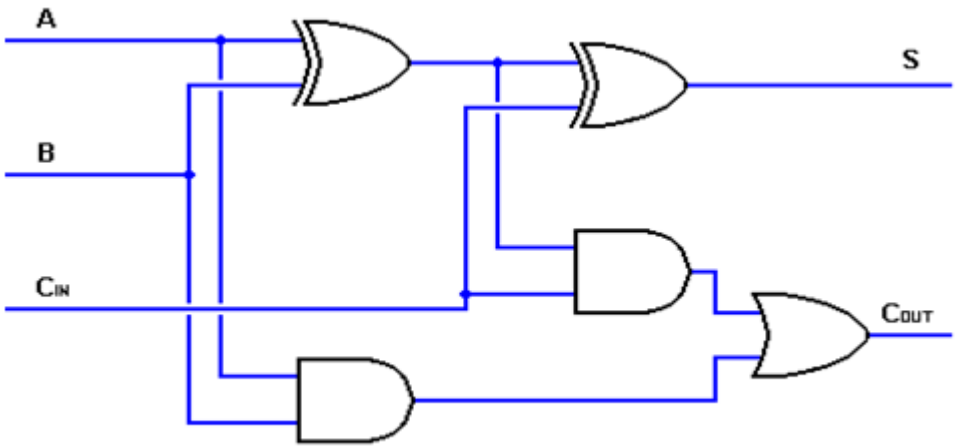


Truth Table

INPUT A	INPUT B	OUTPUT Sum	OUTPUT Carry
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

2) Full adder

Circuitdiagram:

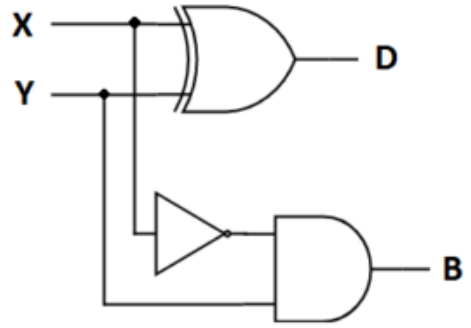


Truth Table

INPUT A	INPUT B	INPUT C_{IN}	OUTPUT S	OUTPUT C_{OUT}
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

3) Half Subtractor

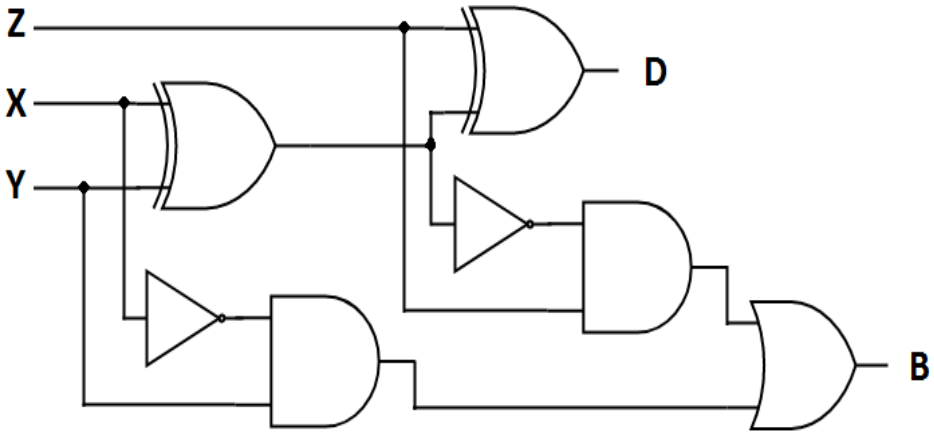
Circuit diagram: Truth Table



INPUT X	INPUT Y	OUTPUT D	OUTPUT B
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0

4)Full Subtractor

Circuit diagram:



Truth Table

INPUT X	INPUT Y	INPUT Z	OUTPUT D	OUTPUT B
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

Procedure:

1) Make connections as shown in the circuit diagram.
2) Connect input to +5v for logic 1 and to ground for logic 0
3) Verify the truth table.

Experiment No. 8

VHDL CODE TO REALIZE FULL ADDER AND FULL SUBTRACTORS

Aim: Design and develop VHDL code to realize Full adder and Full Subtractors.

Steps in Using the Xilinx software for writing VHDL Code:

1. Double click on "**Xilinx ISE 9.1i**" icon on the desktop.
2. Click on File- New project.
3. Give a name (preferably same name as the experiment name) and click on next.
4. In the new project wizard select Family as "**Automotive Spartan3**" and simulator "**ISE simulator (VHDL/Verilog)**" and prefer language"**VHDL**". Click on next.
5. Click on "**New source**" and next.
6. Enter the same file name as given in step 3 and select "**VHDL module**" click on next.
7. Enter the port name, direction and bus information given in the VHDLprogram under Entity.

Click on next.

8. After ensuring the port definition clicks on finish if not go back to re-enter the values for step

7 and then click on next.

9. Click on finish to enter the editor window and enter the VHDL code.
10. Save the file and check for syntax (by expanding codes "**synthesize-XST**")
11. Double click on "**Create new source"** and enter the file name. Select"**Test Bench Waveform**" and click on next - next – finish.
12. Select single clock/ combinational under "**clock information**" and clickon finish.
13. Select the inputs as high and low by clicking the mouse on the required inputs and save.
14. Select "**Behavioral simulation**" under sources and select **".tbw file**"
15. Click on process and expand "**Xlinx ISE simulator**" and double click on simulate behavioral module to observe the output waveforms.
16. Use cursor to verify truth table / result

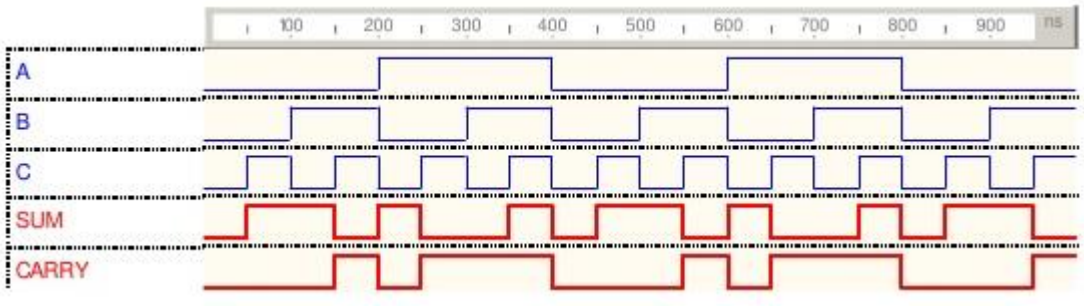
Note: The above steps have to be used for all VHDL simulations.

1) VHDL code for Full adder:

```
 library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_ARITH.ALL;
use IEEE.STD_LOGIC_UNSIGNED.ALL;

entityfull_adder is
    Port (  a : in std_logic;
            b : in std_logic;
            c : in std_logic;
            sum : out std_logic;
            carry : out std_logic);
end full_adder;

architecture behavioural of full_adder is
```

```
begin
sum<= a xor b xor c;
carry<=((a xor b )and c) or (a and b) ;

end behavioural;
```

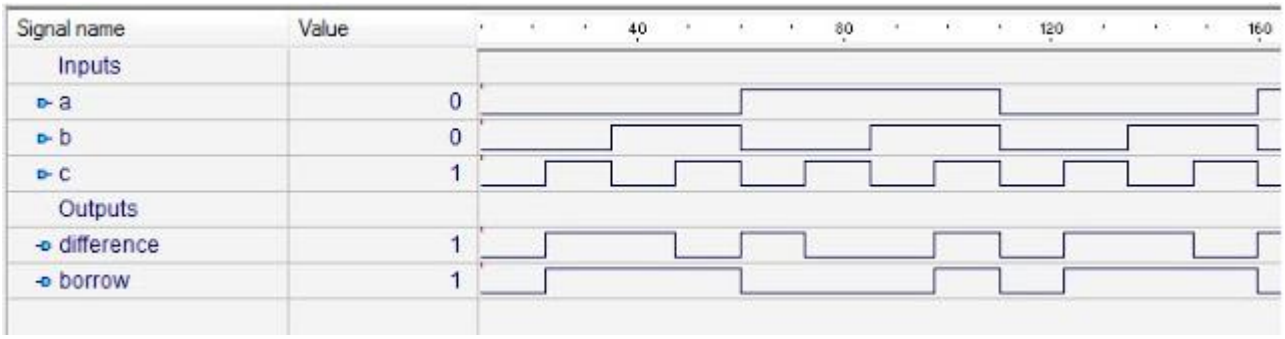
Output waveform:



2)VHDL code for Full Subtractor:

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_ARITH.ALL;
use IEEE.STD_LOGIC_UNSIGNED.ALL;

entity full_subtractor is
    port(
        a : in STD_LOGIC;
        b : in STD_LOGIC;
        c : in STD_LOGIC;
        difference : out STD_LOGIC;
        borrow : out STD_LOGIC);
end full_subtractor;

architecture behavioural of full_subtractor is
begin

   difference <= a xor b xor c;
   borrow <= ((not a) and b) or ((not(a xor b)) and c);

end behavioural;
```

Output Waveform:



OBSERVATIONS

1.) What are the errors encountered in conducting the experiment/compilation?

2.) Measures taken to fix the problem (circuit debug/logical errors)?

3.) Results

ASSIGNMENT

1.) Realize the full adder using 3:8 decoder and verify the behavior.

VIVA QUESTIONS

1.) The full adder realized in this experiment is

a.) 4-bit adder b) 2-bit adder c) 3-bit adder d) 1-bit adder

2.) Draw the block diagram for 3-bit parallel adder.

3.) Write the 2's compliment of the following numbers

a.) 00001111

b.) 01011010

c.) 10111110

4.) Subtract 64 from 89 using 2's compliment addition.

Experiment No. 9

8:1 MULTIPLEXER

Aim: Given a 4-variable logic expression, simplify it using Entered Variable Map and realize the simplified logic expression using 8:1 multiplexer IC

Components/Apparatus required:

1) Multiplexer IC74151.
2) Digital IC Trainer Kit.
3) Patch Chords.

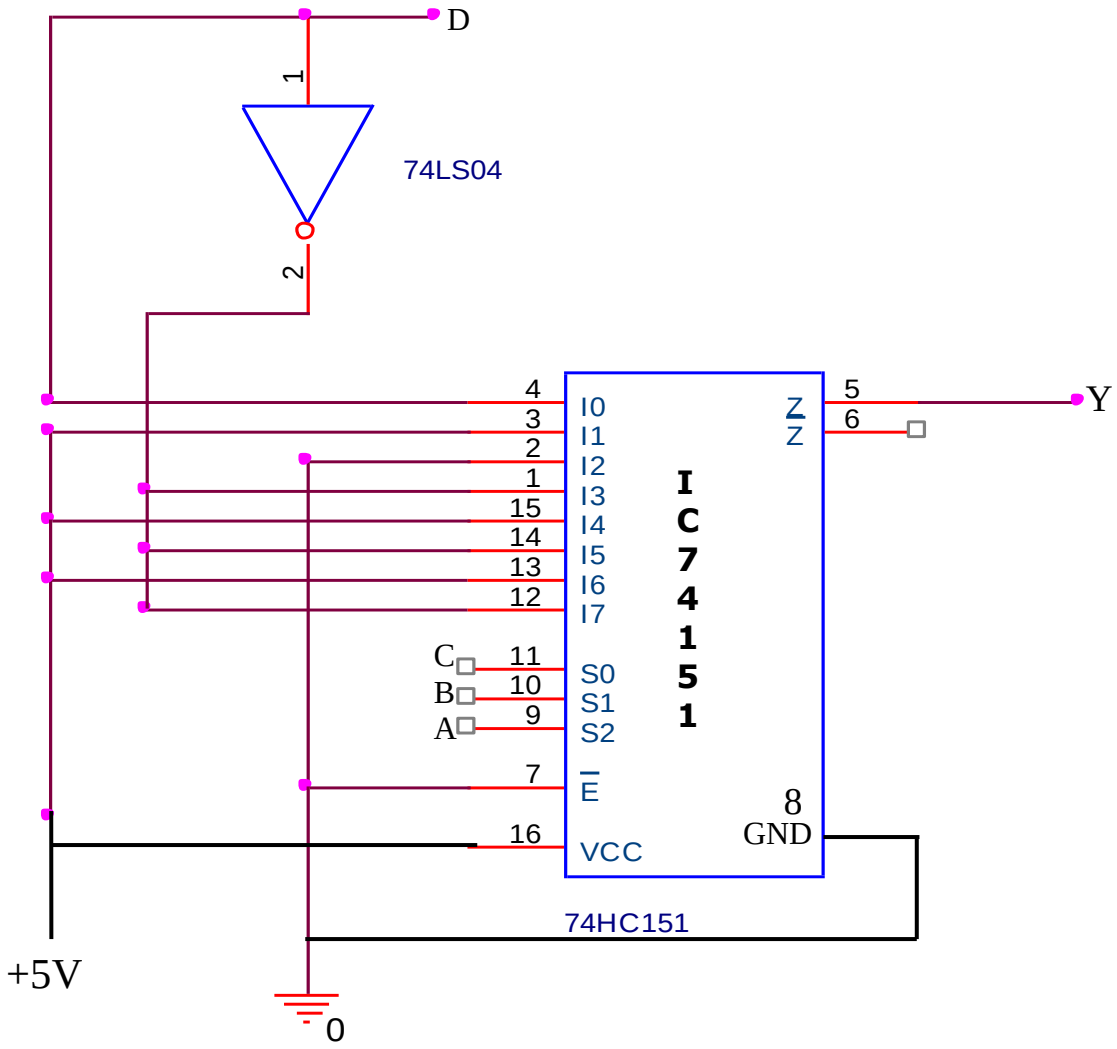
TRUTH TABLE:

A	B	C	D	Y
0	0	0	0	0
0	0	0	1	1
0	0	1	0	1
0	0	1	1	1
0	1	0	0	0
0	1	0	1	0
0	1	1	0	1
0	1	1	1	0
1	0	0	0	1
1	0	0	1	1
1	0	1	0	1
1	0	1	1	0
1	1	0	0	1
1	1	0	1	1
1	1	1	0	1
1	1	1	1	0

IMPLEMENTATION TABLE:

A B C	0 0 0	0 0 1	0 1 0	0 1 1	1 0 0	1 0 1	1 1 0	1 1 1
D = 0	Y = 0	Y = 1	Y = 0	Y = 1	Y = 1	Y = 1	Y = 1	Y = 1
D = 1	Y = 1	Y = 1	Y = 0	Y = 0	Y = 1	Y = 0	Y = 1	Y = 0
Mux I/P	$I_0 = D$	$I_1 = 1$	$I_2 = 0$	$I_3 = \overline{D}$	$I_4 = 1$	$I_5 = \overline{D}$	$I_6 = 1$	$I_7 = \overline{D}$

CIRCUIT DIAGRAM:



PROCEDURE:

1. Convert any given Boolean Expression into Σm( ) notation.
2. Write the Implementation table for the given expression.
3. Find the inputs to be applied to the inputs of the Multiplexer.
4. Make connections as per the implementation table.
5. Apply the inputs using Switches on the Trainer kit and verify the output LEDs on the Trainer kit.
6. Verify the truth table

Experiment No. 10

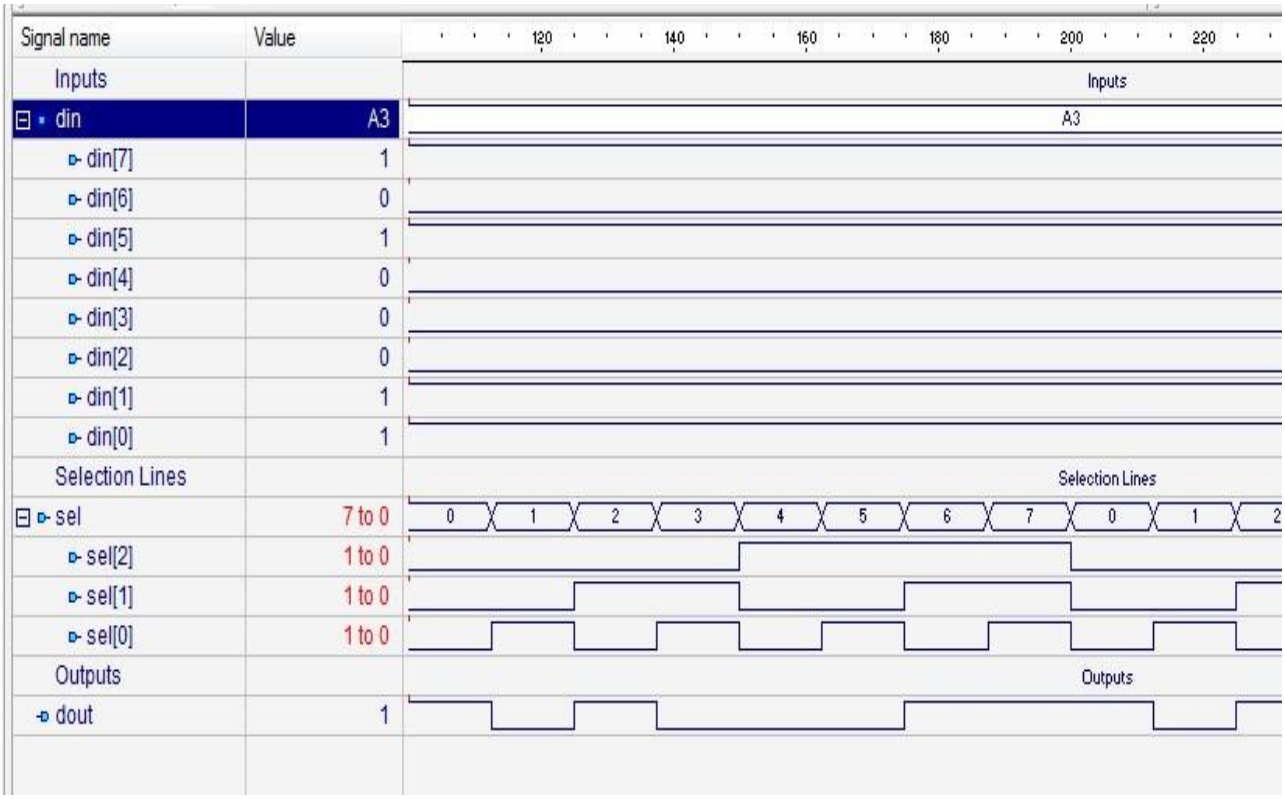
VHDL CODE FOR AN 8:1 MULTIPLEXER

Aim: Design and develop the VHDL code for an 8:1 multiplexer. Simulate and verify it's working.

VHDL code for 8:1 MUX

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_ARITH.ALL;
use IEEE.STD_LOGIC_UNSIGNED.ALL;

entity mux8to1 is
                Port ( sel : in  STD_LOGIC_vector(2 downto 0);
                din : in  STD_LOGIC_vector(7 downto 0);
                dout : out  STD_LOGIC);
end mux8to1;

architecture Behavioral of mux8to1 is
begin
        process(sel,din(7), din(6), din(5), din(4), din(3), din(2), din(1), din(0))

begin
        case sel is

        when "000"=>dout<=din(7);
        when "001"=>dout<= din(6);
        when "010"=>dout<= din(5);
        when "011"=>dout<= din(4);
        when "100"=>dout<= din(3);
        when "101"=>dout<= din(2);
        when "110"=>dout<= din(1);
        when "111"=>dout<= din(0);
        when others=>null;

end case;

end process;

end Behavioral;
```

Output waveform:



OBSERVATIONS

1.) What are the errors encountered in conducting the experiment/compilation?

2.) Measures taken to fix the problem(circuit debug/logical errors)

3.) Results

ASSIGNMENT

1.) Realize the Boolean Expression Y= πM(1,2,3,6,8,9,10,12,13,14) using 8:1 Multiplexer IC

VIVA QUESTIONS

1.) Draw the block diagram of a 4:1 multiplexer and a 2:1 multiplexer.

2.) Realize a 8:1 multiplexer using two 4:1 multiplexer and a 2:1 multiplexer.

3.) A circuit with many inputs and only one output is called a _____

4.) Write a VHDL code for 4:1 multiplexer.

Experiment No. 11

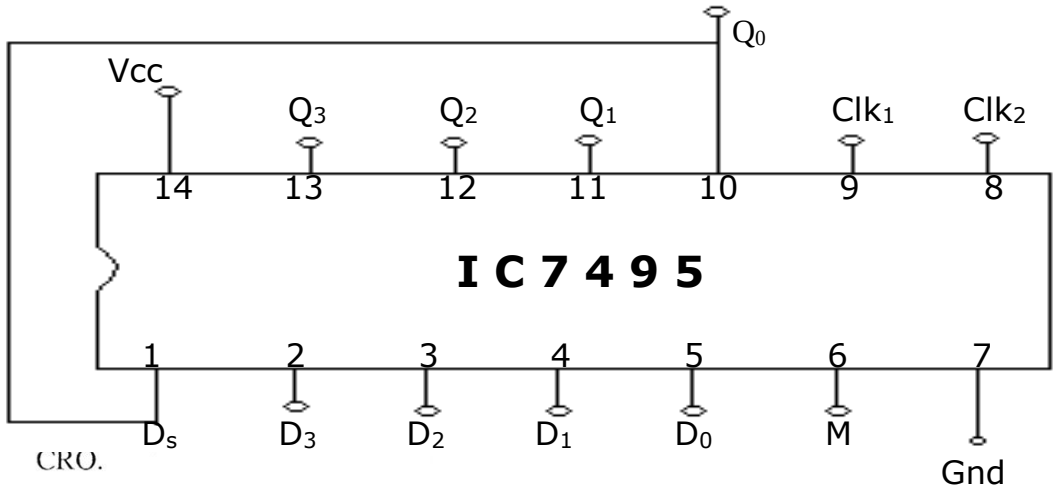
RING COUNTER

Aim: Design and implement a ring counter using 4-bit shift register and demonstrate its working.

Components/Apparatus required:

1) Shift Register IC 7495
2) Digital IC Trainer Kit
3) Patch Chords

CIRCUIT DIAGRAM:



Procedure:

1. Mode control is made 1.
2. Parallel inputs say 0001 are given to D_3 D_2 D_1 D_0 inputs of 7495 respectively
3. Clock 2 is pulsed once. Now D_3 D_2 D_1 D_0 parallel inputs appears on Q_3 Q_2 Q_1 Q_0 lines.
4. Clock 1 of 7495 is connected to the pulser.
5. Now mode control is made '0'.
6. When clock pulses are applied this '1' circulates around the circuit as shown.

Clock	Time	Outputs Q_3	Q_2	Q_1	Q_0
Clock 2	t_0 (Starting state)	0	0	0	1
Clock 1	t_1 (After 1st clock pulse)	1	0	0	0
	t_2 (After 2nd clock pulse)	0	1	0	0
	t_3 (After 3rd clock pulse)	0	0	1	0
	t_4 (After 4th clock pulse)	0	0	0	1

Experiment No. 12

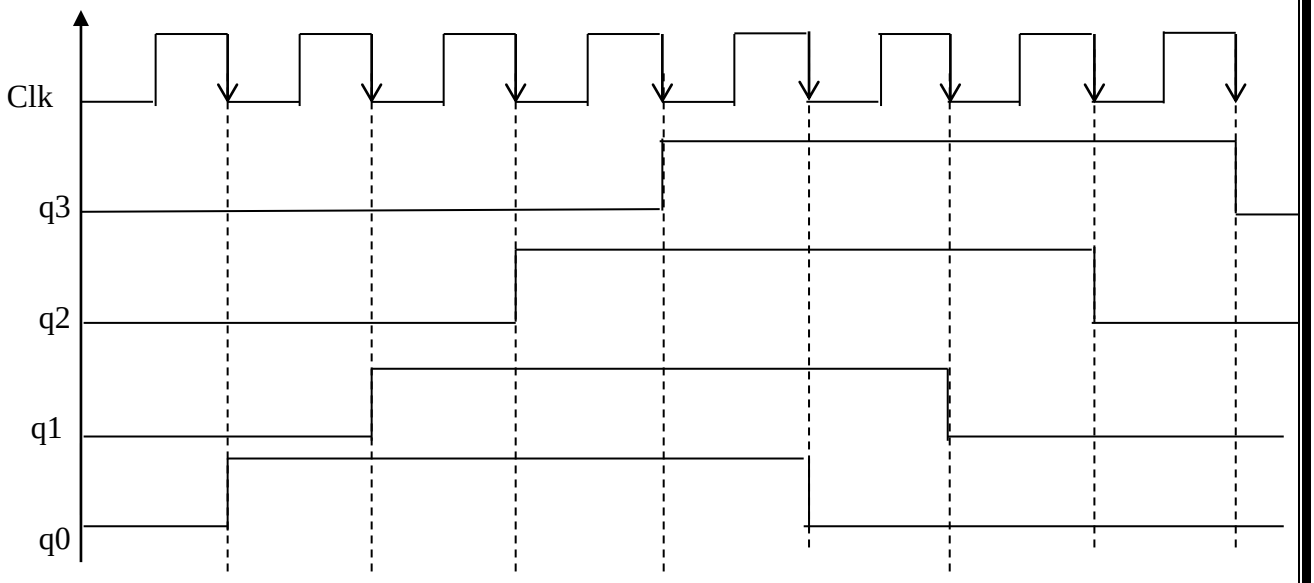
VHDL code for switched tail counter

Aim: Design and develop the Verilog / VHDL code for switched tail counter.

VHDL code

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_ARITH.ALL;
use IEEE.STD_LOGIC_UNSIGNED.ALL;

entity johnson is
        Port ( clk : in  STD_LOGIC;
                q :inout  STD_LOGIC_VECTOR (3 to 0) :="0000");
end johnson;

architecture Behavioral of johnson is

begin
        process(clk)
begin
        if(clk'event and clk='0') then
        q(3)<= not(q(0));
        for i in 3 downto 1 loop
        q(i-1)<= q(i);

        end loop;
        end if;
        end process;

end Behavioral;
```

WAVEFORM:



Procedure: Follow the steps given for simulation of experiment 1b.

OBSERVATIONS

1.) What are the errors encountered in conducting the experiment/compilation?

2.) Measures taken to fix the problem (circuit debug/logical errors)

3.) Results

ASSIGNMENTS

1.) Modify the above ring counter circuit to Johnson counter.

2.) Modify the above VHDL code for a ring counter.

VIVA QUESTIONS

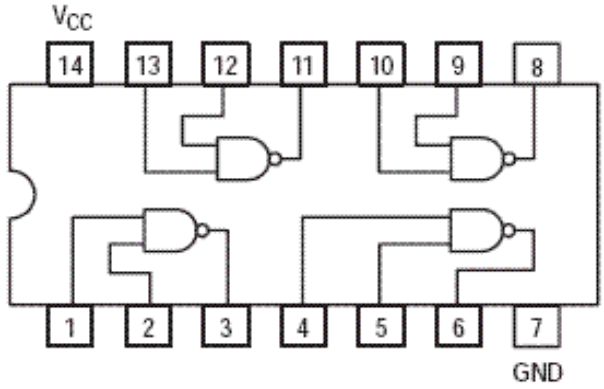
1.) List the difference between ring counter and Johnson counter.

2.) List the different type of shift register.

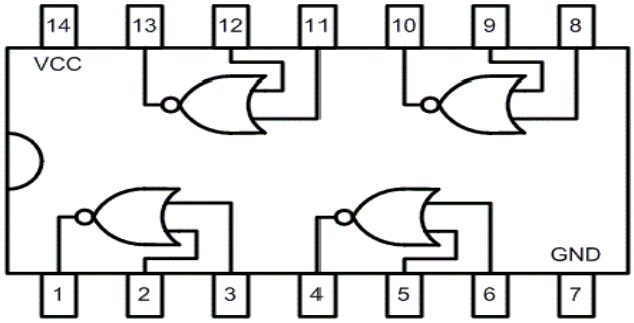
3.) Draw the circuit of a 3-bit ring counter using JK-flip flop.

IC Pin Configuration Sheet:

IC 7400 2 I/P NAND GATE

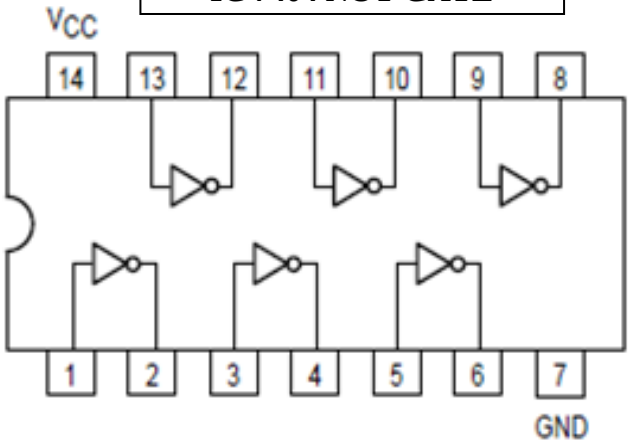


IC 7402 2 I/P NOR GATE

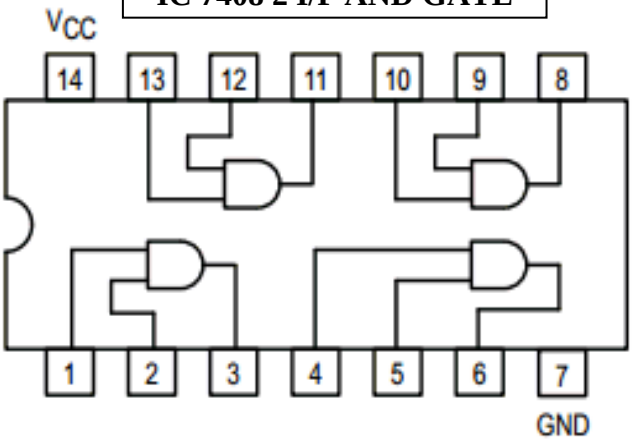


7402 Quad 2 Input NOR

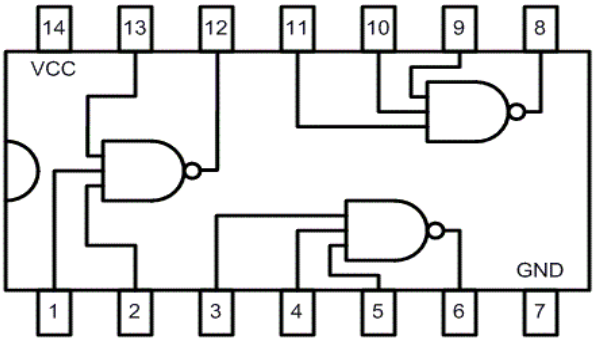
IC 7404 NOT GATE



IC 7408 2 I/P AND GATE

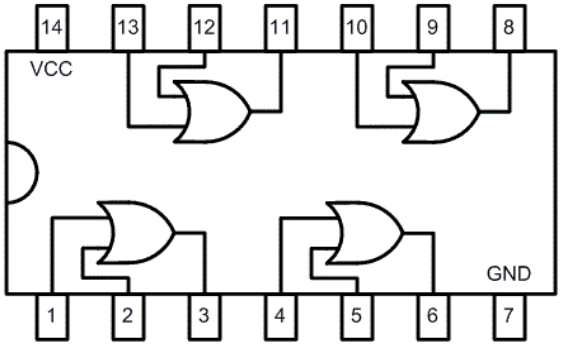


IC 7410 3 I/P NAND GATE



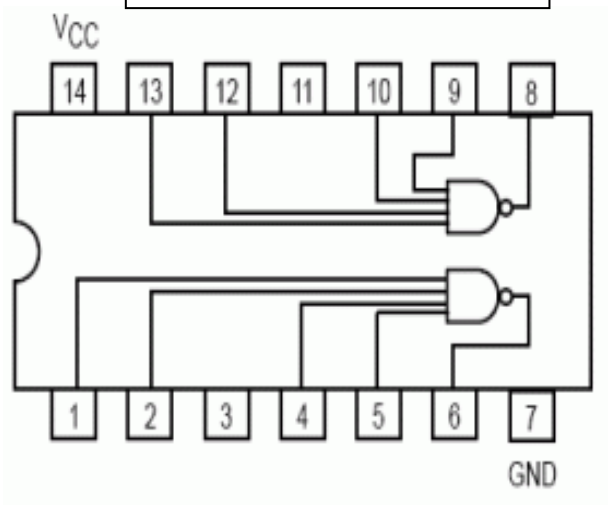
7410 Triple 3 Input NAND

IC 7432 2 I/P OR GATE

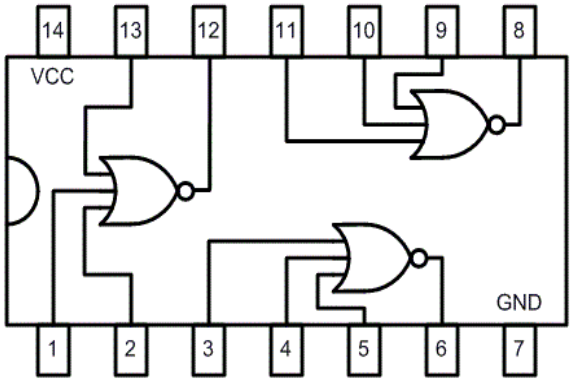


7432 Quad 2 Input OR

IC 7420 4 I/P NAND GATE

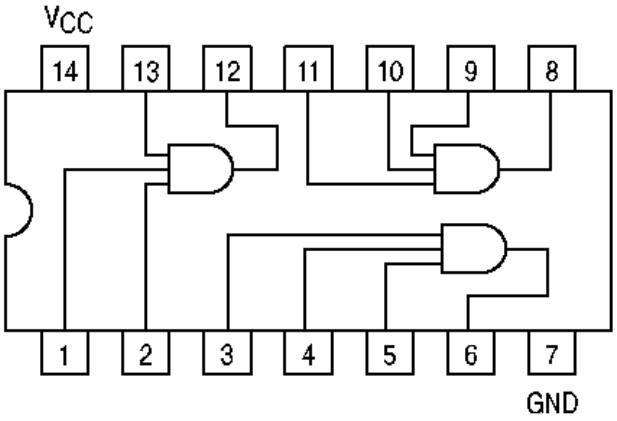


IC 7427 3 I/P NOR GATE

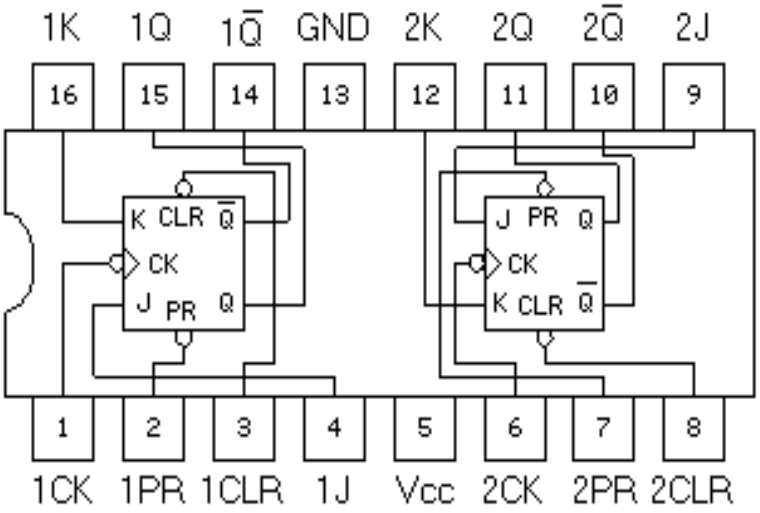


7427 Triple 3 Input NOR

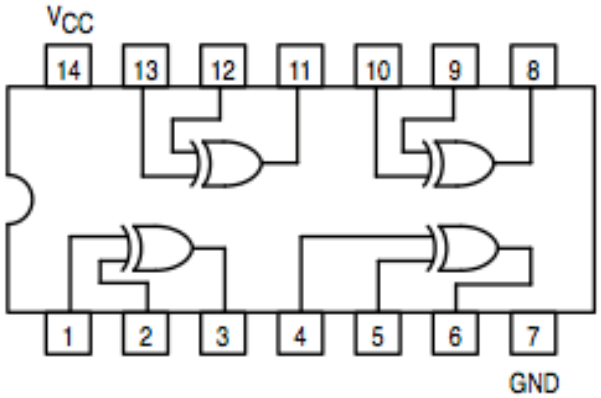
IC 7411 3 I/P AND GATE



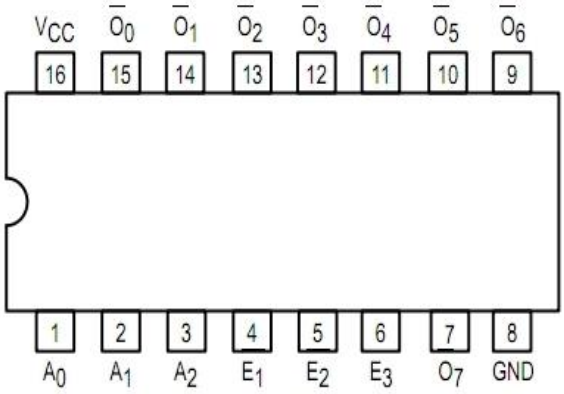
IC 7476 JK FLIP FLOP



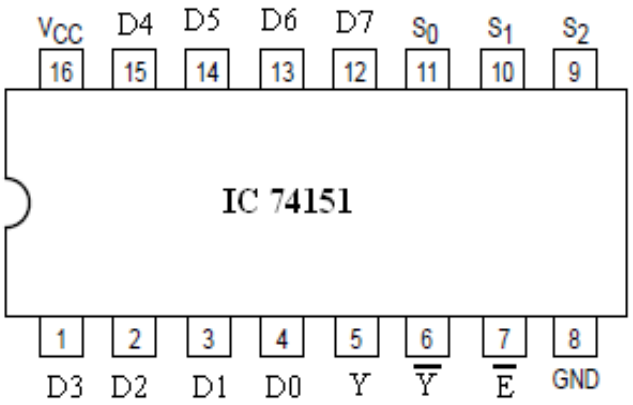
IC 7486 2 I/P EXOR GATE



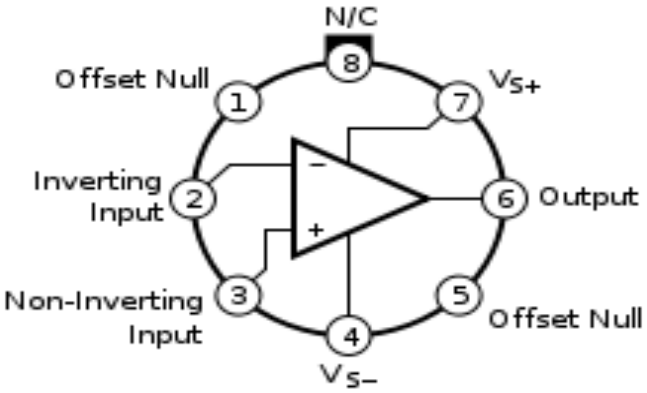
IC 74138 Decoder



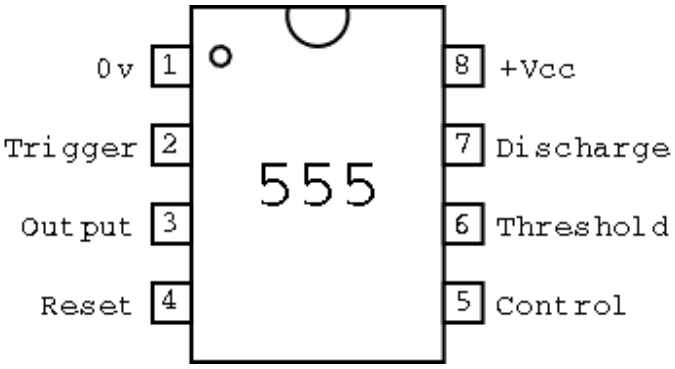
IC 74151 8:1 Mux



IC uA741 OPAMP



IC 555 Timer



Components names of Analog Circuits

Sl.No	Component Name	Library	Part Code
1	Resistor	Analog	R
2	Capacitor	Analog	C
3	Sine wave	Source	Vsin
4	DC supply	Source	Vdc
5	Opamp	Opamp	uA741
6	Diode	Diode	D1N4007
7	Transistor	Bipolar	Q2N2222
8	Voltage Regulator	Opamp	LM7805C
9	Ground		GND(0/Source)