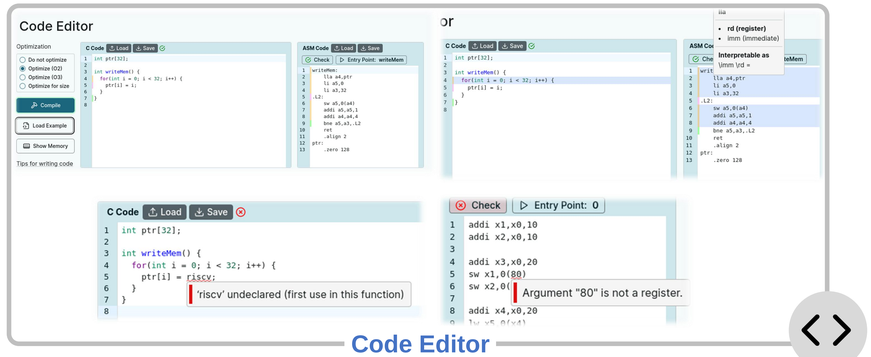
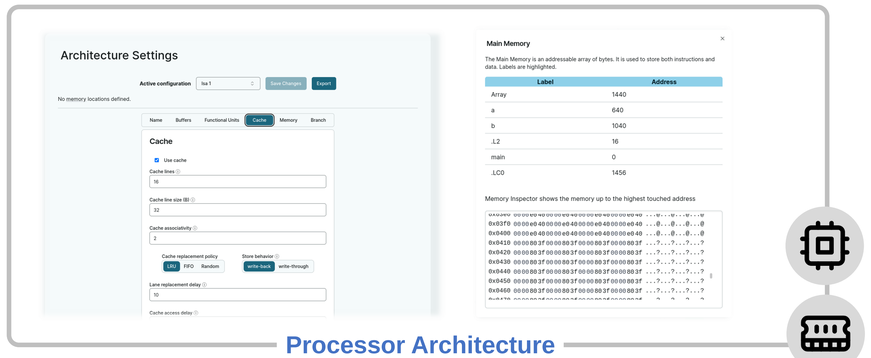
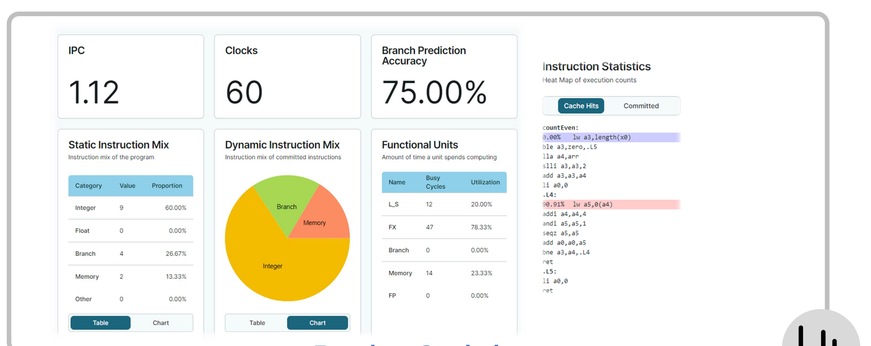
Web-Based Simulator of Superscalar RISC-V Processors

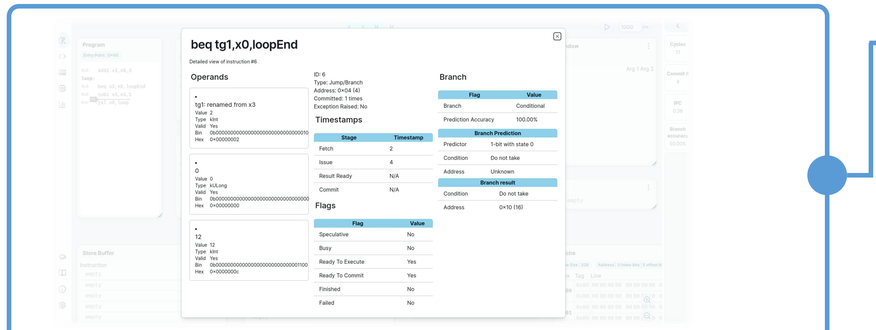
Jiri Jaros, Michal Majer, Jakub Horky and Jan Vavra

Brno University of Technology, Faculty of Information Technology, Brno, CZ









1 Motivation and Goals

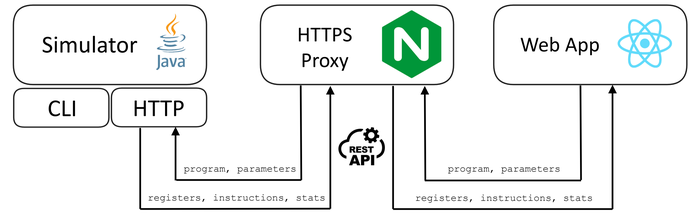
Mastering computational architectures is key to developing efficient programs. Our web-based simulator helps IT students and professionals understand superscalar processors and HW-SW co-design. With customizable architecture, C compiler support, and performance stats, users can explore RISC-V processor pipelines, identify bottlenecks, and see how algorithm implementations affect execution time, cost, and power. Currently supporting RV32IMFD instruction set, future updates will include 64-bit and vector extensions, providing an accessible tool for optimizing algorithms and preparing developers for modern computing challenges.

2 Feature Highlights

- **User-Friendly Interface**: Simple and illustrative web presentation with detailed information on each block and instruction.
- **Fully Configurable Processors**: Customize issue width, register files, reorder, load and store buffers, branch predictors, functional and memory units, along with cache memory settings including size, associativity, cache line size, and replacement strategy.
- **Forward and Backward Simulation**: Flexibility to simulate in both directions for thorough analysis.
- **GCC Compiler Interface**: Build C code into assembly using various optimization levels with syntax highlighting and pairing between C and assembly code.
- **Comprehensive Performance Statistics**: Access static and dynamic metrics such as FLOPs, IPC, branch prediction accuracy, unit utilization and cache hit rate.
- **Benchmark CLI**: Command-line interface for benchmarking complex programs.

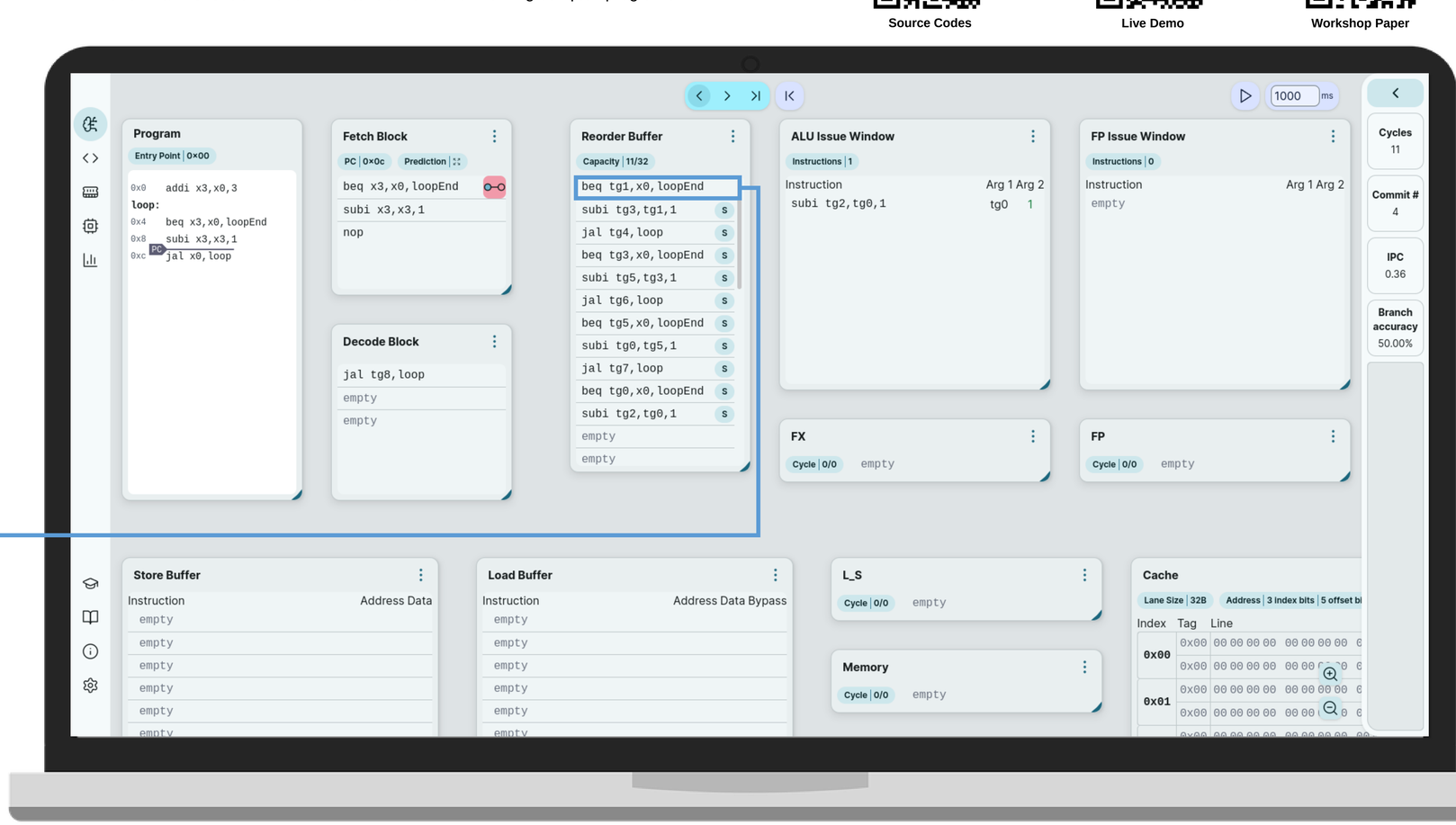
3 Implementation, Testing and Deployment

- **Fully Containerized Solution**: Implemented in Docker for seamless deployment and scalability.
- **Extensive Static Unit Testing**: Achieves 83% code coverage.
- **Robust Dynamic Testing**: Supports 100 concurrent users with a median latency under 1.2 seconds on an Intel i5-8300 laptop with 16GB RAM.



4 Source Codes, Live Demo and SC 24 Workshop Paper

Source Codes | Live Demo | Workshop Paper



We are proud to have achieved this magnificent results through our own resources and efforts without relying on any external funding. This presentation was supported by Brno University of Technology under project FIT-S-23-8141.