ARM based Microcontrollers & Peripherals

IEEE SSCS Alexandria Student Chapter

Agenda

1. Overview on ARM architecture
2. ARM Cortex-M4 and ARM Cortex-M3 Specifications
3. TM4C123GH6PM Microcontroller Peripherals.
4. TIVA TM4C123GH6PM Launchpad kit specifications
5. GPIO Interface with applications
6. Interrupts and exceptions of TM4C123GH6PM.
7. DMA and its applications.
8. UART Interface.
9. SPI Interface with applications.
10. I2C Interface with applications.
11. ADC Interface with applications
12. Timers and PWM interfacing .

Outline

- The point consists of the following topics:
  - The Cortex-M Processor family
  - The Cortex-M3 and Cortex-M4 processors features
  - Cortex-M4 block diagram
  - Cortex-M4 Architecture
  - Cortex-M4 Exceptions and interrupts

The Cortex-M Processor family

- For general data processing and I/O control tasks, the Cortex-M0 and Cortex-M0þ processors have excellent energy efficiency
- But for applications with complex data processing requirements, they may take more instructions and clock cycles.

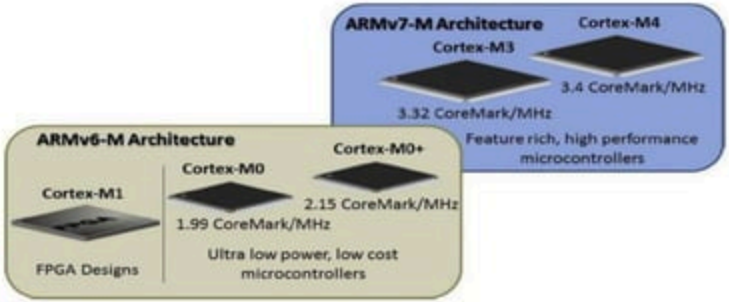


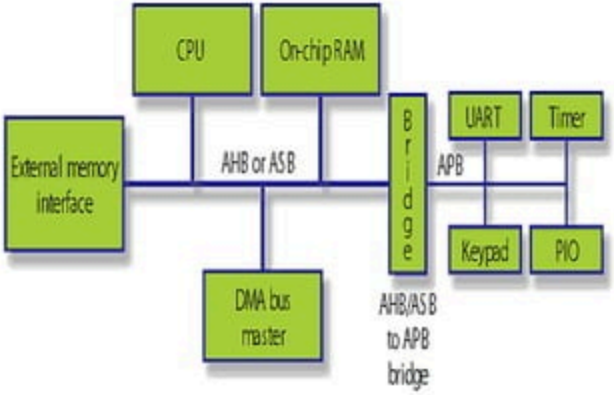
FIGURE 1.1
The Cortex-M processor family

The Cortex-M3 and Cortex-M4 processors features

- Cortex-M3 was released in 2005 and Cortex – M4 was released in 2010.
- 32-bit registers
- 32-bit internal data path
- 32-bit bus interface
- The Instruction Set Architecture (ISA) is called Thumb ISA.
- Three-stage pipeline design
- Harvard bus architecture with unified memory space: instructions and data use the same address space
- 32-bit addressing, supporting 4GB of memory space.

The Cortex-M3 and Cortex-M4 processors features

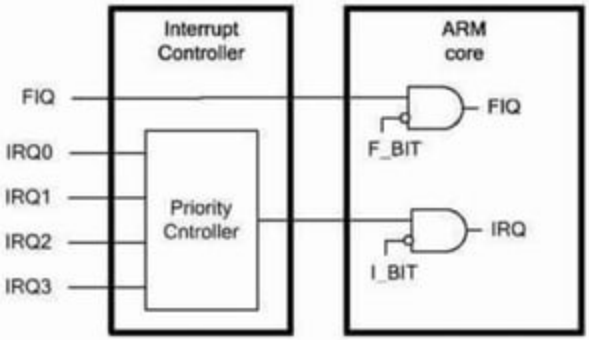
- On-chip bus interfaces based on ARM AMBA (Advanced Microcontroller Bus Architecture)Technology, which allow pipelined bus operations for higher throughput



AHB	ASB	APB
High performance	High performance	Low power
Pipelined operation	Pipelined operation	Latched address and control
Multiple bus masters	Multiple bus masters	Simple interface
It consists of master, slave, arbiter decoder	It consists of master, slave, arbiter decoder	It consist of APB bridge and slave

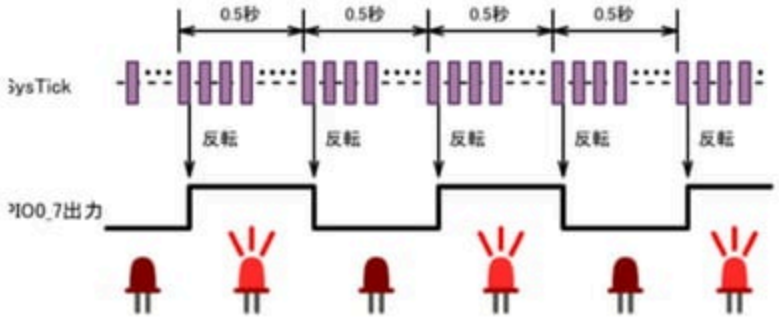
The Cortex-M3 and Cortex-M4 processors features

- An interrupt controller called NVIC (Nested Vectored Interrupt Controller)
- supporting up to 240 interrupt requests and from 8 to 256 interrupt priority levels (dependent on the actual device implementation)



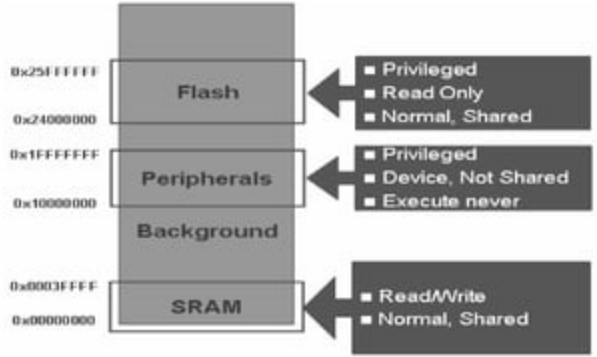
The Cortex-M3 and Cortex-M4 processors features

- • Support for various features for OS (Operating System) implementation such as a system tick timer, shadowed stack pointer



The Cortex-M3 and Cortex-M4 processors features

- Sleep mode support and various low power features.
- Support for an optional MPU (Memory Protection Unit) to provide memory protection features like programmable memory, or access permission control.



Cortex-M4 block diagram

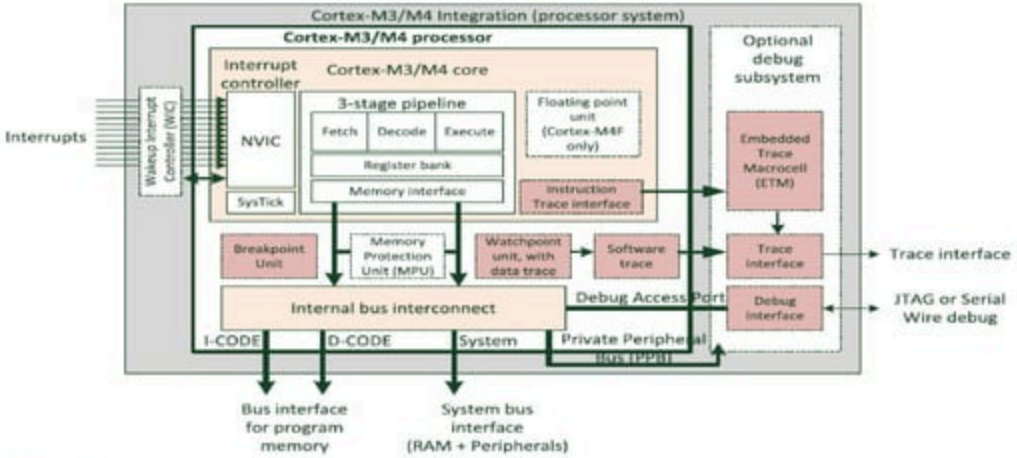


FIGURE 3.3

Block diagram of the Cortex-M3 and Cortex-M4 processor

Cortex-M4 Architecture

- **Programmer model**

The processors can have privileged and unprivileged access levels:

- Privileged access level can access all resources in the processor.
- Unprivileged access level means some memory regions are inaccessible, and a few operations cannot be used.

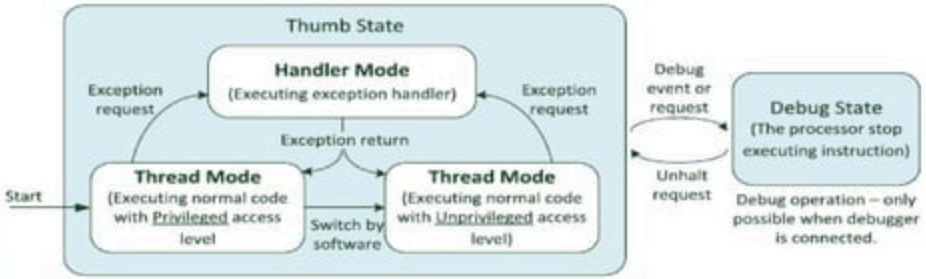
- The separation of privileged and unprivileged access levels allows system designers to develop robust embedded systems.

Cortex-M4 Architecture

- **Programmer model**

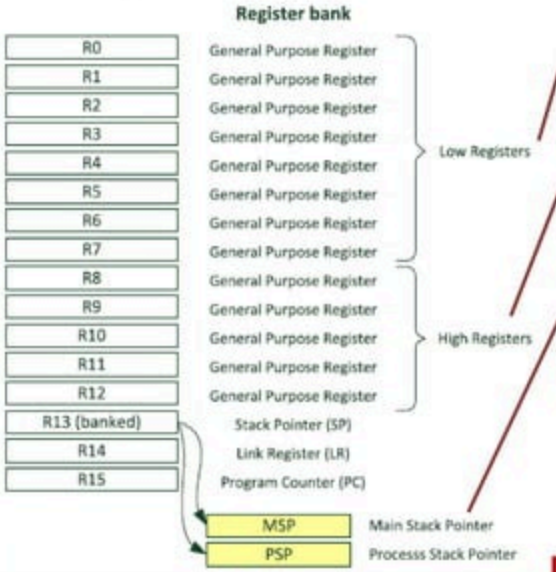
The processor is also has two operational states:

- Debug state: When the processor is halted (e.g., by the debugger, or after hitting a breakpoint), it enters debug state and stops executing instructions.
- Thumb state: If the processor is running program code (Thumb), it is in the Thumb state.



Cortex-M4 Architecture

- Register file



Due to the limited available space in the instruction set, many 16-bit instructions can only access the low registers.

can be used with 32-bit instructions, and a few with 16-bit instructions

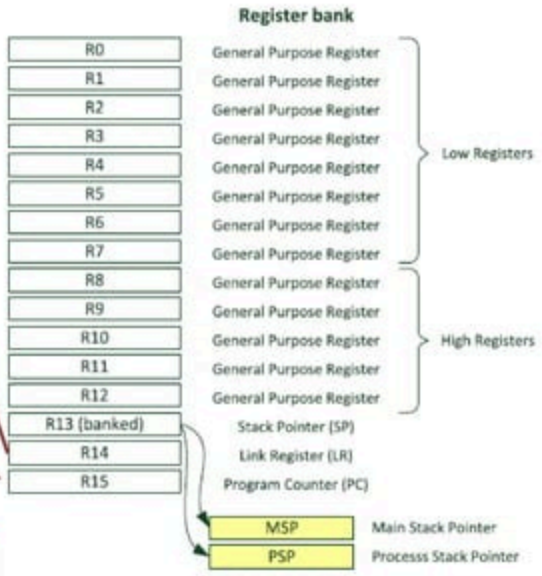
MSP is the default Stack Pointer.
It is selected after reset, or when the processor is in Handler Mode.
PSP can only be used in Thread Mode.
The PSP is normally used when an embedded OS is involved, where the stack for the OS kernel and application tasks are separated.

Cortex-M4 Architecture

- Register file

Link Register (LR) is used for holding the return address when calling a function or subroutine.
At the end of the function or subroutine, the program control can return to the calling program and resume by loading the value of LR into the Program Counter (PC).

Program Counter (PC) is readable and writeable: a read returns the current instruction address plus 4. Writing to PC causes a branch operation.



Cortex-M4 Architecture

- **Instruction Set:**
- Classic ARM processors were supporting both ARM-32 bit Instructions and Thum16 bit instructions

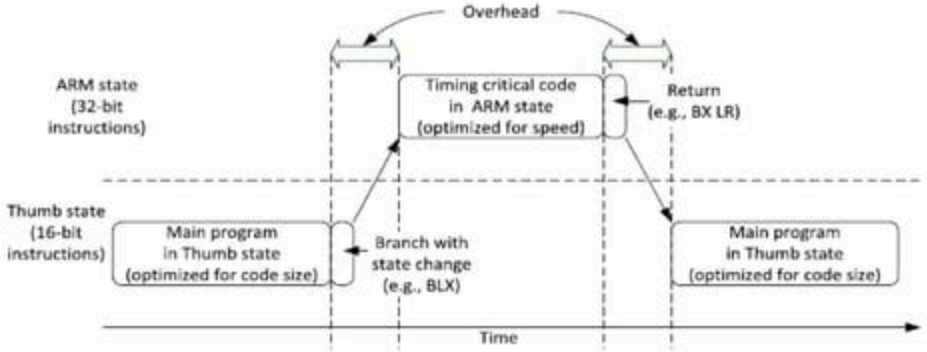


FIGURE 3.1

Switching between ARM code and Thumb code in class ARM processors such as the ARM7TDMI

Cortex-M4 Architecture

- **Instruction Set:**
- ARM Cortex Instruction set introduced Thumb-2 technology, the Thumb instruction set has been extended to support both 16-bit and 32-bit instruction encoding.

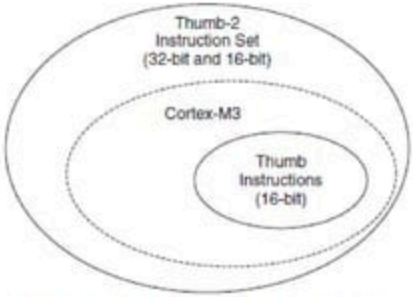


Figure 1.4 The Relationship Between the Thumb-2 Instruction Set and the Thumb Instruction Set

Cortex-M4 Architecture

- **Instruction Set:**
- With Thumb-2 technology, the Cortex-M processor has a number of advantages over classic ARM processors:

1. No state switching overhead, saving both execution time and instruction space.
2. No need to specify ARM state or Thumb state in source files, making software development easier.
3. It is easier to get the best code density, efficiency, and performance at the same time.
4. With Thumb-2 technology, the Thumb instruction set has been extended by a wide margin when compared to a classic processor

Cortex-M4 Architecture

- **Memory System**
- The Cortex-M3 and M4 processors themselves do not include memories.
- they come with a generic on-chip bus interface.
- the microcontroller vendor will need to add the following items to the memory system:

1. Program memory, typically flash
2. Data memory, typically SRAM
3. Peripherals

Cortex-M4 Architecture

- **Memory System**
- The provided bus interfaces on the Cortex-M processors are 32-bit, and based on the Advanced Microcontroller Bus Architecture (AMBA) standard.

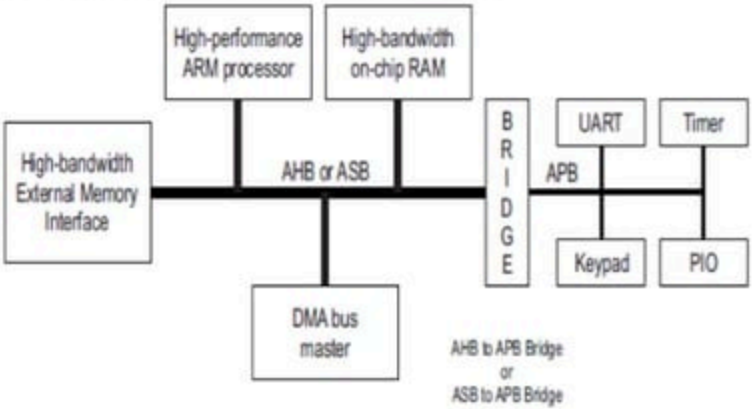
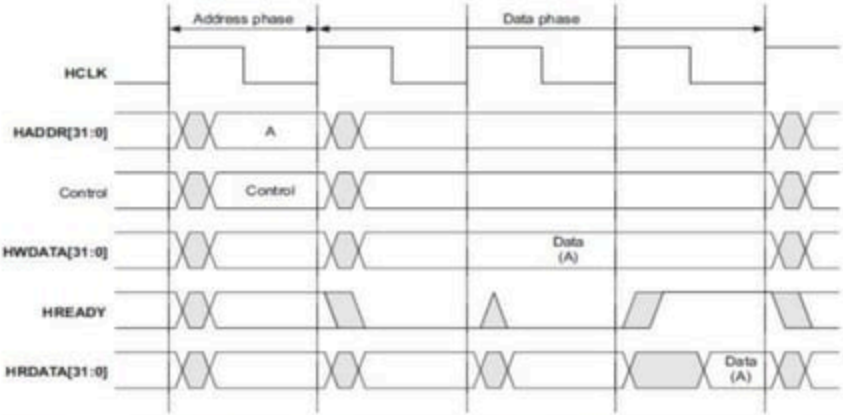


Fig. 1. AMBA based Simple Microcontroller

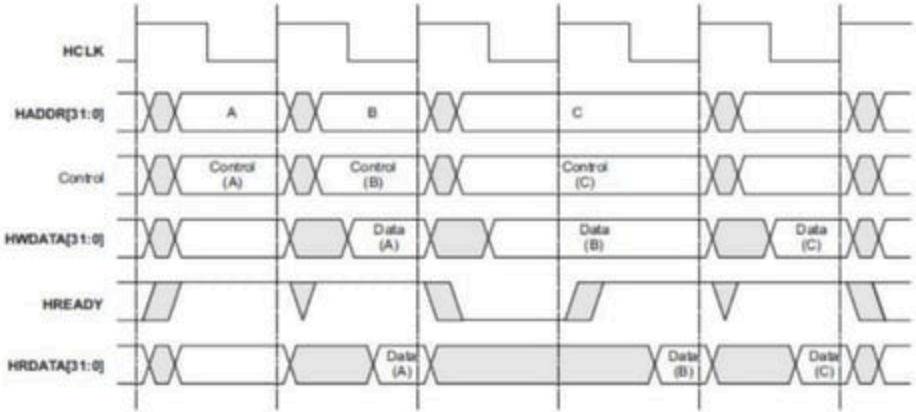
Cortex-M4 Architecture

- **Memory System**
- AHB Bus transfer:
  - **Transfer with wait states**



Cortex-M4 Architecture

- **Memory System**
- AHB Bus transfer:
  - Multiple Transfer



Cortex-M4 Architecture

- **Memory System**
- **What is Bit Banding?**

Bit Banding is a method of performing atomic bitwise modifications to memory.

- **Why Bit banding?**

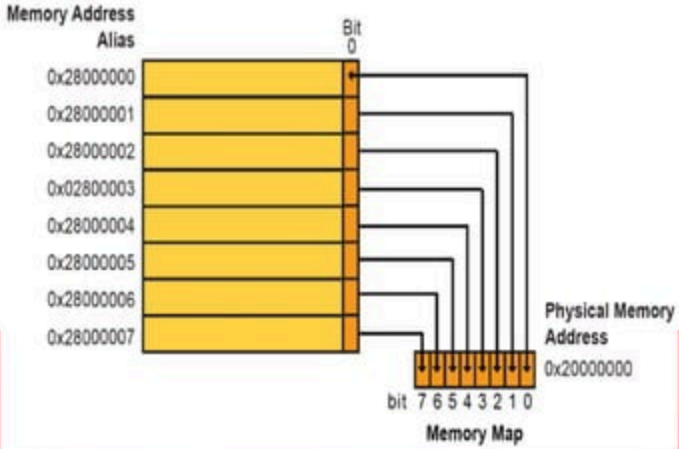
Usually changing a word in memory requires a read-modify-write cycle. If this operation is interrupted there can be data loss.

Read (0xaa) from A to register
Interrupt!
Write (0x33) to A
Return!
Modify (0xaa to 0xab)
Write (0xab) to A

(0x33) data has been lost!

Cortex-M4 Architecture

- **Memory System**
- **How is Bit Banding Working?**
- Bit-banding uses address space that aliases peripheral or SRAM address space, allowing a single bit within a word to be manipulated by a reference to a byte at an aliased address.



Cortex-M4 Architecture

- **Memory System**
- **Bit Banding in ARM Cortex-M4?**
- **SRAM Bit banding and alias regions**

Address Range		Memory Region	Instruction and Data Accesses
Start	End		
0x2000.0000	0x2000.7FFF	SRAM bit-band region	Direct accesses to this memory range behave as SRAM memory accesses, but this region is also bit addressable through bit-band alias.

Address Range		Memory Region	Instruction and Data Accesses
Start	End		
0x2200.0000	0x220F.FFFF	SRAM bit-band alias	Data accesses to this region are remapped to bit band region. A write operation is performed as read-modify-write. Instruction accesses are not remapped.

Cortex-M4 Architecture

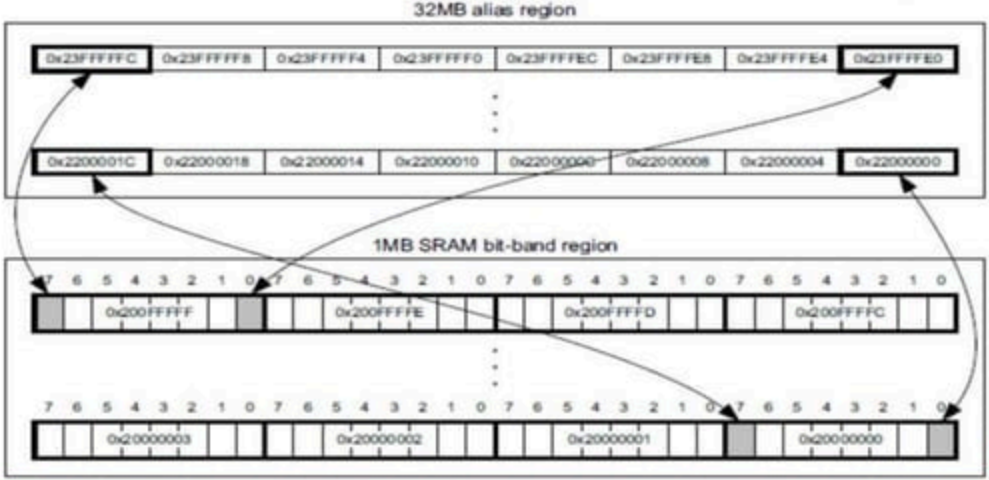
- **Memory System**
- **Bit Banding in ARM Cortex-M4?**
- **Peripheral memory Bit banding and alias regions**

Address Range		Memory Region	Instruction and Data Accesses
Start	End		
0x4000.0000	0x400F.FFFF	Peripheral bit-band region	Direct accesses to this memory range behave as peripheral memory accesses, but this region is also bit addressable through bit-band alias.
0x4200.0000	0x43FF.FFFF	Peripheral bit-band alias	Data accesses to this region are remapped to bit band region. A write operation is performed as read-modify-write. Instruction accesses are not permitted.

Cortex-M4 Architecture

- **Memory System**
- **Bit Banding in ARM Cortex-M4?**

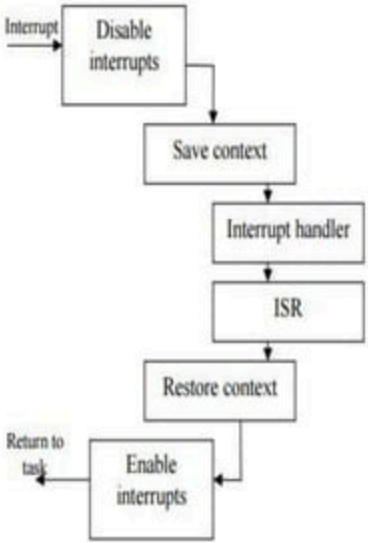
How Alias word address calculated to modify a single bit?



alias_word_address =
alias_region_base + bit_band_byte_offset x 32) + (bit_number x 4)

Cortex-M4 Architecture

- **Exceptions and interrupt control**
- Exceptions are events that cause changes to program flow.
- When one happens, the processor suspends the current executing task and executes a part of the program called the exception handler.
- After the execution of the exception handler is completed, the processor then resumes normal program execution.



Cortex-M4 Architecture

- **Exceptions and interrupt control**
- Nested Interrupt Vector Controller. (NIVC)
- The NVIC handles the exceptions and interrupt configurations, prioritization, and interrupt masking.
- The NVIC has the following features:

1. Flexible exception and interrupt management
2. Nested exception/interrupt support.
3. Vectored exception/interrupt entry.
4. Interrupt masking.

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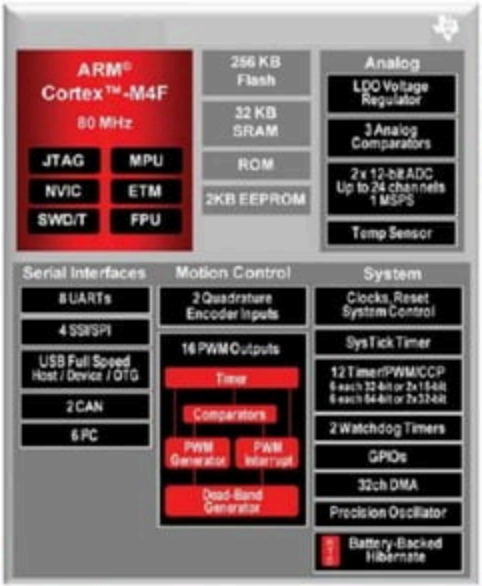
TM4C123GH6PM Microcontroller Overview

Microcontroller Features



Low power consumption

- As low as 370 µA/MHz
- 500µs wakeup from low-power modes
- RTC currents as low as 1.7µA
- Internal and external power control

TM4C123GH6PM Microcontroller Overview

Microcontroller Features

M4 Core and Floating-Point Unit

- 32-bit ARM® Cortex™-M4 core
- Thumb2 16/32-bit code: 26% less memory & 25 % faster than pure 32-bit
- System clock frequency up to 80 MHz
- 100 DMIPS @ 80MHz
- Flexible clocking system
  - Internal precision oscillator
  - External main oscillator with PLL support
  - Internal low frequency oscillator
  - Real-time-clock through Hibernation module
- Saturated math for signal processing
- Atomic bit manipulation. Read-Modify-Write using bit-banding
- Single Cycle multiply and hardware divider
- Unaligned data access for more efficient memory usage
- IEEE754 compliant single-precision floating-point unit
- JTW and Serial Wire Debug debugger access
  - ETM (Embedded Trace Macrocell) available through Keil and IAR emulators

TM4C123GH6PM Microcontroller Overview

Microcontroller Features

TM4C123GH6PM Memory

256KB Flash memory

- Single-cycle to 40MHz
- Pre-fetch buffer and speculative branch improves performance above 40 MHz

32KB single-cycle SRAM with bit-banding

Internal ROM loaded with TivaWare software

- Peripheral Driver Library
- Boot Loader
- Advanced Encryption Standard (AES) cryptography tables
- Cyclic Redundancy Check (CRC) error detection functionality

2KB EEPROM (fast, saves board space)

- Wear-leveled 500K program/erase cycles
- Thirty-two 16-word blocks
- Can be bulk or block erased
- 10 year data retention
- 4 clock cycle read time

0x00000000 Flash
0x01000000 ROM
0x20000000 SRAM
0x22000000 Bit-banded SRAM
0x40000000 Peripherals & EEPROM
0x42000000 Bit-banded Peripherals
0xE0000000 Instrumentation, ETM, etc.

TM4C123GH6PM Microcontroller Overview

Microcontroller Features

TM4C123GH6PM Peripherals

Battery-backed Hibernation Module

- Internal and external power control (through external voltage regulator)
- Separate real-time clock (RTC) and power source
- VDD3ON mode retains GPIO states and settings
- Wake on RTC or Wake pin
- Sixteen 32-bit words of battery backed memory
- 5 µA Hibernate current with GPIO retention. 1.7 µA without

Serial Connectivity

- USB 2.0 (OTG/Host/Device)
- 8 - UART with IrDA, 9-bit and ISO7816 support
- 6 - I²C
- 4 - SPI, Microwire or TI synchronous serial interfaces
- 2 - CAN

TM4C123GH6PM Microcontroller Overview

Microcontroller Features

TM4C123GH6PM Peripherals

Two 1MSPS 12-bit SAR ADCs

- Twelve shared inputs
- Single ended and differential measurement
- Internal temperature sensor
- 4 programmable sample sequencers
- Flexible trigger control: SW, Timers, Analog comparators, GPIO
- VDDA/GNDA voltage reference
- Optional hardware averaging
- 3 analog and 16 digital comparators
- µDMA enabled

0 - 43 GPIO

- Any GPIO can be an external edge or level triggered interrupt
- Can initiate an ADC sample sequence or µDMA transfer directly
- Toggle rate up to the CPU clock speed on the Advanced High-Performance Bus
- 5-V-tolerant in input configuration (except for PB0/1 and USB data pins when configured as GPIO)
- Programmable Drive Strength (2, 4, 8 mA or 8 mA with slew rate control)
- Programmable weak pull-up, pull-down, and open drain

TM4C123GH6PM Microcontroller Overview

Microcontroller Features

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TM4C123GH6PM Microcontroller Overview

Microcontroller Features

TM4C123GH6PM Peripherals

Memory Protection Unit (MPU)

- Generates a Memory Management Fault on incorrect access to region

Timers

- 2 Watchdog timers with separate clocks
- SysTick timer. 24-bit high speed RTOS and other timer
- Six 32-bit and Six 64-bit general purpose timers
- PWM and CCP modes
- Daisy chaining
- User enabled stalling on CPU Halt flag from debugger for all timers

32 channel µDMA

- Basic, Ping-pong and scatter-gather modes
- Two priority levels
- 8,16 and 32-bit data sizes
- Interrupt enabled

TM4C123GH6PM Microcontroller Overview

Microcontroller Features

TM4C123GH6PM Peripherals

Nested-Vectored Interrupt Controller (NVIC)

- 7 exceptions and 71 interrupts with 8 programmable priority levels
- Tail-chaining and other low-latency features
- Deterministic: always 12 cycles or 6 with tail-chaining
- Automatic system save and restore

Two Motion Control modules. Each with:

- 8 high-resolution PWM outputs (4 pairs)
- H-bridge dead-band generators and hardware polarity control
- Fault input for low-latency shutdown
- Quadrature Encoder Inputs (QEI)
- Synchronization in and between the modules