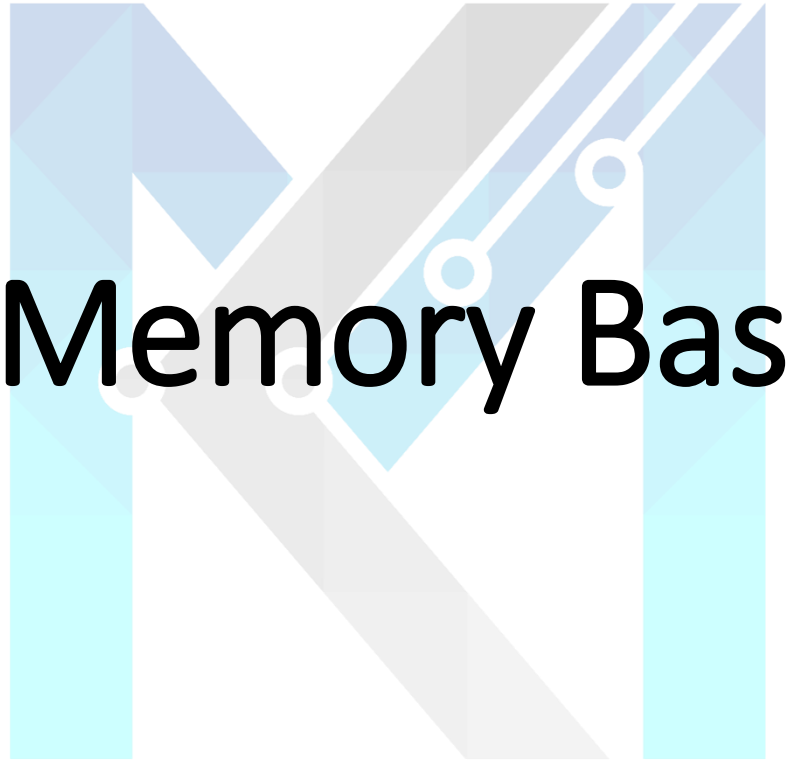


Memory Basics

KERNEL MASTERS

Microprocessor Initiated Operations

- These are operations that the microprocessor itself starts.

  These are usually one of **4 operations**:

  - Memory Read
  - Memory Write
  - I/O Read (Get data from an input device)
  - I/O write (Send data to an output device)

Microprocessor Initiated Operations

- It is important to note that the microprocessor treats memory and I/O devices the same way.
- Input and output devices simply look like memory locations to the microprocessor.

For example, the keyboard may look like memory address A3F2H. To get what key is being pressed, the microprocessor simply reads the data at location A3F2H.

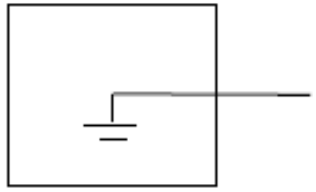
- The communication process between the microprocessor and peripheral devices consist of the following **three** steps:
  - Identify the address.
  - Transfer the binary information.
  - Provide the right timing signals.

The Read Operation

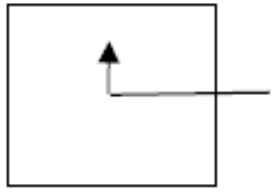
- To read the contents of a memory location, the following steps take place:
  - The microprocessor places the 16-bit address of the memory location on the address bus.
  - The microprocessor activates a control signal called “memory read” which enables the memory chip.
  - The memory decodes the address and identifies the right location.
  - The memory places the contents on the data bus.
  - The microprocessor reads the value of the data bus after a certain amount of time.

Tri-State Buffers

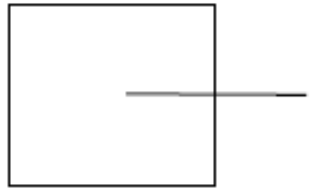
- An important circuit element that is used extensively in memory.
- This buffer is a logic circuit that has three states:
  - Logic 0, logic1, and high impedance.
  - When this circuit is in high impedance mode it looks as if it is disconnected from the output completely.



The Output is Low



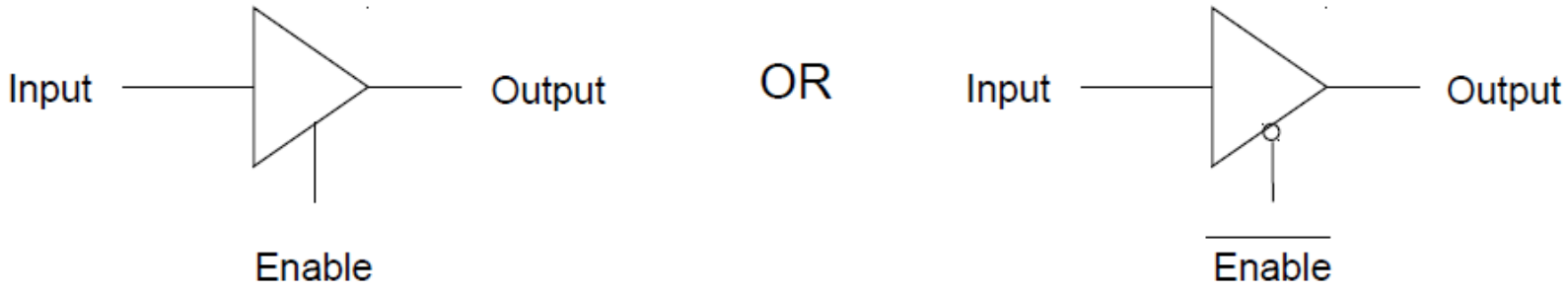
The Output is High



High Impedance

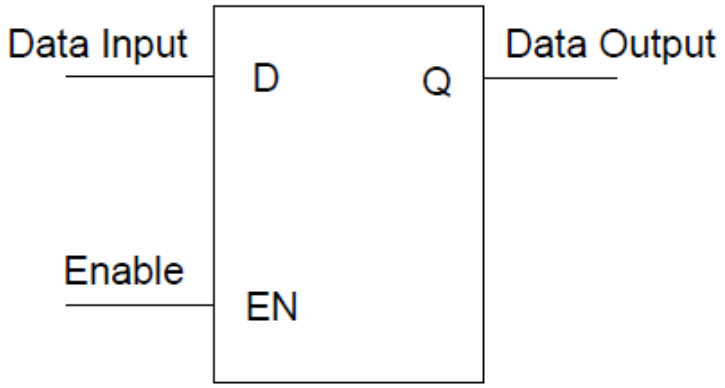
Tri-State Buffers

- This circuit has two inputs and one output.
- The first input behaves like the normal input for the circuit.
- The second input is an “**enable**”.
  - If it is set high, the output follows the proper circuit behavior.
  - If it is set low, the output looks like a wire connected nothing.



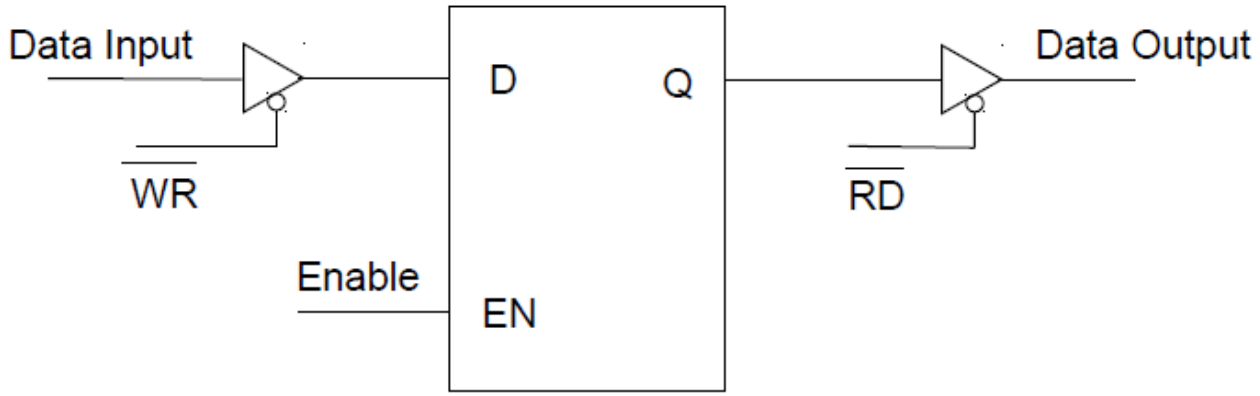
The Basic Memory Element

- The basic memory element is similar to a D latch.
- This latch has an input where the data comes in.
  - It has an enable input and an output on which data comes out.



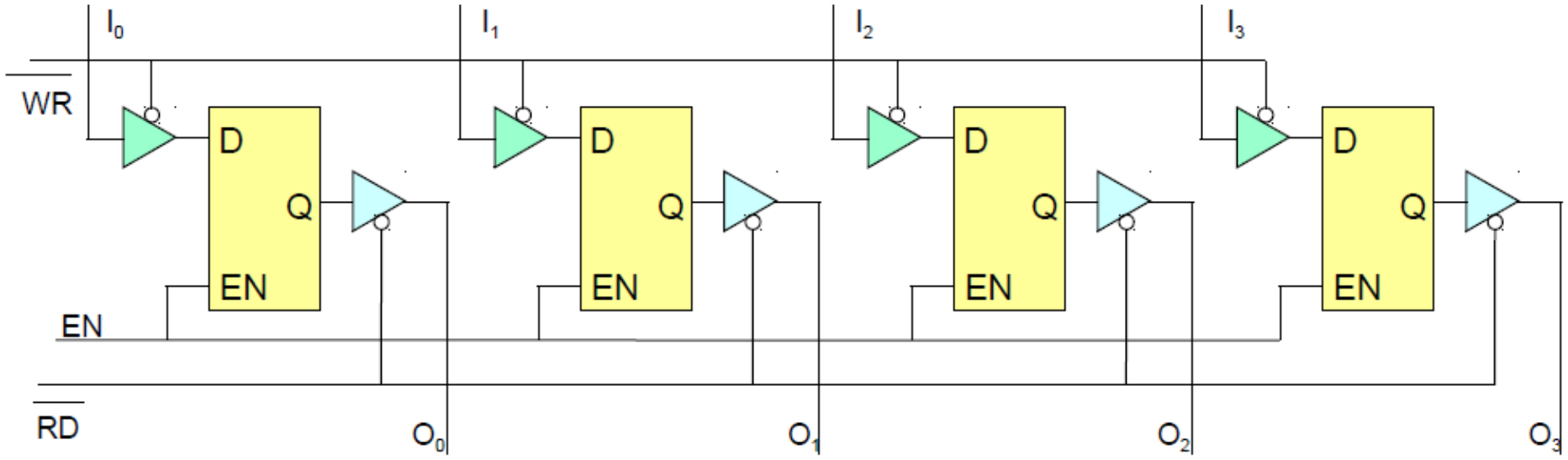
The Basic Memory Element

- However, this is not safe.
  - Data is always present on the input and the output is always set to the contents of the latch.
  - To avoid this, tri-state buffers are added at the input and output of the latch.

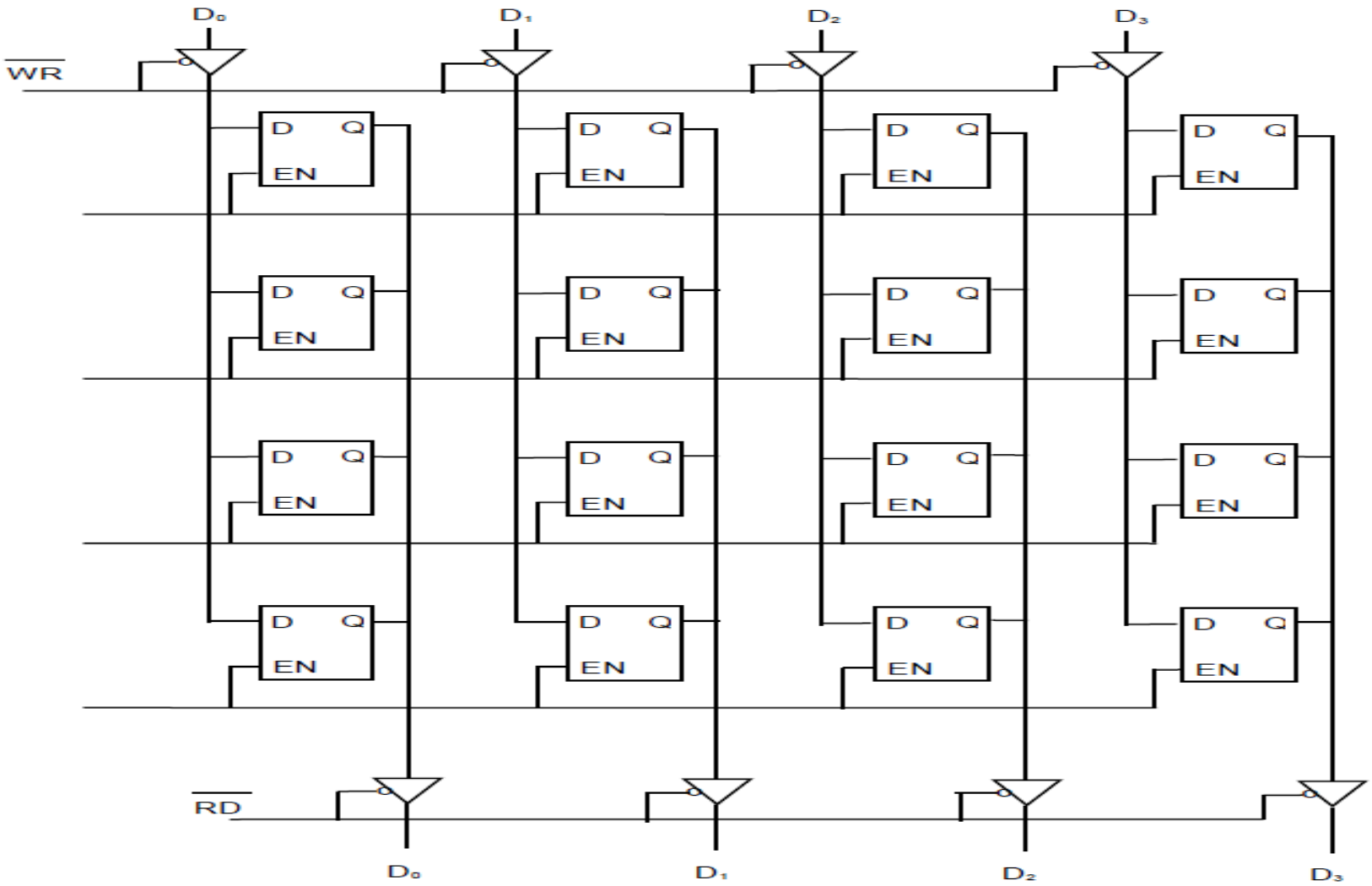


A memory Register

- If we take four of these latches and connect them together, we would have a 4-bit memory register.

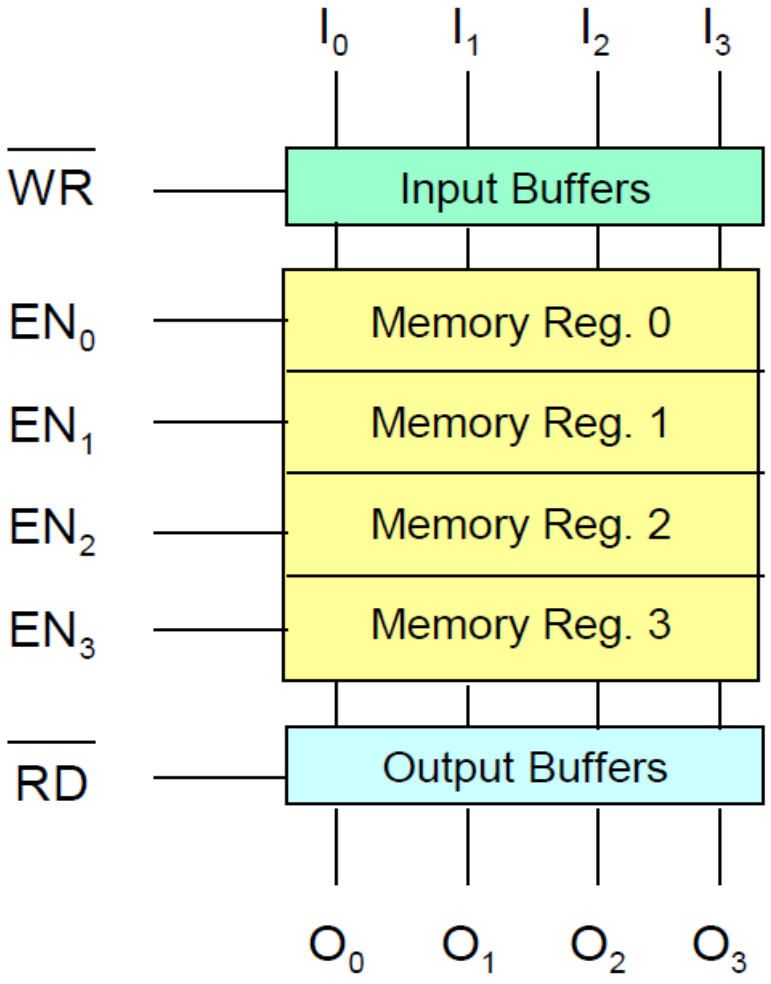


A Group of memory registers



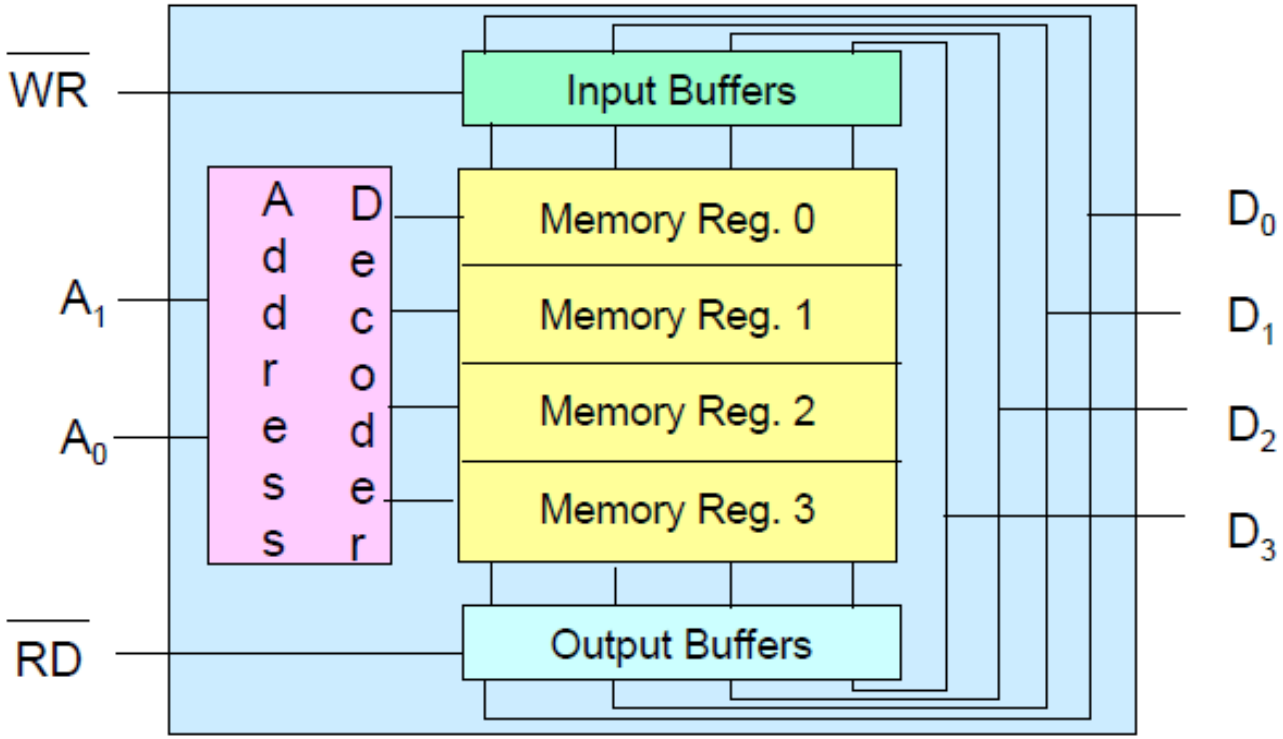
KERNEL MASTERS

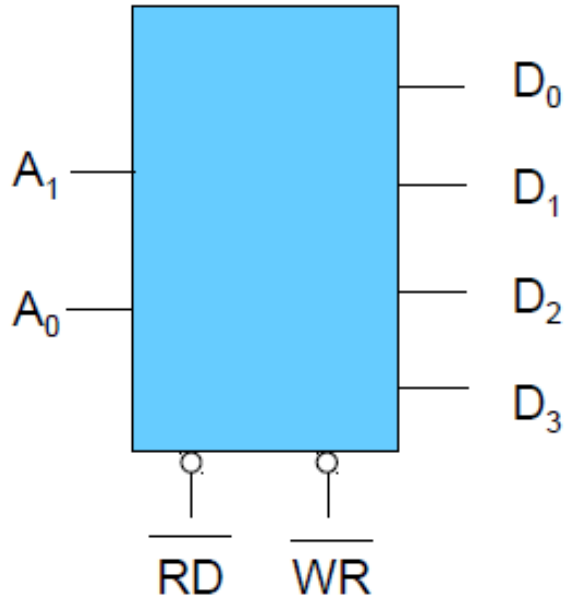
Memory Structure



KERNEL MASTERS

4x4 Memory Structure





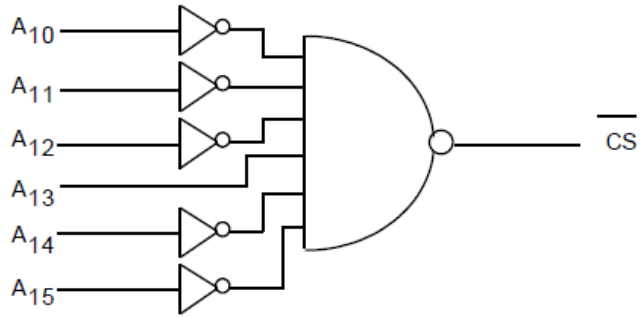
KERNEL MASTERS

Design 8bit Register

- SN54LS173 (4 bit Register)
- 74HC245 (8 bit transceiver)

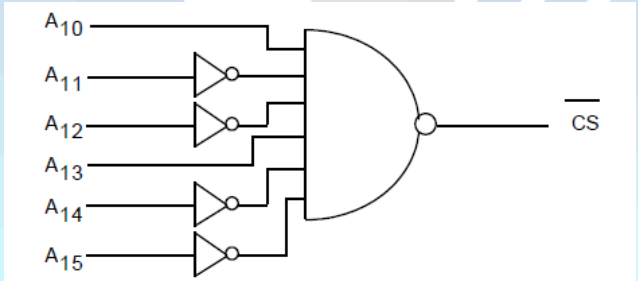
Chip Select Example

- A chip that uses the combination A15 - A10 = 001000 would have addresses that range from 2000H to 23FFH.
  - Keep in mind that the 10 address lines on the chip gives a range of 00 0000 0000 to 11 1111 1111 or 000H to 3FFH for each of the chips.
  - The memory chip in this example would require the following circuit on its chip select input:



Chip Select Example

If we change the above combination to the following:



- Now the chip would have addresses ranging from: 2400 to 27FF.
- Changing the combination of the address bits connected to the chip select changes the address range for the memory chip.

Lab Experiments

Combinational Digital Circuits

1. Design AND, OR, EX-NOR, NAND Gates.
2. Design a 4 bit adder using 74HC283
3. Design a 3 line to 8 line decoder active high outputs using 74HC238.
4. Design a 4 line to 16 line decoder active high outputs (Using two 3x8 Decoders).
5. Design and implement a computational function using 8:1 MUX IC 74151.

Lab Experiments

Sequential Digital Circuits

6. Design a SR Latch using Cross coupled NAND Gates (DM7403N)
7. Design a 1HZ Clock Generator Circuit using 555 Timer
8. Test JK Flip Flop use 555 timer clock output. Design output of JK Flip Flop is half of the input frequency.
9. Design 8-bit Serial-In and Parallel-output(74HC595) use 555 timer clock output.
10. Design an 8-bit register.
    - 74LS173 (Quad D Flip-flop, three states outputs and asynchronous clear)
    - 74LS245 (Octal Bus Transceiver, non inverting three state outputs)