060010104- Digital Electronics

Unit1 : Codes

Short Question

1. Define signal.
2. List out the advantages of using digital circuitry.
3. What do you mean by radix of the number system?
4. Differentiate Analog and Digital system.
5. What is the essential characteristic of Hexadecimal number system over Binary number system?
6. What is the full form of ASCII?
7. What do you mean by alphanumeric codes?
8. What is the usage of the 8^{th} bit of ASCII 7 bit code?
9. List out advantage of Unicode over other Alphanumeric Codes.
10. Even if the EBCDIC is having no technical advantage over ASCII why it is used.
11. What is the binary equivalent of 'A' in ASCII code?
12. What is the decimal equivalent of 'D' in EBCDIC code?
13. What is nibble?
14. What is parity bit?
15. What is MSB and LSB?
16. What do you mean by odd parity?
17. Define byte.
18. What do you mean by even parity?
19. What is the full form of EBCDIC?
20. Encode the following decimal numbers in BCD code. A)64 B) 525.25

Long Question

1. Explain characteristics of Number System with proper example.
2. Consider an arbitrary number system having the independent digit as X,Y,Z. What is the radix of this number system? List the numbers that you can represent using this number system with 3 digits.
3. Explain Decimal number system
4. Write a short not on Binary number system.
5. Write a short not on ASCII.
6. Write a short not on CRC.
7. Explain Hamming Code using proper example.
8. What is UNICODE? Explain it in brief.
9. Write a short note on Repetition code.
10. Draw a chart for ASCII Code.
11. Construct Hamming code for the following 8-bits words
    a) 10101010
    b) 00000000
    c) 11111111
    d) 01010101
12. Draw EBCDIC Code chart.

060010104- Digital Electronics

13. For some 8-bit data words, the following Hamming code words are received. Determine the correct data words. Assume even parity check.
    a) 000011101010
    b) 101110000110
    c) 101111110100
14. Convert the following number into binary numbers to octal and then to decimal.
    a) 11011100.101010
    b) 01010011.010101
    c) 10110011
15. What is parity bit? Define even and odd parity. What is the limitation of parity code when it comes to detection and correction of bit errors?
16. Write step to for sender and receiver side of CRC method.
17. Given seven-bit ASCII notation for A=''1000001" and that the data word gets corrupted to 1010001 in the transmission channel, show how the hamming code can be used to identify the error. Use even parity.

Multiple Choice Questions

1. Hamming code is capable of
    a) Only detect single-bit error
    b) Only correct single-bit error
    c) Detect and correct single bit error
    d) None of above
2. How many alphanumeric characters can be represented using ASCII 7 bit Code.
    a) 126
    b) 129
    c) 128
    d) 127
3. What is the base of hexadecimal number system?
    a) 15
    b) 16
    c) 10
    d) None of above
4. Which of the following statements does NOT describe an advantage of digital technology?
    a) The values may vary over a continuous range.
    b) The circuits are less affected by noise.
    c) The operation can be programmed.
    d) Information storage is easy.
5. What are the symbols used to represent digits in the binary number system?
    a) 0,1
    b) 0,1,2
    c) 0 through 8
    d) 1,2

060010104- Digital Electronics

6. Give the decimal value of binary 10010.
   a) 6_{10} b) 9_{10}
   c) 18_{10} d) 20_{10}
7. Convert the fractional binary number 0000.1010 to decimal.
   a) 0.625 b) 0.50
   c) 0.55 d) 0.10
8. In the decimal numbering system, what is the MSD?
   a) The middle digit of a stream of numbers
   b) The digit to the right of the decimal point
   c) The last digit on the right
   d) The digit with the most weight
9. Digital representations of numerical values of quantities may BEST be described as having characteristics:
   a) that are difficult to interpret because they are continuously changing.
   b) that vary constantly over a continuous range of values.
   c) that vary in constant and direct proportion to the values they represent.
   d) that vary in discrete steps in proportion to the values they represent.
10. Convert the fractional decimal number 6.75 to binary.
    a) 0111.1100 b) 0110.1010
    c) 0110.1100 d) 0110.0110
11. How many binary bits are necessary to represent 748 different numbers?
    a) 9 b) 7
    c) 10 d) 8
12. How many unique symbols are used in the decimal number system?
    a) One b) Nine
    c) Ten d) Unlimited
13. What is the radix of octal number system?
    a) 8
    b) 7
    c) 9
    d) 10
14. Choose the odd one out
    a) ASCII
    b) EBCDIC
    c) UNICODE
    d) Parity Code
15. EBCDIC is having how many bits code.
    a) 4
    b) 8
    c) 16
    d) 2
16. The Hamming distance between equal code words is _____.
    a) 1
    b) N
    c) 0
    d) None of the above

060010104- Digital Electronics

17. If the Hamming distance between a dataword and the corresponding codeword is three, there are ____ bits in error.
    a) 3
    b) 5
    c) 4
    d) None of the Above
18. The Hamming distance between 100 and 001 is _____.
    a) 1
    b) 2
    c) 0
    d) 3
19. Which is correct Frame for this G(x)=X4 + X + 1 Generator Polynomial G(x).
    a) 11000110
    b) 11100110
    c) 00111010
    d) 1101011011
20. In cyclic redundancy checking, what is the CRC?
    a) The divisor
    b) The quotient
    c) The dividend
    d) The remainder

True FALSE

1. The most important reason why digital circuitry becoming more popular is because digital circuits are usually simpler and faster than analog circuits.
2. Parity code can be used to correct error.
3. Parity code can be used to detect multiple-bit error.
4. Repetition code is highly efficient gives maximum throughput.
5. Binary number system is having radix 2.
6. The decimal equivalent of 'A' is 56.
7. Temperature variation is normally an analog quantity.
8. A digital quantity has a discrete set of values.
9. The real world is mainly analog.
10. Binary means having two states or values.
11. The binary number 11101111 has an even parity.
12. Four bits equal one byte.
13. Analog signals are continuous in nature.
14. In a binary system there are only two symbols.
15. The decimal number system is having radix 10.
16. Binary code for 0(zero) is 0110000.
17. Error detecting method that can detect more errors without increasingadditional information in each packet is CRC.
18. In cyclic redundancy checking CRC is the divisor.
19. VRC is also known as Parity check.
20. The binary number 11101011 has an odd parity.

060010104- Digital Electronics

Fill in the blanks:

1. The radix of binary number system is _____ and the digits used are _____.
2. Parity bit codes can _____ error.
3. In _____ number system 16 distinct symbols are used to specify any number.
4. A(n) _____ device is one that has signal which varies continuously in step with the input.
5. Most "real-world" events are _____ in nature.
6. MSB = _____.
7. A byte contains _____ bits.
8. ASCII is ____ bit codes and EBCDIC is ____ bit codes.
9. The parity of 01110010 is _____.
10. Gray code is a _____.(weighted/non-weighted)
11. Consider a hypothetical number system with a radix of 3 and its three independent digits as 0, 2, 4. The number that would come immediately after 444 is _____.
12. 1101011 is _____ a binary number. (necessarily, not necessarily)
13. The binary number 11101011 has an _____ parity. (even, odd)
14. LSB= _____.
15. 100010.11 _____ be a decimal number. (can, cannot)
16. The term _____ means that only 1bit of a given data unit is changed from 0 to 1.
17. The central concept in detecting or correcting error is _____.
18. The Hamming distance between equal code words is _____.
19. Full form of EBCDIC is _____.

Unit 2 : Boolean Algebra and Simplification Techniques

Short Questions

1. Define Gates.
2. List out the basic gates.
3. Define AND Gate.
4. What do you mean by logic circuit?
5. How to obtain dual of a given expression.
6. What do you mean by truth table?
7. Define variable.
8. What is Redundancy Law?
9. Define complement.
10. List out the Postulates.
11. What is the method of perfect induction?
12. Define OR Gate.
13. What do you mean by Boolean algebra?
14. List out the truth table entry for two input NAND Gate.
15. Define term.
16. Design a logic circuit for expression AB + C.

060010104- Digital Electronics

17. Define literals.
18. Define fundamental products.
19. Define fundamental sums
20. What does the algebraic means of simplifying the Boolean expression misses?
21. How to obtain complement of a given expression.
22. What is the use of Boolean algebra?
23. What is Involution Law?
24. Write Redundancy Law.
25. What is Karnaugh Map method?

Long Questions

1. Explain using diagram how NOR and NAND Gates are Universal Gate.
2. Explain De Morgan's theorem using example.
3. Explain Identity, Complementation, Commutative, Associative and Distributive Laws with example.
4. Explain three variable Karnaugh map using example.
5. Explain Don't care condition using example.
6. Explain sum-of-products and product-of-sums.
7. Explain expanded form and canonical form of Boolean expression using example.
8. Show the logic circuit for Y = AB' + AB. Next simplify this Boolean equation and the corresponding circuit.
9. Show the logic circuit for this Boolean equation Y = (A'+B) · (A+B). Then, simplify the circuit s much as possible using algebra.
10. Obtain the simplified expression in sum of products for the following Boolean functions:
    a) xy + x'y'z' + x'yz'
    b) A'B + BC' + B'C'
    c) a'b' + bc + a'bc'
    d) xy'z + xyz' + x'yz + xyz
11. Convert the following sum-of-products Boolean expression into product-of-sums and vice versa.
    a) (A + B + C') · (A + B'+ C) · (A' + B + C) · (A' + B' + C')
    b) A · B + A' · B'
    c) A' · B'·C' + A' · B · C+ A · B · C' + A · B' · C
    d) (A + B') · (B' + C) · (B' + D)

12. Given the following truth table:

A	B	C	Y
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

    a) Obtain the simplified functions in sum of products

060010104- Digital Electronics

b) Obtain the simplified functions in product of sums

13. Design a sum-of-product and product-of-sum expression for the given truth table.

A	B	C	Y
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

14. Simplify the following Boolean expressions:
    a) $A \cdot B \cdot C + A \cdot B \cdot C' + A \cdot B' \cdot C + A \cdot B' \cdot C' + A' \cdot B \cdot C + A' \cdot B \cdot C' + A' \cdot B' \cdot C' + A' \cdot B' \cdot C$
    b) $(A' + B + C') \cdot (A' + B + C) \cdot (C + D) \cdot (C + D + E)$
15. Prove the following expression
    a) $A + A \cdot B' + A \cdot B' \cdot C' + A \cdot B' \cdot C + C' \cdot B \cdot A = A$
    b) $[\, 1 + L \cdot M + L \cdot M' + L' \cdot M \,] \cdot [\, (L + M') \cdot (L' \cdot M) + L' \cdot M' (L + M) \,] = 0$
16. Minimize the Boolean function:
    $F(A,B,C) = \sum 0,1,3,5 + \sum_{\emptyset} 2,7$
17. Obtain the canonical form for the following
    a) $F(A,B,C,D) = A \cdot B' \cdot C' + A \cdot B \cdot C \cdot D + A' \cdot B \cdot C' \cdot D + A' \cdot B' \cdot C' \cdot D$
    b) $F(A,B,C,D) = (B + C' + D')\,(A' + B' + C + D)\,(A + B' + C' + D')$
18. Obtain the simplified expressions in sum-of-products:
    a) $F(x,y,z) = \sum(2,3,6,7)$
    b) $F(A,B,C,D) = \sum(7,13,14,15)$
    c) $F(A,B,C,D) = \sum(4,6,7,15)$
    d) $F(w,x,y,z) = \sum(2,3,12,13,14,15)$
19. Obtain the simplified expressions in product-of-sums:
    a) $F(x,y,z) = \prod(0,1,4,5)$
    b) $F(A,B,C,D) = \prod(0,1,2,3,4,10,11)$
    c) $F(w,x,y,z) = \prod(1,3,5,7,13,15)$
20. The following Boolean expression BE + B'DE' is a simplified version of the expression A'BE + BCDE + BC'D'E + A'B'DE' + B'C'DE'. Are there any don't-care conditions? If so, what are they?
21. Draw a Karnaugh map for the following truth tables. Then encircle all the octets, quads and pairs you can find.

060010104- Digital Electronics

A	B	C	D	Y
0	0	0	0	0
0	0	0	1	1
0	0	1	0	0
0	0	1	1	0
0	1	0	0	0
0	1	0	1	1
0	1	1	0	0
0	1	1	1	0
1	0	0	0	0
1	0	0	1	0
1	0	1	0	1
1	0	1	1	1
1	1	0	0	1
1	1	0	1	1
1	1	1	0	0
1	1	1	1	0

A	B	C	D	Y
0	0	0	0	0
0	0	0	1	1
0	0	1	0	1
0	0	1	1	1
0	1	0	0	0
0	1	0	1	0
0	1	1	0	0
0	1	1	1	1
1	0	0	0	1
1	0	0	1	1
1	0	1	0	1
1	0	1	1	0
1	1	0	0	0
1	1	0	1	1
1	1	1	0	0
1	1	1	1	0

22. Simplify the Boolean expression using Karnaugh map method.
    a) F = X'YZ + X'YZ' + XY'Z' + XY'Z
    b) F = X'YZ + XY'Z' + XYZ + XYZ'

Multiple Choice Questions

1. NOT Gate is having how many input
    a) One or more
    b) Two or more
    c) Zero or more
    d) One
2. The dual of a Boolean expression is A + B. The expression is
    a) A · B
    b) A' · B'
    c) A' + B'
    d) A + B
3. How many combination are there for three input gates
    a) 2
    b) 4
    c) 6
    d) 8
4. If all the inputs are HIGH then the output is HIGH
    a) AND
    b) NAND
    c) OR
    d) NOR

060010104- Digital Electronics

5. Any Gate is having how many output
   a) One or more
   b) Two or more
   c) One
   d) Zero or more
6. The dual of Boolean expression is A + B
   a) A ·B
   b) B+A
   c) A'+B'
   d) A'·B'
7. Which Law it is? X · Y + X · Z = (X + Z) · (X + Y)
   a) Distributive Law
   b) Associative Law
   c) Transposition Law
   d) Commutative Law
8. Complement of complement of A' B + A B' is
   a) A · B + A' · B'
   b) (A' + B) · (A + B')
   c) A' · B + A · B'
   d) None of these
9. $\overline{x} \cdot \overline{x} \cdot \overline{x}$
   a) $\overline{0}$
   b) $\overline{X}$
   c) X
   d) 1
10. In a four variable Boolean expression, a group of four 1's in the corresponding Karnaugh map will yield a term having
    a) 2 literals
    b) 1 literals
    c) 4 literals
    d) None of these
11. If a 3-input NOR gate has eight input possibilities, how many of those possibilities will result in a HIGH output?
    a) 1 b) 2
    c) 7 d) 8
12. In a two variable Boolean expression, a group of four 1's in the corresponding Karnaugh map will yield a term having
    a) 2 literals
    b) 1 literals
    c) 4 literals
    d) None of these

13. The output of an OR gate with three inputs, A, B, and C, is LOW when _____.
    a) A = 0, B = 0, C = 0
    b) A = 0, B = 0, C = 1
    c) A = 0, B = 1, C = 1
    d) all of the above
14. Logically, the output of a NOR gate would have the same Boolean expression as a(n):

060010104- Digital Electronics

a) NAND gate immediately followed by an inverter
b) OR gate immediately followed by an inverter
c) AND gate immediately followed by an inverter
d) NOR gate immediately followed by an inverter

15. The output of a NOR gate is HIGH if _____.
a) all inputs are HIGH
b) any input is HIGH
c) any input is LOW
d) all inputs are LOW

16. The Boolean expression for a 3-input AND gate is _____.
a) X = AB
b) X = ABC
c) X = A + B + C
d) X = AB + C

17. What does the small bubble on the output of the NAND gate logic symbol mean?
a) open collector output
b) tristate
c) The output is inverted
d) none of the above

18. The output of a NOT gate is HIGH when _____.
a) the input is LOW
b) the input is HIGH
c) power is applied to the gate's IC
d) power is removed from the gate's IC

19. How many inputs of a four-input AND gate must be HIGH in order for the output of the logic gate to go HIGH?
a) any one of the inputs
b) any two of the inputs
c) any three of the inputs
d) all four inputs

20. Which of the following gates has the exact inverse output of the OR gate for all possible input combinations?
a) NOR b) NOT
c) NAND d) AND

21. Which of the following gates is described by the expression X= $\overline{ABCD}$?
a) OR b) AND
c) NOR d) NAND

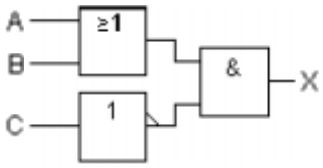
22. In the Karnaugh map for a five variable Boolean function, a certain group corresponds to a term having two literals. It should be a group of
a) 64
b) 32
c) 128
d) None of above

True/False

060010104- Digital Electronics

1. A NOR gate output is LOW if any of its inputs is LOW.
2. If in a given expression the variable and it's complements are said two different variables.
3. 1 · 0 = 1. (here . means AND Operation)
4. In OR Gate if all the inputs are low then the output is high.
5. A NOR gate and an OR gate operate in exactly the same way.
6. A NAND gate output is LOW only if all the inputs are HIGH.
7. An exclusive-NOR gate output is HIGH when the inputs are unequal.
8. 1 + 0 = 1. (here + means OR Operation)
9. $X + X + X + \ldots\ldots + X = X$
10. $X \cdot \overline{Y} + X \cdot Z + Y \cdot Z = X \cdot Y + \overline{X} \cdot Z$
11. If in a given expression the variable and it's complements are said two different variables.
12. NOR gate is also known as Bubbled AND Gate.
13. If f(x, y, z) is a Boolean function, then f(x, y, z) + f'(x, y, z) = 1.
14. In the Boolean expression X Y + Y' Z + W, there are five literals, four variables and three terms.
15. In a Boolean equation the use of the + symbol represents the OR function.
16. A logic gate has one or more output terminals and one input terminal.
17. An inverter output is the complement of its input.

1. Fill in the Blanks
2. _____ & _____ are the Universal Gate.
3. 1 + 0 = ____.
4. + is used to denote _____ operation.
5. NAND gate is also known as _____ Gate.
6. The equality (A · B · C)' = A' + B' + C' is better known as _____ Law.
7. _____,_____ are the logic gates whose output entries are logic '1' except for one entry that is logic 'o'.
8. A logic gate with six inputs can have ____ possible input combinations.
9. _____ is the only input combination that will produce logic '1' at the output of eight-input AND gate.
10. _____ is the only input combination that will produce logic '0' at the output of eight-input NAND gate.
11. _____ is the only input combination that will produce logic '1' at the output of eight-input NOR gate.
12. _____ is the only input combination that will produce logic '0' at the output of four-input OR gate.
13. The Boolean expression C + CD is equal to _____.
14. The Boolean expression for the logic circuit shown is ____.



15. Applying DeMorgan's theorem and Boolean algebra to the expression $\overline{(A\bar{B})(\bar{A}C)}$ results in _____.
16. The standard SOP form of the expression $\bar{A}B+\bar{A}C$ is _____.

UNIT 3: Arithmetic Circuits

Short Questions

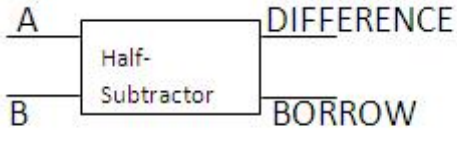
1. What do you mean by sequential circuits?
2. What do you mean by combinational circuits?
3. List out any three combinational circuits.
4. Define Half Adder.
5. Define Half Subtractor.
6. Define Full Adder.
7. Define Full Subtractor.
8. Give logic implementation of half adder.
9. Define ALU.
10. What do you mean by Multipliers?
11. What do you mean by controlled inverter?
12. Draw a logic circuit for 4-bit controlled inverter.
13. Which part of CPU performs addition, subtraction operations?
14. Draw a logic diagram for CARRY.
15. Draw a logic diagram for BORROW.
16. Write a product of sums expression for full adder CARRY.
17. Write a product of sums expression for full subtractor BORROW.
18. Write a sum of products expression for full adder SUM.
19. Write a product of sums expression for full subtractor DIFFERENCE.
20. A six-variable truth table would have how many combinations?
21. Convert the signed number -25 to its 8-bit 2's complement form. Remember that left most bit will be 1, which means the number is negative.
22. Draw a truth table for half adder.
23. Draw a truth table for half subtractor.
24. Write the carry expression for BCD adder.

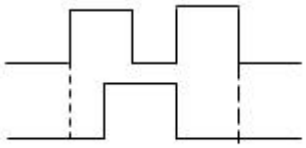
Long Question

1. Explain the steps to implement or design combinational logic circuit.
2. Explain BCD Adder with proper logic circuit diagram.
3. Explain full adder with proper logic circuit diagram.
4. Explain half subtractor with proper logic circuit diagram.
5. Draw a circuit for a two's complement implementer using the 4-bit adder cum subtractor.
6. Implement a full subtractor with two half subtractor and an OR gate.
7. Show how a full adder can be converted to a full subtractor with the addition of one inverter circuit.
8. Design a combinational circuit that converts a decimal digit from the 8, 4,-2,-1 code to BCD.

060010104- Digital Electronics

9. Design a combinational circuit that converts a decimal digit from the 2,4,2,1 code to the 8, 4,-2,-1 code.
10. Design a combinational circuit whose input is a four-bit number and whose output is the 2's complement of the input number.
11. Design a combinational circuit that accepts a three-bit number and generate an output binary number equal to the square of the input number.
12. Give different implementations of half adder logic circuit.
13. Explain 4 X 4 bit multiplier using proper logic circuit diagram.
14. Design a combinational circuit that will compare two 8-bit numbers.
15. Design a combinational circuit that will generate odd-parity.
16. Draw a block diagram for 4 full adders processing the addition on 4 bits of A and 4 bits of B register.
17. Show the different implementation of half subtractor and full subtractor.
18. Show the different implementation of half adder and full adder.
19. Design a combinational circuit that accepts a three-bit number and generates an output binary number equal to the square of the input number.
20. For the following figure plot the corresponding DIFFERENCE and BORROW outputs on the same scale.





Multiple Choice Questions

1. A half adder circuit has two inputs and
   a) one output
   b) two output
   c) three output
   d) none of these
2. A half subtractor circuit has
   a) 2 i/p & 2 o/p
   b) 3 i/p & 2 o/p
   c) 2 i/p & 3 o/p
   d) none of these
3. Which one of the following is odd?
   a) Multiplexer b) Decoder c) Adder d) Flip-Flop
4. The output of SUM is equal to output of
   a) OR gate b) AND gate c) X-OR gate d) X-Nor gate
5. The output of CARRY is equal to output of
   a) AND gate b) OR gate c) NOT gate d) NOR gate
6. The output of full adder SUM is equal to
   a) $X \cdot Y \cdot Z$
   b) $X + Y + Z$
   c) $X + Y \cdot Z$
   d) $X \oplus Y \oplus Z$

060010104- Digital Electronics

7. Solving –11 + (–2) will yield which two's-complement answer?
   a) 1110 1101 b) 1111 1001 c) 1111 0011 d) 1110 1001
8. For a 4-bit parallel adder, if the carry-in is connected to a logical HIGH, the result is:
   a) The same as if the carry-in is tied LOW since the least significant carry-in is ignored.
   b) That carry-out will always be HIGH.
   c) One will be added to the final result.
   d) The carry-out is ignored.
9. Solve this BCD problem: 0100 + 0110 =
   a) 00010000_{BCD}
   b) 00010111_{BCD}
   c) 00001011_{BCD}
   d) 00010011_{BCD}
10. What is the major difference between half-adders and full-adders?
   a) Nothing basically; full-adders are made up of two half-adders.
   b) Full adders can handle double-digit numbers.
   c) Full adders have a carry input capability.
   d) Half adders can handle only single-digit numbers.
11. The binary subtraction 0 – 0 =
   a) difference = 0, borrow = 0
   b) difference = 1, borrow = 0
   c) difference = 1, borrow =1
   d) difference = 0, borrow = 1
12. How many basic binary subtraction operations are possible?
   a) 2
   b) 1
   c) 3
   d) 4
13. When performing subtraction by addition in the 2's-complement system:
   a) the minuend and the subtrahend are both changed to the 2's-complement
   b) the minuend is changed to 2's-complement and the subtrahend is left in its original form
   c) the minuend is left in its original form and the subtrahend is changed to its 2's-complement
   d) the minuend and subtrahend are both left in their original form
14. One way to make a four-bit adder perform subtraction is by:
   a) Inverting the output.
   b) Inverting the carry-in.
   c) Inverting the B inputs.
   d) Grounding the B inputs.
15. Which of the following is the primary advantage of using binary-coded decimal (BCD)
   a) Fewer bits are required to represent a decimal number with the BCD code
   b) BCD codes are easily converted from decimal
   c) the relative ease of converting to and from decimal
   d) BCD codes are easily converted to straight binary codes.

060010104- Digital Electronics

16. What is the difference between a full-adder and a half-adder?
    a) Half-adder has a carry-in.
    b) Full-adder has a carry-in.
    c) Half-adder does not have a carry-out.
    d) Full-adder does not have a carry-out.

True/False

1. The output of combinational circuit is depends only on present input combination.
2. The output of sequential circuit is depends only on present input combination.
3. The half adder circuit performs the addition of three bits.
4. The full adder circuit produces only single output that is SUM.
5. It is possible to perform subtraction with full adder circuit.
6. Addition of 2's complement of the subtrahend with minuend results in subtraction.
7. It is possible to design single circuit for both adder and subtractor.
8. If there is carry while performing subtraction using 2's complement addition then final answer will be 2's complement of the resulting addition.
9. The number of input variables and output variables are same in combinational circuit.
10. For X-NOR gate if the number of 1's at input are odd then output is LOW.
11. The outputs of SUM and DIFFERENCE are equal in adder and subtractor.
12. The output functions specified in the truth table give exact definition of the circuit.
13. When the binary sum is greater than 1001, we obtain invalid BCD representation.
14. The decimal parallel adder that adds n decimal digits need n BCD adder stages.
15. Half subtractor is a circuit that subtracts three bits.
16. The output of SUM is similar to the X-NOR gate.
17. The output of DIFFERENCE is similar to X-OR gate.
18. BCD adder is a decimal adder circuit.
19. Binary multiplication is much simpler than decimal multiplication.
20. All microcontrollers have a multiply instruction.

Fill in the Blanks

1. A _____ is needed when adder is used as subtractor.
2. DIFFERENCE = x' · y + x · y' and BORROW = _____.
3. CARRY = x · y and SUM = _____.
4. 2's complement of 10000 is _____.
5.
6.
7. Binary addition of 101 + 011 = _____.
8. Binary subtraction of 101 – 011 = _____.
9. Twos complement numbers are widely used in digital system because they can be used to represent _____ numbers.
10. A controlled inverter is used to implement ____ complement.

060010104- Digital Electronics

11. BCD stands for _____.
12. The negative of binary number is its _____.
13. The parallel adders are _____ (combinational, sequential) circuits.
14. The addition of _____ to the binary sum converts invalid BCD representation to the correct one.
15. A BCD adder requires _____ no of full adder.
16. There are _____number of don't care inputs are there in a BCD adder?
17. ALU performs _____ & _____ operations.
18. 01101000BCD + 00110110BCD = _____BCD.

UNIT-4 : Combinational Logic Circuits

Short Questions

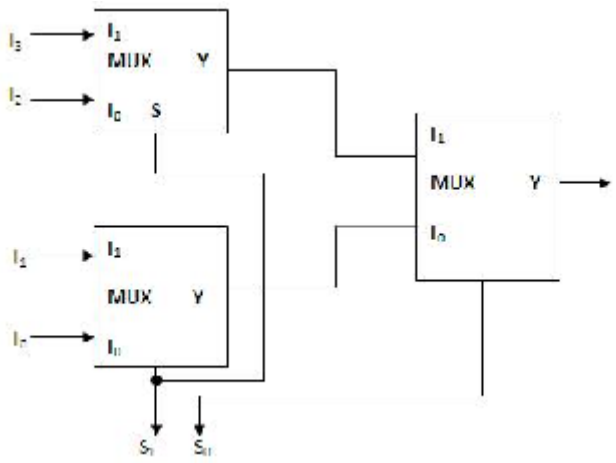
1. List out the different combinational logic circuits.
2. Define Multiplexer.
3. Draw a block diagram for 4 x 1 lines MUX.
4. Draw a truth table for a 4 x 1 line multiplexer without enable line.
5. Draw a truth table for a 4 x 1 line multiplexer with enable line having active LOW.
6. Draw a logic diagram of 2 x 1 lines multiplexer with its truth table.
7. What do you mean by active LOW Multiplexer?
8. Define decoder.
9. Define encoder.
10. What do you mean by priority encoder?
11. Define Demultiplexer.
12. What do you mean by parity generators and parity checkers?
13. What do you mean by strobe?
14. Define active low.
15. What is the purpose of control gate pin in a decoder?
16. Give four application of a decoder.
17. What is difference between a multiplexer and encoder?
18. What is the purpose of decoder's inputs?
19. What do you mean by parallel to serial conversion?

Long Questions

1. Draw a logic diagram of 8 X 1 lines multiplexer with enable HIGH line with its truth table.
2. Write a note on application of multiplexer.
3. Implement the SUM and CARRY Boolean functions of half adder with multiplexers.
4. Implement the DIFFERENCE and BORROW Boolean functions of half subtractor with multiplexers.
5. Implement the SUM and CARRY Boolean functions of full adder with multiplexers.
6. Implement the DIFFERENCE and BORROW Boolean functions of full subtractor with multiplexers.

060010104- Digital Electronics

7. Implement the following Boolean function with multiplexer having one less selection line than the number of variables.
   a) f(A,B,C) = $\sum 2,4,7$
   b) f(A,B,C)= $\sum 1,3,5,7$
   c) f(A,B,C) = $\prod 0,2,7$
8. Draw a logic diagram for quadruple 2-to-1 line multiplexers with enable LOW with their truth table.
9. Design a 16-to-1 multiplexer using two 8-to-1 multiplexer having an active-LOW Enable input.
10. Implement the Boolean function f (A,B,C,D) = $\sum 2,4,9,10$ with multiplexer having active-HIGH Enable input.
11. Explain encoder using proper example.
12. Design a four-line to two-line priority encoder with active HIGH inputs and outputs, with priority assigned to the higher order data input line.
13. Implement a full adder with a decoder.
14. What is the difference between encoder and decoder? Explain with example.
15. Implement a full subtractor combinational circuit using 3-to-8 decoder and external NOR gates.
16. Explain 3-to-8 line decoder in brief with necessary logic diagram.
17. Determine the function performed by the combinational circuit in below figure.



18. Explain cascading decoder circuits with example.
19. Write a brief note on parity generation and checking circuit with necessary logic diagram.
20. Design a 32-to-1 multiplexer using 8-to-1 multiplexer having active-LOW Enable input and 2-to-4 decoder.
21. Draw the logic diagram and explain the 1-to-16 Demultiplexer circuit.

Multiple Choice Questions

060010104- Digital Electronics

1. A combinational circuit which is used to change a decimal number into an equivalent BCD number is
   a) Decoder b) Encoder c) Multiplexer d) Demultiplexer
2. When an application, such as an encoder, calls for a unique response from a circuit corresponding to a combination of its input variables, the two methods that best serve this purpose are the _____ and the _____.
   a) Case construct, truth table
   b) If then statement, else statement
   c) VARIABLE,PROCESS
   d) FUNCTION TYPE
3. A combinational circuit which is used to change a BCD number into an equivalent decimal number is
   (a) Decoder b) Encoder c) Multiplexer d) Demultiplexer
4. A combinational circuit which is used to send data coming from a single source to two or more separate destinations is called as:
   (a) Decoder b) Encoder c) Multiplexer d) Demultiplexer
5. How many data select lines are required for selecting eight inputs?
   a) 1
   b) 2
   c) 3
   d) 4
6. Convert BCD 0001 0111 to binary.
   a) 10101
   b) 10010
   c) 10001
   d) 11000
7. How many 3-line-to-8-line decoders are required for a 1-of-32 decoder?
   a) 1
   b) 2
   c) 4
   d) 8
8. A combinational circuit which is used to change a decimal number into an equivalent BCD number is
   a) Decoder b) Encoder c) Multiplexer d) Demultiplexer
9. When an application, such as an encoder, calls for a unique response from a circuit corresponding to a combination of its input variables, the two methods that best serve this purpose are the _____ and the _____.
   a) Case construct, truth table
   b) If then statement, else statement
   c) VARIABLE,PROCESS
   d) FUNCTION TYPE
10. A combinational circuit which is used to change a BCD number into an equivalent decimal number is
    (a) Decoder (b) Encoder (c) Multiplexer (d) Demultiplexer
11. A combinational circuit which is used to send data coming from a single source to two

or more separate destinations is called as:

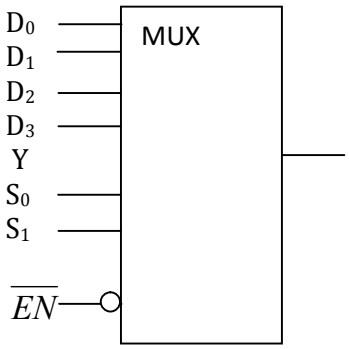
(a) Decoder (b) Encoder (c) Multiplexer (d) Demultiplexer

12. How many data select lines are required for selecting eight inputs?
    a) 1
    b) 2
    c) 3
    d) 4

13. Convert BCD 0001 0111 to binary.
    a) 10101
    b) 10010
    c) 10001
    d) 11000

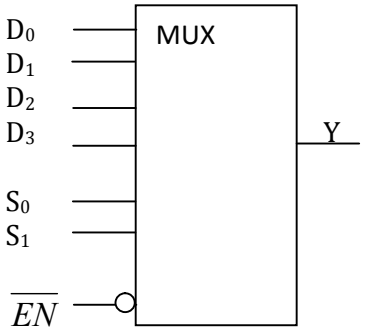
14. How many 3-line-to-8-line decoders are required for a 1-of-32 decoder?
    a) 1
    b) 2
    c) 4
    d) 8

15. For the device shown here, let all D inputs be LOW, both S inputs be HIGH, and the $\overline{EN}$ input be LOW. What is the status of the Y output?



    a) LOW
    b) HIGH
    c) Don't Care
    d) Cannot be determine

16. For the device shown here, let all D inputs be LOW, both S inputs be HIGH, and the $\overline{EN}$ input be HIGH. What is the status of the Y output?



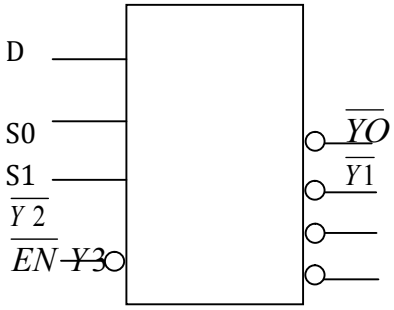
a) LOW
b) HIGH
c) Don't Care
d) Cannot be determine

17. How many 1-of-16 decoders are required for decoding a 7-bit binary number?
a) 5
b) 6
c) 7
d) 8

18. Which of the following statements accurately represents the two BEST methods of logic circuit simplification?
a) Boolean algebra and Karnaugh mapping
b) Karnaugh mapping and circuit waveform analysis
c) Actual circuit trial and error evaluation and waveform analysis
d) Boolean algebra and actual circuit trial and error evaluation

19. Which of the following combinations cannot be combined into K-map groups?
a) Corners in the same row
b) Corners in the same column
c) Diagonal corners
d) Overlapping combinations

20. The device shown here is most likely a _____.



a) Comparator
b) Multiplexer
c) Demultiplexer
d) Parity generator

21. A decoder can be used as a Demultiplexer by _____.
a) tying all enable pins LOW
b) tying all data-select lines LOW
c) tying all data-select lines HIGH
d) using the input lines for data selection and an enable line for data input

22. Which of the following combinations of logic gates can decode binary 1101?
a) One 4-input AND gate
b) One 4-input AND gate, one OR gate
c) One 4-input NAND gate, one inverter
d) One 4-input AND gate, one inverter

23. How many outputs would two 8-line-to-3-line encoders, expanded to a 16-line-to-4-line encoder, have?
a) 3 (b) 4 (c) 5 (d) 6

24. A data selector is also called a

060010104- Digital Electronics

a) De-multiplexer b) Priority encoder c) Decoder d) Multiplexer

25. A decoder is nothing but a Demultiplexer without
a) Control inputs (b) Data input (c) Enable input (d) none of these

26. A 1-of-8 octal decoder has eight outputs and decodes an input of _____ bits.
a) Three
b) Two
c) Four
d) One

27. BCD to Decimal decoder has
a) 10 inputs and 10 outputs
b) 4 inputs and 10 outputs
c) 10 inputs and 4 outputs
d) None of above

True/False

1. A digital multiplexer can be used as demultiplexer.
2. An encoder in which the highest and lowest value input digits are encoded simultaneously is known as a priority encoder.
3. Three select lines are required to address four data input lines.
4. A combinatorial logic circuit has memory characteristics that "remember" the inputs after they have been removed.
5. A data selector is also called a demultiplexer.
6. A digital circuit that converts coded information into a familiar or non-coded form is known as an encoder.
7. An exclusive-OR gate will invert a signal on one input if the other is always HIGH.
8. The following combination is correct for an EVEN parity data transmission system:
9. data = 100111100 and parity = 0
10. The CASE control structure is used when an expression has a list of possible values.
11. When decisions demand one of many possible actions, the ELSIF control structure is used.
12. The input at the 1, 2, 4, 8 inputs to a 4-line to 16-line decoder with active-low outputs is 1110. As a result, output line 7 is driven LOW.
13. A 2n-to-1 MUX can be used to implement a Boolean function with n + 1 variables.
14. Encoder is having one output line.
15. It is normal for more than one decoder output to be active at the same time.
16. The select inputs to a multiplexer may also be called address lines.
17. Basically, a multiplexer changes parallel data inputs to a serial output.
18. A four-line multiplexer must have as inputs four data inputs and two select inputs
19. A demultiplexer is a device that converts some code into a recognizable number or character.
20. The device that is an application of SOP logic is a multiplexer.

Fill in the Blanks

1. Multiplexers, demultiplexers, decoders, encoders are _____ logic circuits.
2. A multiplexer is having _____ output lines.

060010104- Digital Electronics

3. A circuit that can convert one of ten numerical keys pressed on a keyboard to BCD is a _____.
4. The largest truth table that can be implemented directly with an 8-line-to-1-line MUX has _____.
5. Parity generators and checkers use _____ gates.
6. If there are n selection lines, then the number of maximum possible input lines is ____.
7. Encoder is a combinational circuit that has 2n input lines and ____ output lines.
8. A decoder is a special case of _____ without the input line.
9. In a 1-to-16 demultiplexer, the number of control input will be _____.
10. A decoder with an enable input can function as a _____.
11. Parity generators and checkers use _____ gates.
12. Parity generation and checking is used to detect _____.
13. Parity checkers are circuits that detect ____ bit errors in the transmitted data word.
14. _____ can possibly be used for parallel-to-serial conversion.
15. Octal to binary conversion can be done using _____.
16. A 4-to-16 line decoder can be constructed using _____ line decoders having active-LOW ENABLE inputs.

UNIT5 : Flip-Flops

Short Questions

1. List out the sequential circuit.
2. List the types of flip-flops.
3. Draw block diagram of sequential circuit.
4. Define Flip Flop.
5. List two types of edge triggered flip-flops.
6. Draw a logic diagram of RS Flip-Flop with NAND gate.
7. Explain the four condition of RS Flip-Flop.
8. Draw a NOR implementation of RS Flip-Flop.
9. What do you mean by clock?
10. Define Propagation Delay.
11. What is the forbidden condition?
12. Draw a logic implementation of clocked RS Flip-Flop with its truth table.
13. What do you mean by Edge Triggered Flip-Flop?
14. What do you mean by Level Triggered Flip-Flop?
15. Give a logic implementation of positive edge triggered edge detector circuit.
16. What do you mean by frequency?
17. What is race condition?
18. List several devices that are built using J-K flip-flop.
19. Give a logic implementation of J-K Flip-Flop with PRESET & CLEAR inputs.
20. Explain the four condition of RS Flip-Flop.
21. Draw a logic diagram of Toggle Flip-Flop using J-K Flip-Flop.
22. What is D Flip-Flop?
23. What do you mean by asynchronous inputs?
24. Classify flip-flop as synchronous or asynchronous.
25. List one type of asynchronous and three types of synchronous flip-flops.

26. List the different application of flip-flop.

Long Questions

1. Draw a truth table for following flip-flops
   a) J-K
   b) D
   c) RS
   d) Clocked Rs.
2. Draw a traditional logic symbols for the following flip-flops
   a) J-K
   b) D
   c) RS
   d) Clocked Rs.
3. Explain the Master-Slave Flip-Flop. How it overcome the race condition of J-K flip-flop. Use proper logic diagram.
4. Differentiate combinational and sequential circuits.
5. Differentiate synchronous or asynchronous inputs.
6. Differentiate level-triggered and edge-triggered flip-flops.
7. Give a brief note on edge triggered flip-flop using proper logic diagrams.
8. Explain J-K flip-flop with PRESET and CLEAR inputs using proper logic diagrams and truth tables.
9. Explain J-K flip-flop using proper logic diagrams and truth tables.
10. Explain R-S flip-flop using proper logic diagrams and truth tables.
11. Explain Toggle flip-flop using proper logic diagrams and truth tables.
12. Explain Clocked R-S flip-flop using proper logic diagrams and truth tables.
13. Explain Clocked D flip-flop using proper logic diagrams and truth tables
14. Explain two applications of flip-flops other than counters and registers.
15. Explain how D flip-flop can be used to detect the sequence of edges.
16. How we can say that J-K flip-flop is a universal flip-flop. Explain using logic diagrams.
17. Explain the switch debouncing as an application of flip-flop.
18. What is a flip-flop? Show the logic implementation of R-S flip flop having active-High R and S inputs. Draw its truth table and mark the invalid entry.
19. What is a clocked J-K flip flop? What improvement does it have over a clocked R-S flip flop?
20. Differentiate D and T Flip Flop.
21. Briefly describes the following flip flop timing parameters:
    a) Set-up time and hold time;
    b) Propagation delay
    c) Maximum clock frequency.

Multiple Choice Questions

1. Which statement BEST describes the operation of a negative-edge-triggered D flip-flop?
   a) The logic level at the D input is transferred to Q on NGT of CLK.
   b) The Q output is ALWAYS identical to the CLK input if the D input is HIGH.
   c) The Q output is ALWAYS identical to the D input when CLK = PGT.

d) The Q output is ALWAYS identical to the D input.

2. Propagation delay time, tp, is measured from the _____.
   a) triggering edge of the clock pulse to the LOW-to-HIGH transition of the output
   b) triggering edge of the clock pulse to the HIGH-to-LOW transition of the output
   c) preset input to the LOW-to-HIGH transition of the output
   d) clear input to the HIGH-to-LOW transition of the output
3. How is a J-K flip-flop made to toggle?
   a) J = 0, K = 0
   b) J = 1, K = 0
   c) J = 0, K = 1
   d) J = 1, K = 1
4. How many flip-flops are required to produce a divide-by-128 device?
   a) 1
   b) 4
   c) 6
   d) 7
5. On a master-slave flip-flop, when is the master enabled?
   a) when the gate is LOW
   b) when the gate is HIGH
   c) both of the above
   d) neither of the above

6. One example of the use of an S-R flip-flop is as a(n):
   a) Racer
   b) astable oscillator
   c) binary storage register
   d) transition pulse generator
7. Which of the following is correct for a gated D flip-flop?
   a) The output toggles if one of the inputs is held HIGH.
   b) Only one of the inputs can be HIGH at a time.
   c) The output complement follows the input when enabled.
   d) Q output follows the input D when the enable is HIGH.
8. With regard to a D latch, _____.
   a) the Q output follows the D input when EN is LOW
   b) the Q output is opposite the D input when EN is LOW
   c) the Q output follows the D input when EN is HIGH
   d) the Q output is HIGH regardless of EN's input state
9. How can the cross-coupled NAND flip-flop be made to have active-HIGH S-R inputs?
   a) It can't be done.
   b) Invert the Q outputs.
   c) Invert the S-R inputs.
10. When is a flip-flop said to be transparent?
    a) when the Q output is opposite the input
    b) when the Q output follows the input
    c) when you can see through the IC packaging
11. Which of the following is correct for a D latch?
    a) The output toggles if one of the inputs is held HIGH.
    b) Q output follows the input D when the enable is HIGH.
    c) Only one of the inputs can be HIGH at a time.

d) The output complement follows the input when enabled

12. A correct output is achieved from a master-slave J-K flip-flop only if its inputs are stable while the:
a) clock is LOW
b) slave is transferring
c) flip-flop is reset
d) clock is HIGH

13. What does the triangle on the clock input of a J-K flip-flop mean?
a) level enabled
b) edge-triggered

14. On a positive edge-triggered S-R flip-flop, the outputs reflect the input condition when _____.
a) the clock pulse is LOW
b) the clock pulse is HIGH
c) the clock pulse transitions from LOW to HIGH
d) the clock pulse transitions from HIGH to LOW

15. What is the hold condition of a flip-flop?
a) both S and R inputs activated
b) no active S or R input
c) only S is active
d) only R is active

16. The circuit that is primarily responsible for certain flip-flops to be designated as edge-triggered is the:
a) edge-detection circuit.
b) NOR latch.
c) NAND latch.
d) pulse-steering circuit.

17. What is the significance of the J and K terminals on the J-K flip-flop?
a) There is no known significance in their designations.
b) The J represents "jump," which is how the Q output reacts whenever the clock goes high and the J input is also HIGH.
c) The letters were chosen in honor of Jack Kilby, the inventory of the integrated circuit.
d) All of the other letters of the alphabet are already in use.

18. Which of the following is not generally associated with flip-flops?
a) Hold time
b) Propagation delay time
c) Interval time
d) Set up time

19. What is one disadvantage of an S-R flip-flop?
a) It has no enable input.
b) It has an invalid state.
c) It has no clock input.
d) It has only a single output.

20. The output of a gated S-R flip-flop changes only if the:
a) flip-flop is set
b) control input data has changed
c) flip-flop is reset

d) input data has no change

21. An invalid condition in the operation of an active-HIGH input S-R latch occurs when _____.
    a) HIGHs are applied simultaneously to both inputs S and R
    b) LOWs are applied simultaneously to both inputs S and R
    c) a LOW is applied to the S input while a HIGH is applied to the R input
    d) a HIGH is applied to the S input while a LOW is applied to the R input

True/False

1. Flip-Flop outputs are always opposite or complementary.
2. Combinational circuit is having memory unit.
3. Flip flop is 1bit storage unit.
4. Master-slave J-K flip-flops are called pulse-triggered or level-triggered devices because input data is read during the entire time the clock pulse is at a LOW level.
5. Gated S-R flip-flops are called asynchronous because the output responds immediately to input changes.
6. Asynchronous inputs will cause the flip-flop to respond immediately with regard to the clock input.
7. For an S-R flip-flop to be set or reset, No change will occur in the output.
8. A gated S-R flip-flop goes into the SET condition when S is HIGH, R is LOW, and EN is HIGH.
9. A negative edge-triggered flip-flop will accept inputs only when the clock is LOW.
10. The term CLEAR always means that Q = 0, $\overline{Q}$ = 1.
11. PRESET and CLEAR inputs are normally synchronous.
12. The Q output of a flip-flop is normally HIGH when the device is in the "CLEAR" or "RESET" state.
13. An input which can only be accepted when an enable or trigger is present is called asynchronous.
14. Inputs that cause the output of a flip-flop to change instantaneously are asynchronous.
15. The J-K flip-flop eliminates the invalid state by toggling when both inputs are high and the clock transitions.
16. A D-type latch is able to change states and "follow" the D input regardless of the level of the ENABLE input.
17. A positive edge-triggered flip-flop changes states with a HIGH-to-LOW transition on the clock input.
18. A D latch has one data-input line.
19. Edge-triggered flip-flops can be identified by the triangle on the clock input.
20. The S-R flip-flop has no invalid or unused state.
21. Some flip-flops have invalid states.
22. Simple gate circuits, combinational logic, and transparent S-R flip-flops are synchronous.
23. A flip-flop is in the CLEAR condition when Q = 1, $\overline{Q}$ = 0.
24. Pulse-triggered or level-triggered devices are the same.
25. A D flip-flop is constructed by connecting an inverter between the SET and clock

terminals.

26. It takes four flip-flops to act as a divide-by-4 frequency divider.
27. Flip-flops are wired together to form counters registers and memory devices.

Fill in the Blanks

1. _____ are the basic building blocks of combinational logic circuits.
2. _____ are the basic building blocks of sequential logic circuits.
3. The "D" in flip-flop stands for _____ or data.
4. f an active-HIGH S-R latch has a 0 on the S input and a 1 on the R input and then the R input goes to 0, the latch will be _____.
5. On a J-K flip-flop, when is the flip-flop in a hold condition J = _____ , K = _____.
6. If an input is activated by a signal transition, it is _____.
7. For an S-R flip-flop to be set or reset, the respective input must be _____.S
8. Assume a J-K flip-flop has 1s on the J and K inputs. The next clock pulse will cause the output to _____.
9. In synchronous systems, the exact times at which any output can change state are determined by a signal commonly called the _____.
10. When the output of the NOR gate S-R flip-flop is Q = 0 and , the inputs are _____, _____.
11. A major drawback to an SR Flip Flop is its _____.
12. When the output of the NOR gate S-R flip-flop is in the HOLD state (no change), the inputs are _____.
13. The signal used to identify edge-triggered flip-flops is _____.
14. An edge-triggered flip-flop can change states only when _____.
15. When both inputs of a J-K pulse-triggered FF are high and the clock cycles, the output will _____.
16. The term hold always means _____.
17. A gated S-R flip-flop goes into the CLEAR condition when _____.
18. If an input is activated by a signal transition, it is _____.
19. A flip-flop operation is described as a toggle when the result after a clock is _____.
20. A positive edge-triggered flip-flop will accept inputs only when the clock _____.
21. The advantage of a J-K flip-flop over an S-R FF is that _____.
22. A S-R flip-flop is in the hold condition whenever _____.
23. The toggle mode is the mode in which a(n) _____ changes states for each clock pulse.

UNIT6 : Counters and Registers

Short Questions

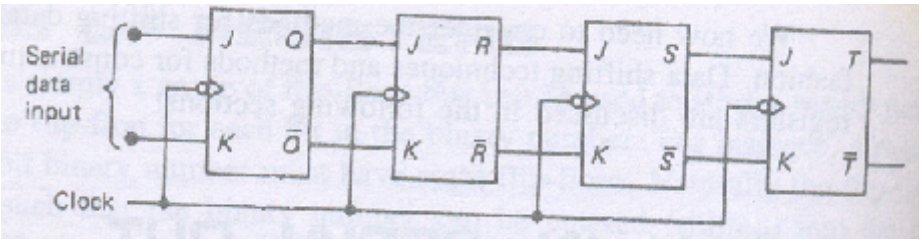
1. What do you mean by serial shifting?
2. Define modulus of counter.
3. Is counter is a sequential circuit or combinational circuit or sequential circuit with or without combination logic devices?
4. To shift 4 bit binary data out from SISO shift register what will be the input bits to a shift register?
5. What do you mean by modulus of counter?

060010104- Digital Electronics

6. Give the steps to design cascading decoder circuits. Also provide logic diagram.
7. Why asynchronous counters are also known as serial counters?
8. In what type of shift register complete binary number can be loaded into it in one operation and then have shifted out one bit at a time?
9. In what type of shift register data can be entered only one bit at a time but has all data bits available as outputs?
10. What are counters with arbitrary counts sequence?
11. Give at least one IC type number for four bit binary ripple counter.
12. Give at least one IC type number for four bit synchronous counter.
13. Give at least one IC type number for eight bit serial-in, serial-out shift register.
14. Give at least one IC type number for bidirectional universal shift register.

Long Questions

1. Define parallel counters. Draw the logic diagram for synchronous counter that count from 0000 to 1111. Explain how it counts the numbers.
2. Differentiate combinational circuits and sequential circuits.
3. Is PRESET & CLEAR are asynchronous inputs? Justify your answer.
4. Draw logic diagram for 4 bit Parallel In Parallel Out shift register and explain how it is used to shift data serially.
5. Draw the waveforms to shift the binary number 1010 into the register in Fig.1.



6. Name the four basic types of shift register, and draw a block diagram for each.
7. Differentiate between asynchronous and synchronous counter.
8. Differentiate between UP, DOWN and UP/DOWN counter.
9. Differentiate between Presentable and clearable counter.
10. Differentiate between BCD and Decade counter.
11. What is the difference between four-bit binary UP and four-bit binary DOWN counter?
12. How does architecture of an asynchronous UP counter differ from that of DOWN counter?
13. Why is maximum usable clock frequency in case of synchronous counter independent of that of size of counter?
14. What do you mean by shift register? Explain the Serial-In-Serial-Out shift register.
15. Design a Mod-10 counter. Also draw the timing waveforms.
16. Explain parallel counters. Give the circuit representation of 4-bit synchronous counter and explain its working.
17. What are counters with arbitrary counts sequence? Briefly describe the producers for designing a counter with a given arbitrary count sequence.

060010104- Digital Electronics

Multiple Choice Questions

1. The minimum number of flip-flops needed to construct a BCD decade counter is
   a) 4
   b) 3
   c) 10
   d) 2
2. A shift counter comprising five flip-flops with an inverse feedback from the output of MSB flip-flop to the input of the LSB flip-flop is a
   a) Divide-by-32- counter
   b) Divide-by-10- counter
   c) Divide-by-5- counter
   d) Five-bit shift counter
3. On the fifth clock pulse, a 4-bit Johnson sequence is Q0 = 0, Q1 = 1, Q2 = 1, and Q3 = 1. On the sixth clock pulse, the sequence is _____.
   a) Q0 = 1, Q1 = 0, Q2 = 0, Q3 = 0
   b) Q0 = 1, Q1 = 1, Q2 = 1, Q3 = 0
   c) Q0 = 0, Q1 = 0, Q2 = 1, Q3 = 1
   d) Q0 = 0, Q1 = 0, Q2 = 0, Q3 = 1
4. The bit sequence 0010 is serially entered (right-most bit first) into a 4-bit parallel out shift register that is initially clear. What are the Q outputs after two clock pulses?
   a) 0000
   b) 0010
   c) 1000
   d) 1111
5. What is a shift register that will accept a parallel input, or a bidirectional serial load and internal shift features, called?
   a) tristate
   b) end around
   c) universal
   d) conversion
6. On the third clock pulse, a 4-bit Johnson sequence is Q0 = 1, Q1 = 1, Q2 = 1, and Q3= 0. On the fourth clock pulse, the sequence is _____.
   a) Q0 = 1, Q1 = 1, Q2 = 1, Q3 = 1
   b) Q0 = 1, Q1 = 1, Q2 = 0, Q3 = 0
   c) Q0 = 1, Q1 = 0, Q2 = 0, Q3 = 0
   d) Q0 = 0, Q1 = 0, Q2 = 0, Q3 = 0
7. A bidirectional 4-bit shift register is storing the nibble 1101. Its $\overline{\text{RIGHT/LEFT}}$ input is HIGH. The nibble 1011 is waiting to be entered on the serial data-input line. After three clock pulses, the shift register is storing _____.
   a) 1101
   b) 0111
   c) 0001
   d) 1110
8. How can parallel data be taken out of a shift register simultaneously?
   a) Use the Q output of the first FF.
   b) Use the Q output of the last FF.

c) Tie all of the Q outputs together.
d) Use the Q output of each FF.

9. What is meant by parallel load of a shift register?
a) All FFs are preset with data.
b) Each FF is loaded with data, one at a time.

10. How many flip-flops are required to make a MOD-32 binary counter?
a) 3
b) 45
c) 5
d) 6

11. Using four cascaded counters with a total of 16 bits, how many states must be deleted to achieve a modulus of 50,000?
a) 50,000
b) 65,536
c) 25,536
d) 15,536

12. The terminal count of a modulus-11 binary counter is _____.
a) 1010
b) 1000
c) 1001
d) 1100

13. Synchronous counters eliminate the delay problems encountered with asynchronous counters because the:
a) input clock pulses are applied only to the first and last stages
b) input clock pulses are applied only to the last stage
c) input clock pulses are not used to activate any of the counter stages
d) input clock pulses are applied simultaneously to each stage

14. What is the difference between combinational logic and sequential logic?
a) Combinational circuits are not triggered by timing pulses, sequential circuits are triggered by timing pulses.
b) Combinational and sequential circuits are both triggered by timing pulses.
c) Neither circuit is triggered by timing pulses.

15. A BCD counter is a _____.
a) Binary counter.
b) Full-modulus counter.
c) Decade counter.
d) Divide-by-10 counter.

16. A five bit counter
a) Has a modulus of 5.
b) Has a modulus of 2.
c) Has modulus that is less than or equal to 32.
d) Cant not have a modulus that is greater than 32.
e) Both c and d are true.

17. All BCD counters
a) Are decade counters because all decades counters are BCD counters.
b) Are not decade's counters.
c) Have a modulus of 10.
d) Are constructed with only presettable D flip-flops.

18. A counter that has a modulus of 64 should use minimum of

060010104- Digital Electronics

a) 6 flip-flops
b) 6 J-K type flip-flops
c) 6 D flip-flops
d) 64 flip-flops

19. A MOD-32 binary synchronous counter would require
a) 6 flip-flops and 3 AND gates
b) 5 flip-flops
c) 5 flip-flops and 3 AND gates
d) None of these

20. In what type of shift register do we have access to only the leftmost and rightmost flip-flops?
a) Serial-in serial-out shift register
b) Serial-in parallel-out shift register
c) Parallel-in serial-out shift register
d) Parallel-in Parallel-out shift register

True/False

1. Bidirectional shift registers can shift data either right or left.
2. In many cases, counters must be strobed in order to eliminate glitches.
3. A state diagram is a table of states.
4. A ripple counter is an asynchronous counter.
5. The MOD number of a Johnson counter will always be equal to one-half the number of flip-flops in the counter.
6. To cascade is to connect in parallel.
7. Cascade means to connect the Q output of one flip-flop to the clock input of the next.
8. In a synchronous counter, each state is clocked by the same pulse.
9. Basic counters can be cascaded in parallel to increase the number of data bits that the counter can handle.
10. Dependency notation is no longer used.
11. A parallel in/serial out shift register enters all data bits simultaneously and transfers them out one bit at a time.
12. Generally speaking, the synchronous counter requires more circuitry than an asynchronous counter.
13. Another term used to describe up/down counters is bidirectional.
14. When implementing a complete system application using IC counter chips, output devices such as LED indicators must be configured to operate from the counter outputs.
15. One of the stages in a register consists of a latch.
16. There are several ways to construct a stepper motor to achieve digitally controlled stepping action. One possibility is to construct four stator coils set up as four pole pairs, each 45° apart and using three ferromagnetic pairs spaced 60° apart.

Fill in the Blanks

1. Assume a LOW logic level is placed on the SHIFT/LOAD input of a 74195 shift register. The output will change _____.
2. A Johnson counter, constructed with N flip-flops, has _____unique states?

060010104- Digital Electronics

3. A type of shift register that requires access to the Q outputs of all stages is _____.
4. An 8-bit serial in/parallel out shift register is clocked at 4 MHz and is used to delay a serial digital signal by 1.25 μs. The output that has the proper delay is _____.
5. A 4-bit ring counter is loaded with a single 1. The frequency of any given output is _____.
6. Shifting a binary number to the left by one position is equivalent to _____.
7. Assume a 4-bit Johnson counter is initially cleared. After the first clock pulse the output is 0001. After the next clock pulse the output will be _____.
8. A reliable method for eliminating decoder spikes is the technique called _____.
9. A decade counter will count through decimal _____.
10. _____ counters are often used whenever pulses are to be counted and the results displayed in decimal.
11. The technique used by one-shots to respond to an edge rather than a level is called _____.
12. A J-K flip-flop is reset and must stay reset after the clock pulse. This transition requires that _____.
13. The _____ counter in the Altera library has controls that allow it to count up or down, and perform synchronous parallel load and asynchronous cascading.
14. A BCD counter has _____ states.
15. The decimal equivalent of the largest number that can be stored in a 4-bit binary counter is _____.