THE NATIONAL UNIVERSITY OF LESOTHO

Department of Mathematics and Computer Science

CS3520 - Computer Organisation and Architecture I

Microarchitecture Design Template

26th October 2025

1. Introduction

Briefly restate your processor's context and target application domain:

- **Reference ISA:** Briefly provide an overview of your ISA which underpin this microarchitecture design.
- **Supported Instruction Classes:** State the classes that your ISA supports.
- **Design Objective:** State your main design goals (e.g., minimize CPI, support low power, enable simple pipeline implementation).

2. Incremental Datapath Design

You will design the datapath incrementally for each instruction format in your ISA. For each class, draw and describe only the components needed to correctly execute that class. For each format:

- Provide a block diagram (partial datapath).
- Annotate all data flows and key control signals.
- Include a one-paragraph explanation of how an instruction of this format executes.

3. Unified Single-Cycle Datapath

After designing each format, combine all into a single unified datapath capable of executing all instruction types.

4. Control Unit Design

Incorporate control unit and signals and truth table which describes how signals are set for each instruction class.

5. Pipelined Implementation

Convert your single-cycle datapath into an n-stage pipeline:

- Update datapath diagram with new elements and additional control paths.
- Discuss data hazards (forwarding or stalling), control hazards, and any pipeline optimizations you propose.

6. Memory Hierarchy Design

Describe the memory hierarchy for your processor.

7. Conclusion

Conclude with a short reflection.

8. References

List all references used.