CME1214 Logic Design
Experiment 3

1. The following function is given. Implement it using a 3x8 multiplexer.

$$F\,(A, B, C, D) = \prod (0, 2, 5, 9, 11, 14$$
$$d\ (don't\ care)\ (A, B, C, D) = \sum (3, 8, 10, 15)$$

2. Design a circuit that displays the prime and non-prime integers between 0-7. Use a 3x8 Demultiplexer(DEMUX) and 2-input AND gates to implement the design.

$$_{F1}(A, B, C) = \sum (0, 1, 4, 6)$$
$$_{F2}(A, B, C) = \sum (2, 3, 5, 7)$$

Preliminary Work

Draw truth tables, Karnaugh maps, logic diagrams and waveforms of the design. Construct and test the designed circuit in Altera Quartus II. Bring the logic diagrams and waveforms.
Come with your PreLab report and data sheets of the ICs you used in your designs.
Prepare the PreLab report **individually**.

Equipments

- 74LS151 (Multiplexer), 74LS138 (DeMultiplexer) and other necessary ICs such as Inverter, OR, AND
- Breadboard
- Connection cables