CME1214 Logic Design
Lab 2

Preliminary Work

1. Examine function F and
   a. Draw the truth table of F and then simplify F using Karnaugh map.
   b. Use Altera Max+Plus II to implement logic design of F.
   c. Simulate your circuit and verify that it works correctly using the waveform.

$$F(a, b, c, d) = \sum(0, 1, 2, 3, 4, 5, 6, 7, 8, 9, 11)$$

   (See sample Sum of Product (SOP) solutions)

2. Design a **2-bits full adder** circuit using logic gates.
   (exp. 01+01=010, discard initial *carry in* bit)
   - Give the truth tables and Karnaugh maps of the designs.
   - Use Altera Max+Plus II to implement your designs.
   - Simulate your circuits and verify that they work correctly using the waveform.

3. Prepare preliminary work report
   The PreLab report should include truth tables, logic diagrams, Karnaugh maps, waveforms and all other preliminary works.

The preliminary work and report are expected from each student **individually**. Please upload your reports on classroom page. Bring your reports and necessary datasheets of the ICs to lab course.

Equipment

- AND (IC 7408), OR (IC 7432), NOT (IC 7414), XOR (IC 7486)
- Breadboard
- Connection cables
- Any other equipment necessary for the experiments.

Lab Work

1. Simplify the Boolean function F and implement it by using integrated circuits(IC).
2. Implement 2-bits full adder circuits by using ICs.