CREATING AND DEPLOYING AN OPEN STANDARD SPI ON AN FPGA, INVOLVING C BASED TEST CASE DEVELOPMENT FOR EMULATION

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UNDER THE GUIDANCE OF

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&

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OUTLINE:

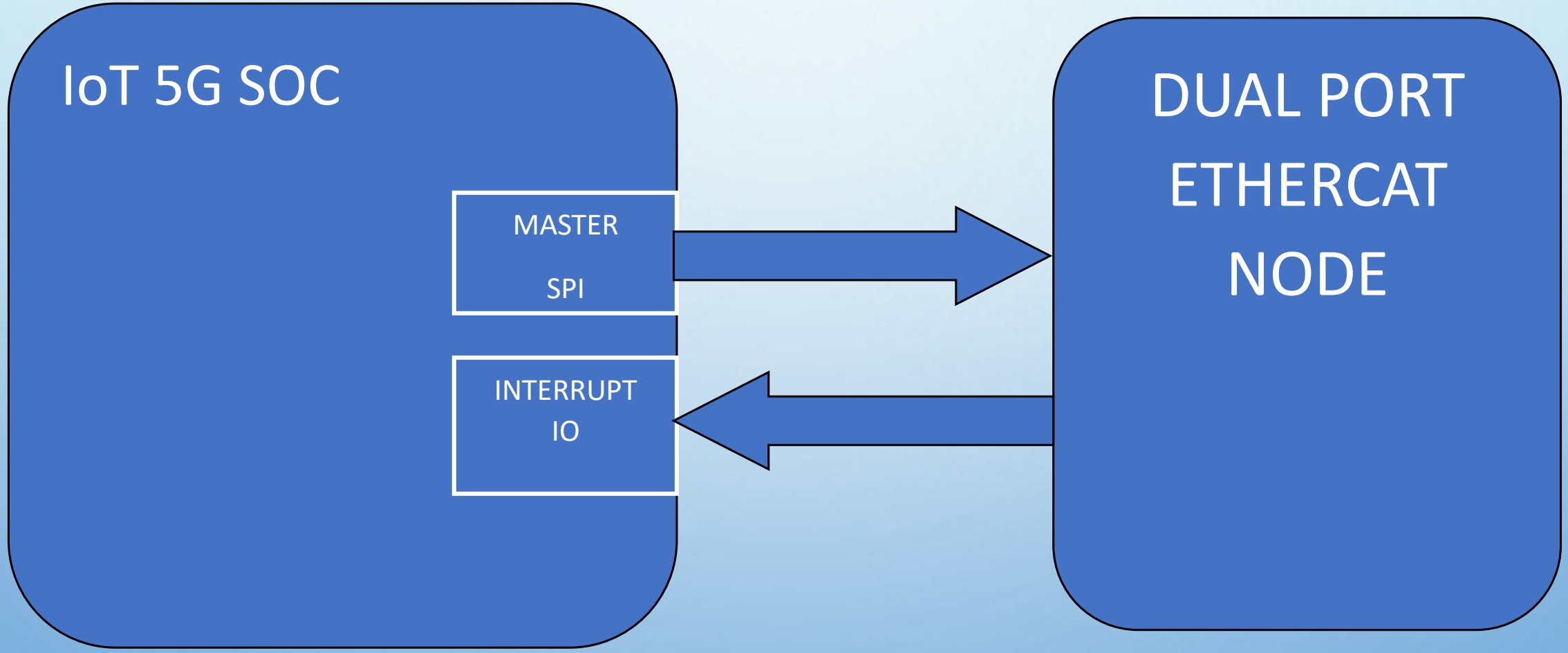
- OUTLINE OF THIS DISSERTATION IS TO DESIGN A SIMPLE SOC WITH A CUSTOM IP (SPI) AND REQUIRED ECOSYSTEM TO VALIDATE THE IP AND PORTRAIT THE IP QUALIFICATION KPIS. IT ALSO INCLUDES THE C BASED TESTCASES TO MEASURE THE KPIS AND TEST SPECIFICATIONS AND TESTCASE DEVELOPMENT.
- TO VERIFY THE DIGITAL LOGIC, SOC DESIGN WILL BE SYNTHESIZED FOR FPGA PLATFORM WHERE THE GATE LOGICS ARE IMPLEMENTED AS CLOSE AS DESIRED SOC.
- THE ADVANTAGE OF FPGA BASED EMULATION IS, EXECUTION OF TESTCASES WILL BE FASTER AS SILICON WHEN COMPARED TO DV PLATFORM. THE ONLY CONSTRAINT IS, IT NEEDS SOME MODIFICATIONS IN RTL TO MEET THE TIMINGS IN THE FPGA. THESE MODIFICATIONS WILL NOT AFFECT THE FUNCTIONALITY OF THE RTL IN THE SILICON.

OBJECTIVE:

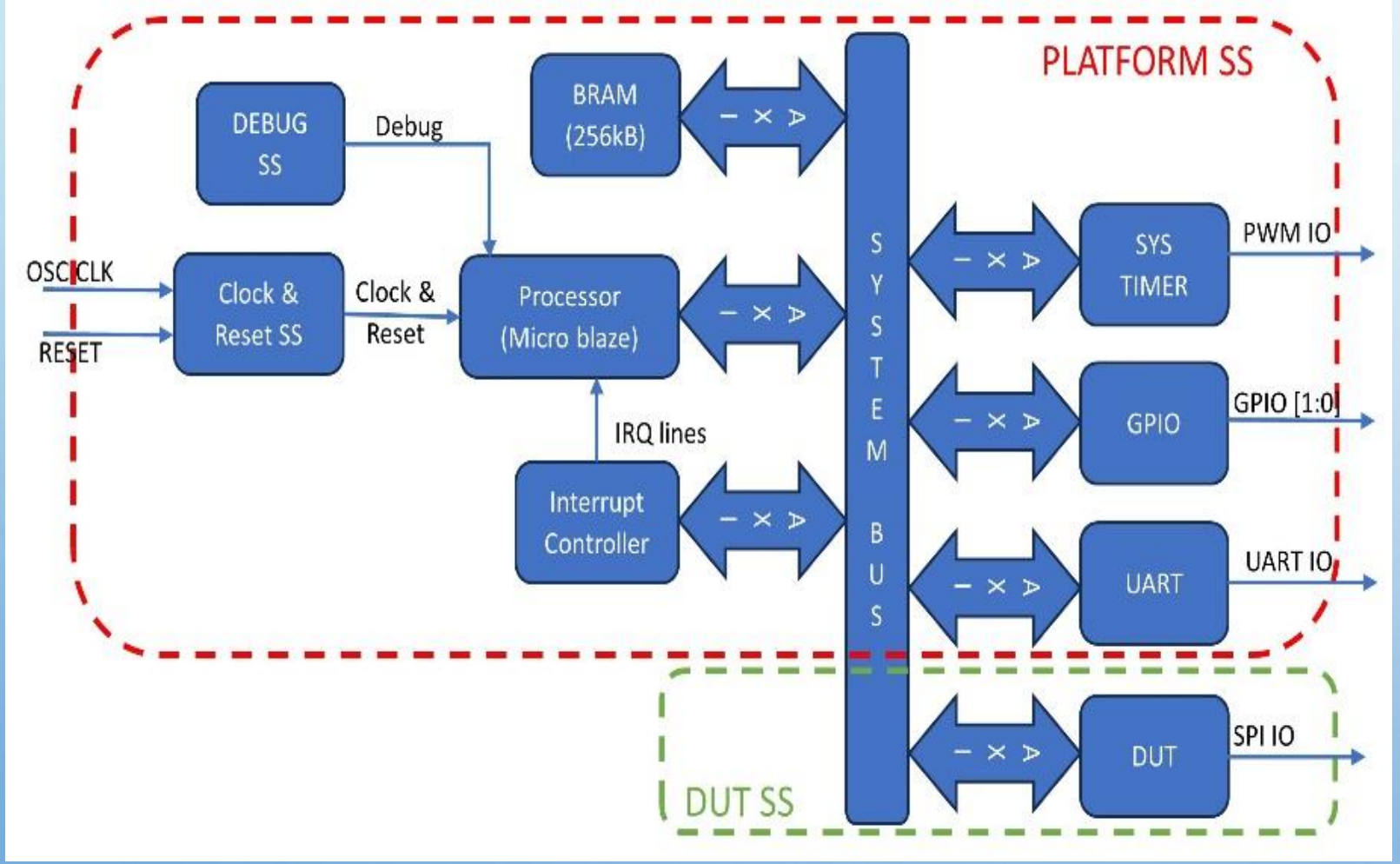
THE OBJECTIVES OF MY PROJECT ARE AS FOLLOWS:

- CREATING A CUSTOM SPI IP FROM XILINX IP INTEGRATOR
- CREATING AN ECOSYSTEM TO VALIDATE THIS IP
- UNDERSTANDING THE HARDWARE SPECIFICATION OF IP
- WRITING A TEST SPEC FROM THE HARDWARE SPECIFICATION
- CREATING THE TESTCASES TO QUALIFY THE IP
- COLLECTING THE OUTPUT WAVEFORMS FROM THE XILINX ILA

USE CASE OF THE IP

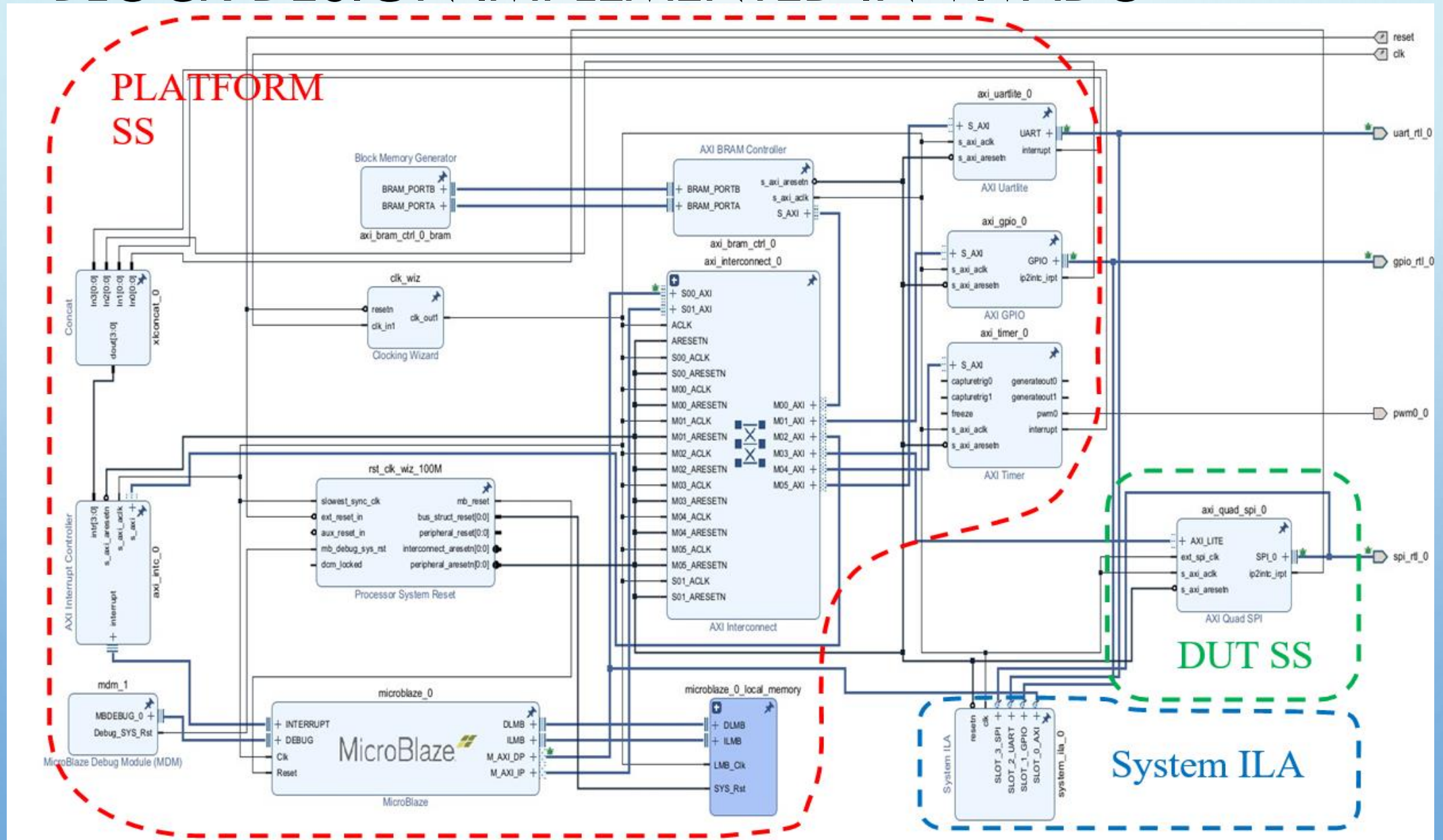


BLOCK DIAGRAM:

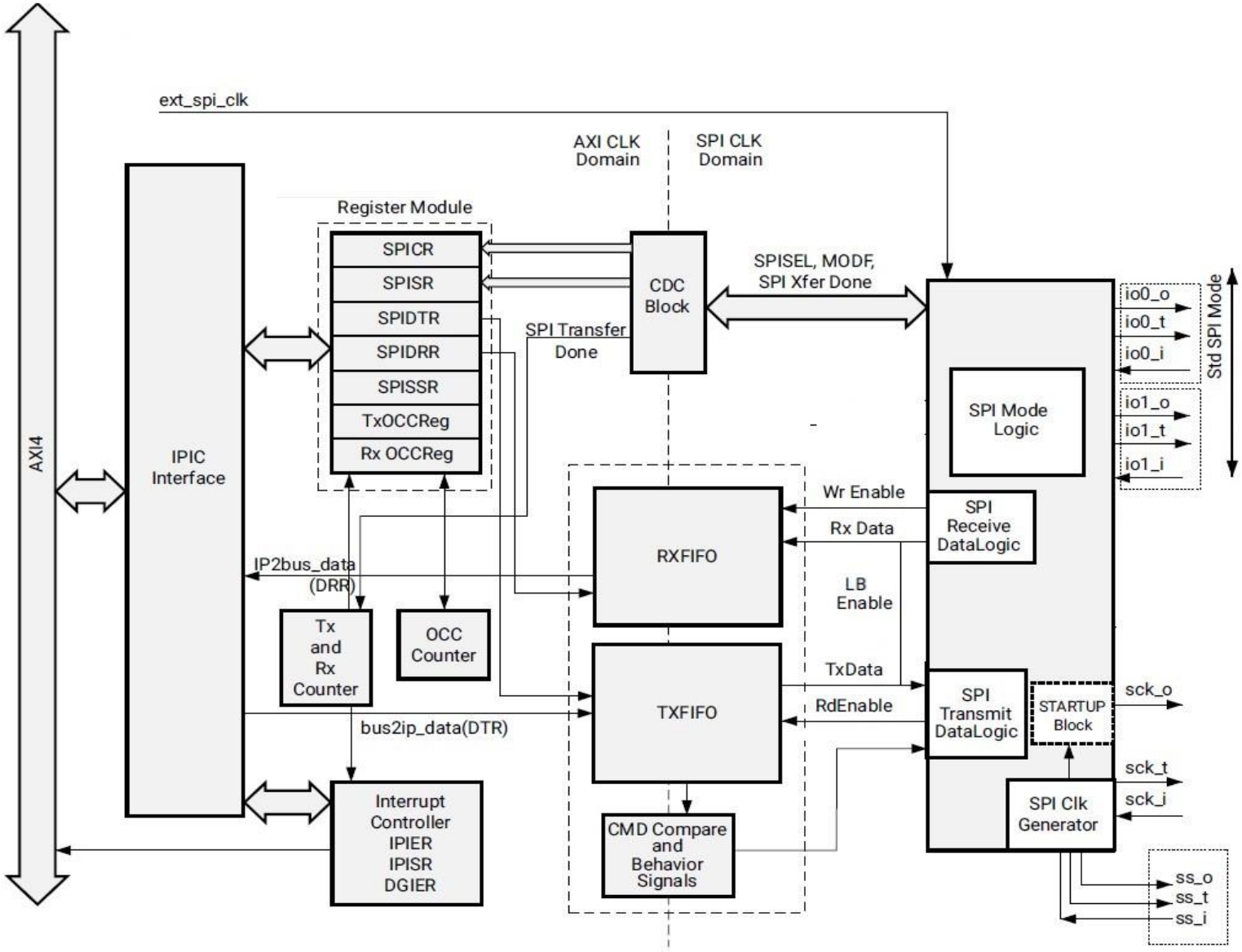


Xilinx IP Used	Address map	Size
clk_wiz:6.0\	NA	
microblaze:11.0\	NA	
mdm:3.2\	NA	
proc_sys_reset:5.0\	NA	
axi_gpio:2.0\	0x40000000	1kB
axi_bram_ctrl:4.1\	NA	
blk_mem_gen:8.4\	0xC0000000	512kB
xlconcat:2.1\	NA	
axi_intc:4.1\	0x41200000	1kB
axi_uartlite:2.0\	0x40600000	1kB
system_ila:1.1\	NA	
axi_timer:2.0\	0x41C00000	1kB
lmb_v10:3.0\	0x00000000	16kB
axi_quad_spi:3.2\	0x44A00000	4kB

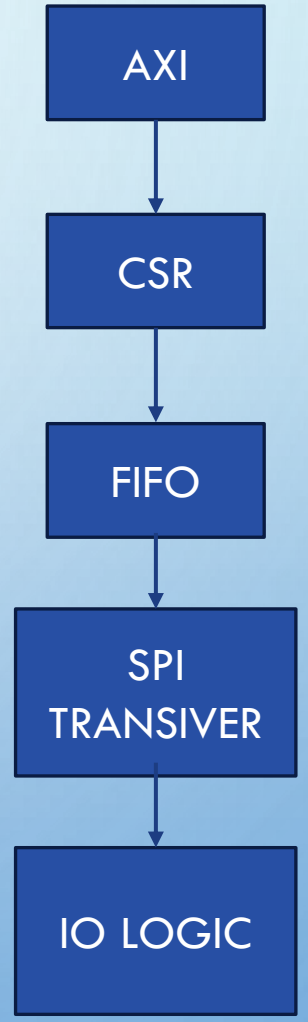
BLOCK DESIGN IMPLEMENTED IN VIVADO



BLOCK DIAGRAM OF SPI



DATA FLOW DIAGRAM:



UTILIZATION REPORT

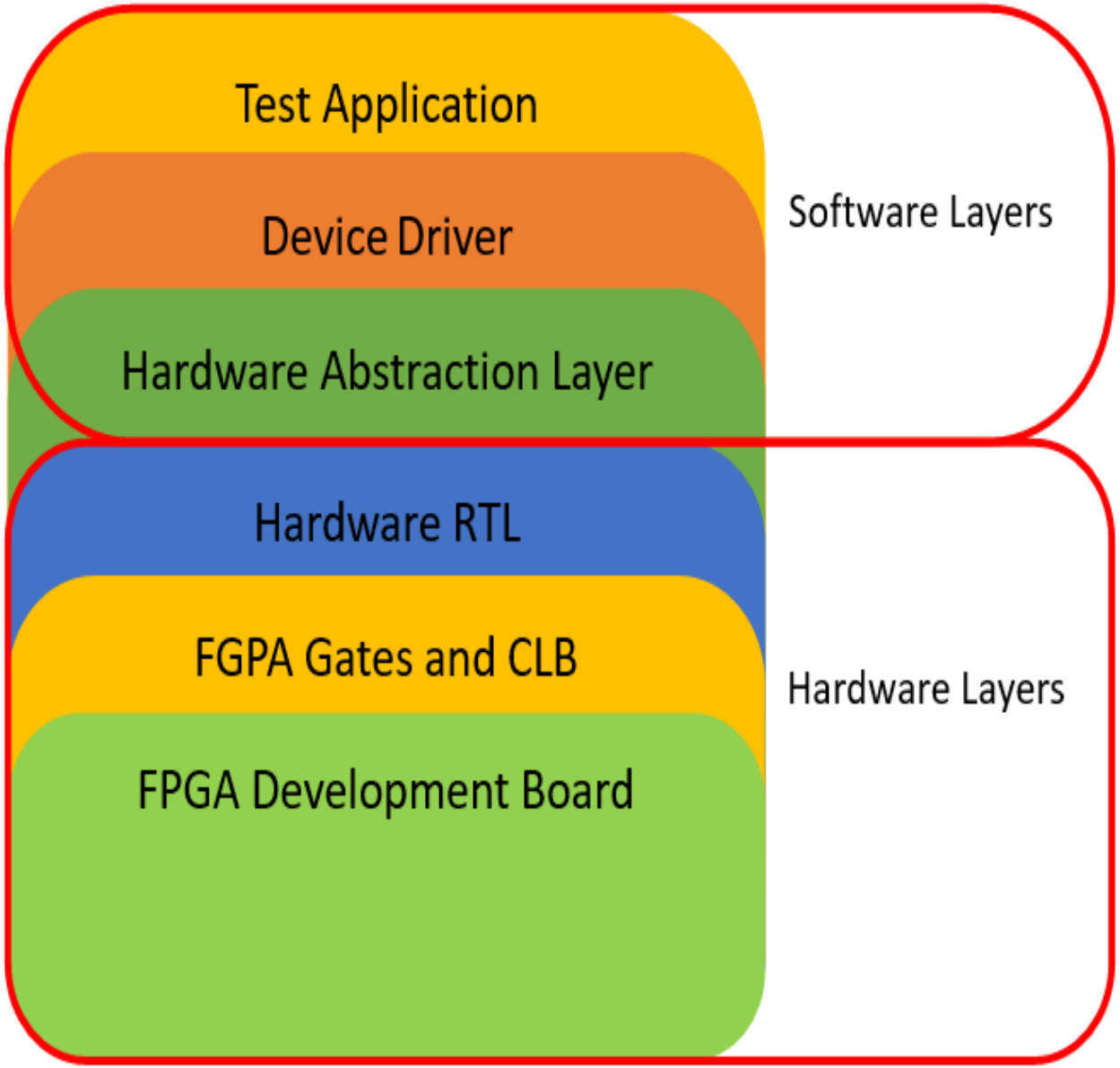
LIVE BOARD

Name	CLB LUTs (117120)	CLB Registers (234240)	CARRY8 (14640)	F7 Muxes (58560)	CLB (14640)	LUT as Logic (117120)	LUT as Memory (57600)	Block RAM Tile (144)	Bonded IOB (189)	HPIOB_M (58)	HPIOB_S (58)	HDIOB_M (35)	HDIOB_S (35)	GLOBAL CLOCK BUFFERs (352)
Microblaze_MPU_wrapper	5716	5954	65	117	1192	5046	670	142	13	3	1	5	4	4
Microblaze_MPU_i (Microblaze_MPU)	5716	5954	65	117	1192	5046	670	142	0	0	0	0	0	4
axi_bram_ctrl_0 (Microblaze_MPU_a	202	239	0	2	69	202	0	0	0	0	0	0	0	0
axi_bram_ctrl_0_bram (Microblaze_I	89	5	0	0	81	89	0	128	0	0	0	0	0	0
axi_bram_ctrl_0_bram1 (Microblaze_	4	0	0	0	3	4	0	8	0	0	0	0	0	0
axi_bram_ctrl_1 (Microblaze_MPU_a	225	241	0	2	64	225	0	0	0	0	0	0	0	0
axi_gpio_0 (Microblaze_MPU_axi_gp	63	103	0	0	25	63	0	0	0	0	0	0	0	0
axi_intc_0 (Microblaze_MPU_axi_intc	81	90	0	0	20	81	0	0	0	0	0	0	0	0
axi_quad_spi_0 (Microblaze_MPU_a	386	624	0	0	99	366	20	0	0	0	0	0	0	0
axi_smc (Microblaze_MPU_axi_smc_	2413	2725	0	4	508	1994	419	0	0	0	0	0	0	0
axi_timer_0 (Microblaze_MPU_axi_ti	291	244	40	0	77	291	0	0	0	0	0	0	0	0
axi_uartlite_0 (Microblaze_MPU_axi_	98	108	0	1	26	80	18	0	0	0	0	0	0	0
clk_wiz_0 (Microblaze_MPU_clk_wiz_	0	0	0	0	0	0	0	0	0	0	0	0	0	1
mdm_0 (Microblaze_MPU_mdm_0_	88	110	0	0	25	81	7	0	0	0	0	0	0	3
microblaze_0 (Microblaze_MPU_mic	1538	1299	25	108	319	1333	205	6	0	0	0	0	0	0
microblaze_0_axi_periph (Microblaze	233	132	0	0	80	233	0	0	0	0	0	0	0	0
rst_clk_wiz_0_100M (Microblaze_MP	14	34	0	0	6	13	1	0	0	0	0	0	0	0
xlconcat_0 (Microblaze_MPU_xlconca	0	0	0	0	0	0	0	0	0	0	0	0	0	0

DEMO BOARD

Name	Slice LUTs (63400)	Slice Registers (126800)	F7 Muxes (31700)	Slice (15850)	LUT as Logic (63400)	LUT as Memory (19000)	Block RAM Tile (135)	Bonded IOB (170)	ILOGIC (170)	BUFGCTRL (32)	PLLE2_ADV (6)	BSCANE2 (4)
Microblaze_wrapper	4220	4995	115	1903	3919	301	78	11	2	6	1	2
dbg_hub (dbg_hub)	450	741	0	241	426	24	0	0	0	1	0	1
inst (xsdbm_v3_0_0_xs	450	741	0	241	426	24	0	0	0	1	0	1
Microblaze_i (Microblaze)	3770	4254	115	1668	3493	277	78	0	2	5	1	1
axi_bram_ctrl_0 (Microbl	220	238	2	116	220	0	0	0	0	0	0	0
axi_bram_ctrl_0_bram (	54	1	0	42	54	0	64	0	0	0	0	0
axi_gpio_0 (Microblaze_	67	93	0	31	67	0	0	0	0	0	0	0
axi_intc_0 (Microblaze_a	82	90	0	29	82	0	0	0	0	0	0	0
axi_interconnect_0 (Micr	242	132	0	111	242	0	0	0	0	0	0	0
axi_quad_spi_0 (Microbl	359	543	0	166	347	12	0	0	2	0	0	0
axi_timer_0 (Microblaze_	293	244	0	114	293	0	0	0	0	0	0	0
axi_uartlite_0 (Microblaz	88	107	1	40	78	10	0	0	0	0	0	0
clk_wiz (Microblaze_clk_	0	0	0	0	0	0	0	0	0	3	1	0
mdm_1 (Microblaze_md	93	110	0	44	86	7	0	0	0	2	0	1
microblaze_0 (Microblaz	1160	1021	108	472	1042	118	0	0	0	0	0	0
microblaze_0_local_me	16	14	0	12	14	2	8	0	0	0	0	0
rst_clk_wiz_100M (Micro	18	38	0	14	17	1	0	0	0	0	0	0
system_ila_0 (Microblaz	1081	1623	4	555	954	127	6	0	0	0	0	0
xlconcat_0 (Microblaze_	0	0	0	0	0	0	0	0	0	0	0	0

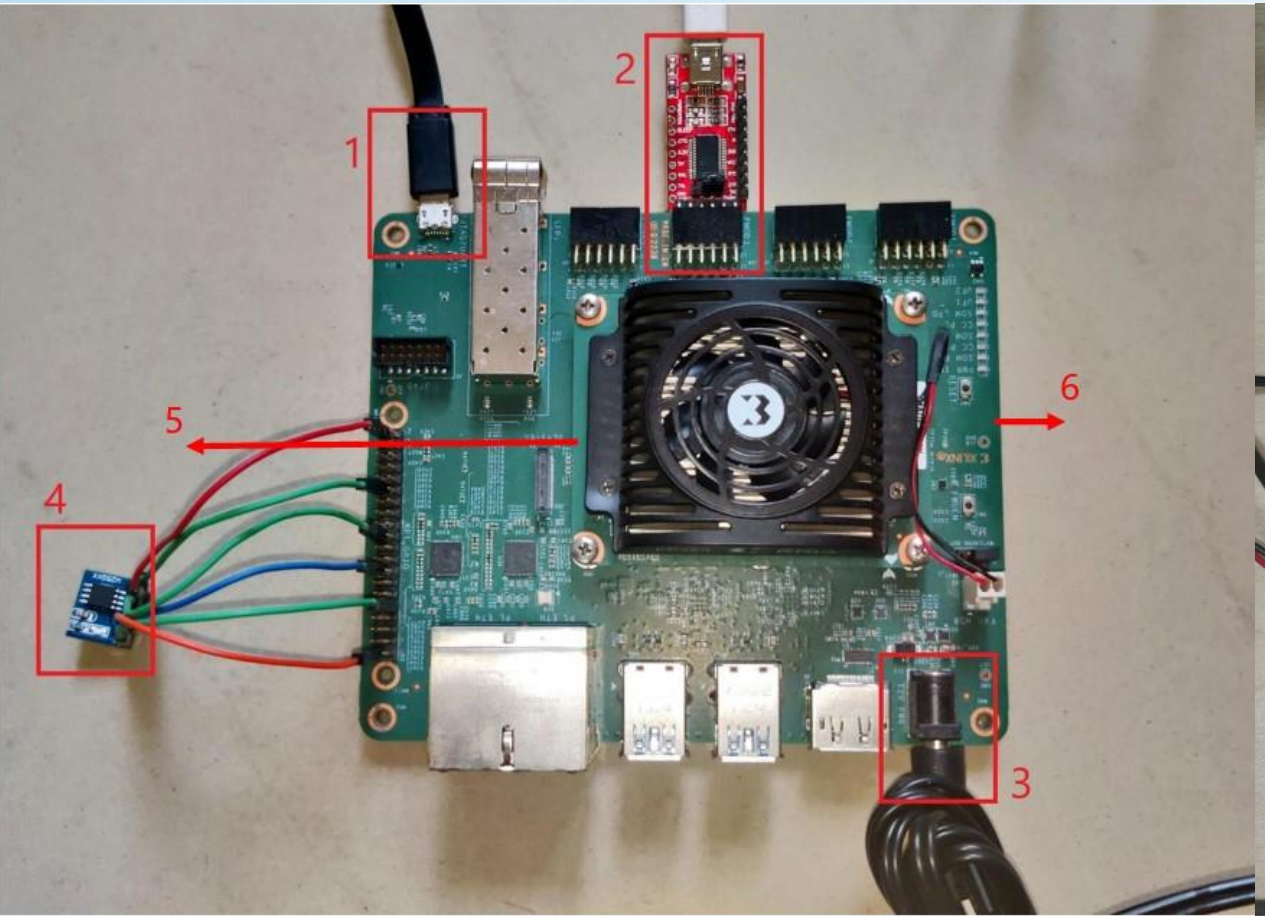
LAYERS OF IMPLEMENTATION



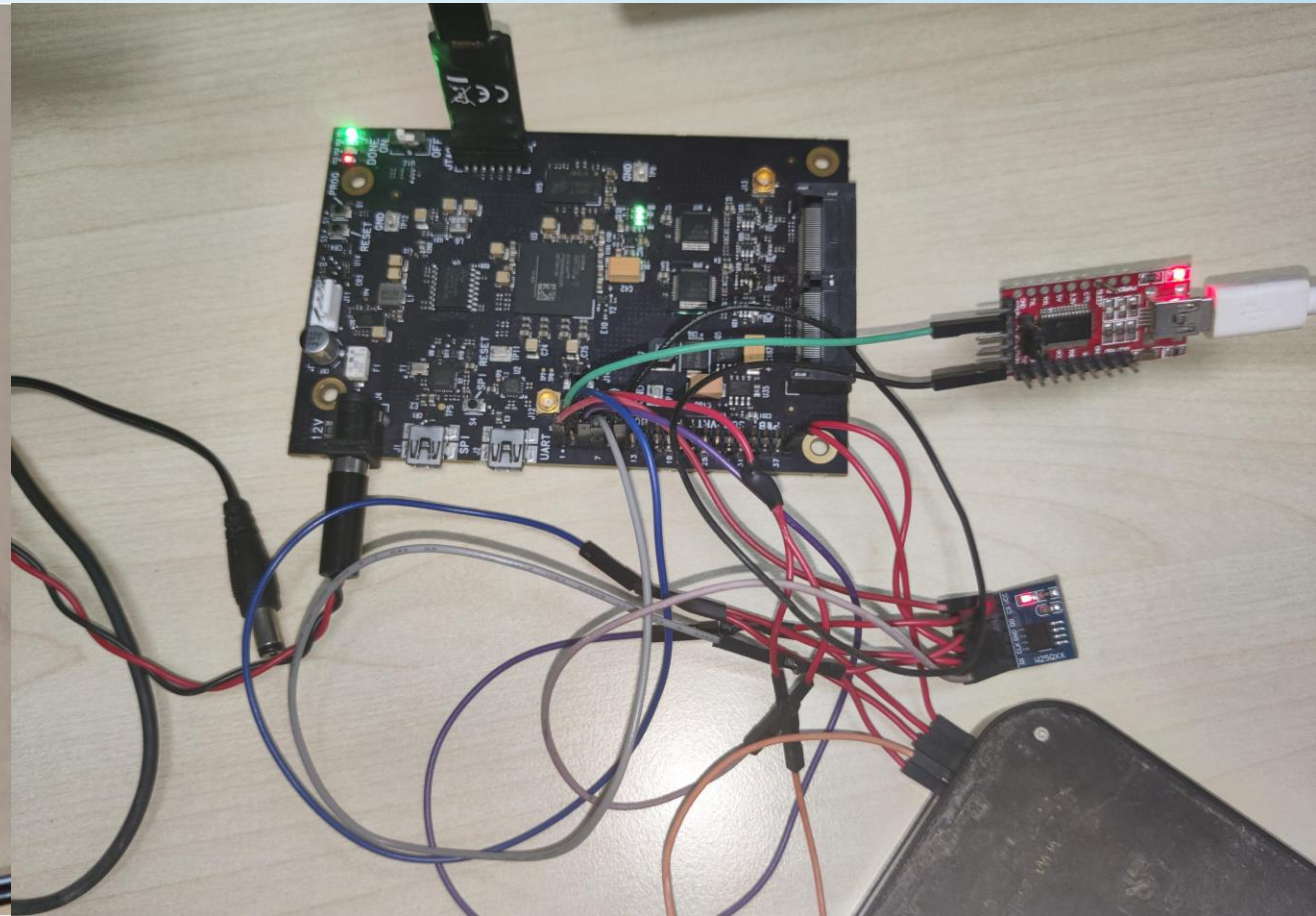
- TEST APPLICATION
  - SIP LOOPBACK AND FLASH TESTCASE
- DEVICE DRIVER
  - SPI IP AND FLASH DRIVER AND PLATFORM DRIVERS
- HARDWARE ABSTRACTION LAYER
  - ALL REGISTER DEFINITION C MACROS OF ALL IP
- RTL
  - THIS IS THE BLOCK DESIGN GENERATED AND SYNTHESIZED FROM VIVADO
- FPGA HARWARE:
  - REAL HARDWARE WHERE THE BITSTREAM FILE IS FLASHED
- FPGA BOARD
  - THE BOARD WHERE THE FPGA IC IS SOLDERED AND CONNECTED TO PERIPHERALS

HARDWARE SETUPS:

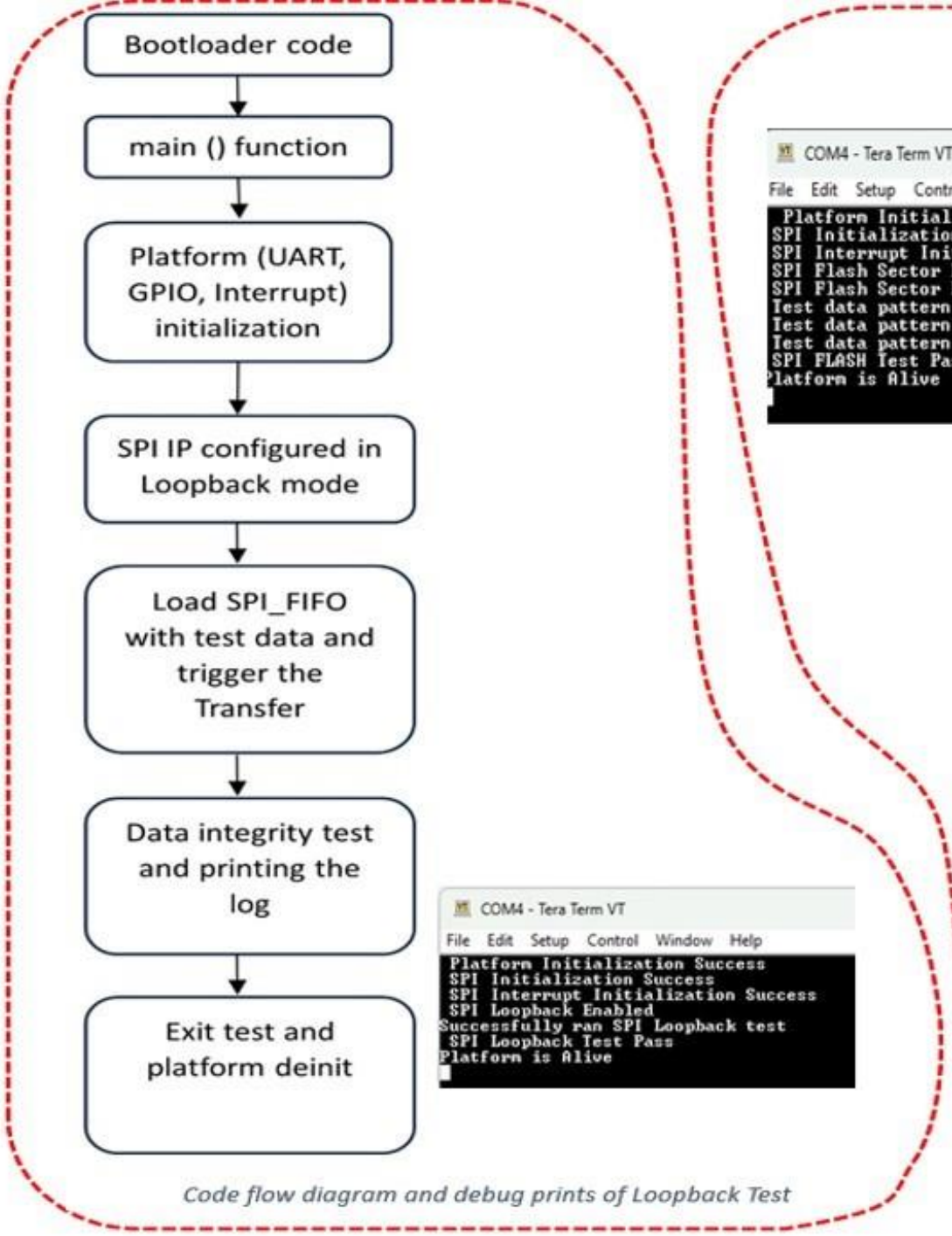
LIVE BOARD



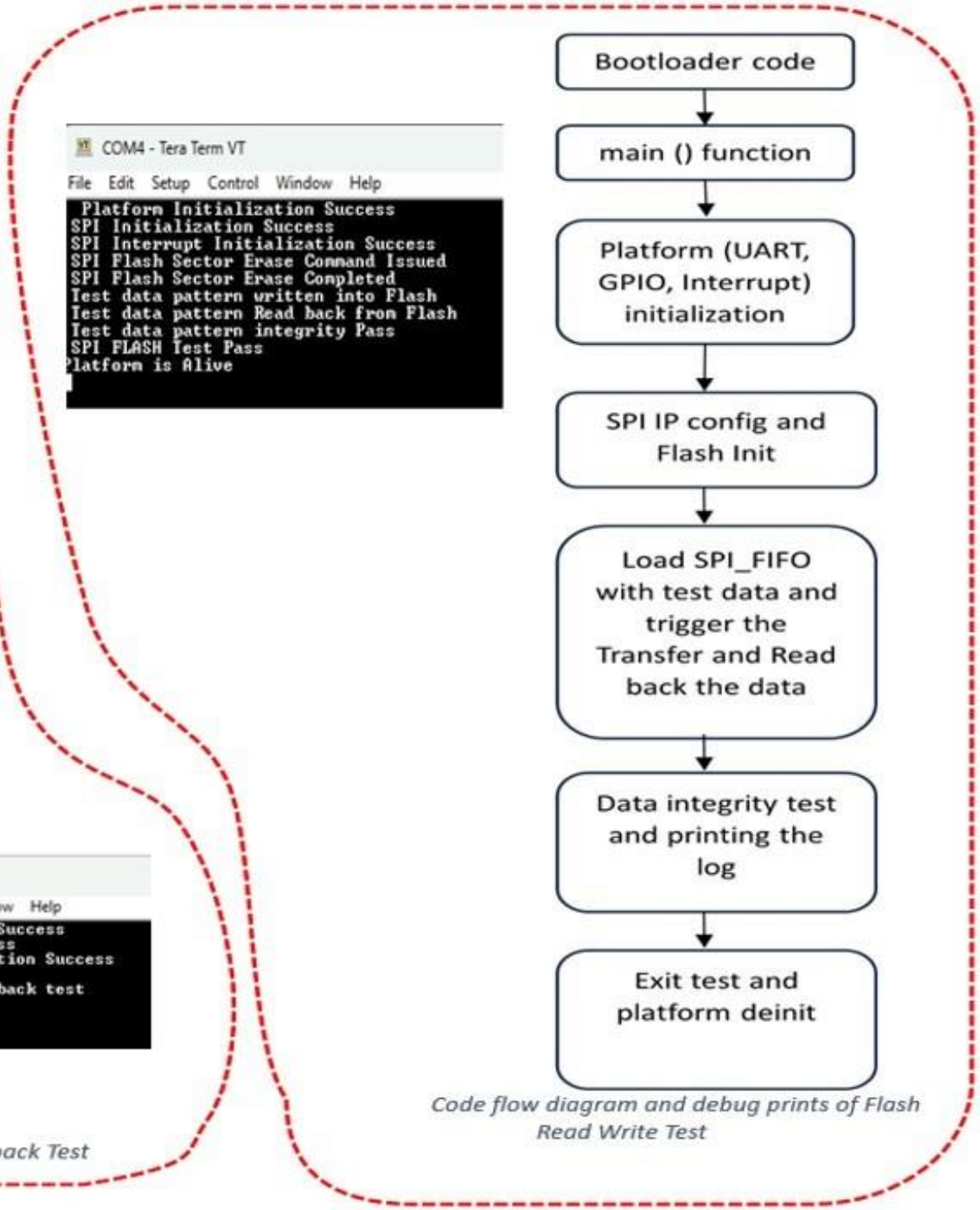
DEMO BOARD



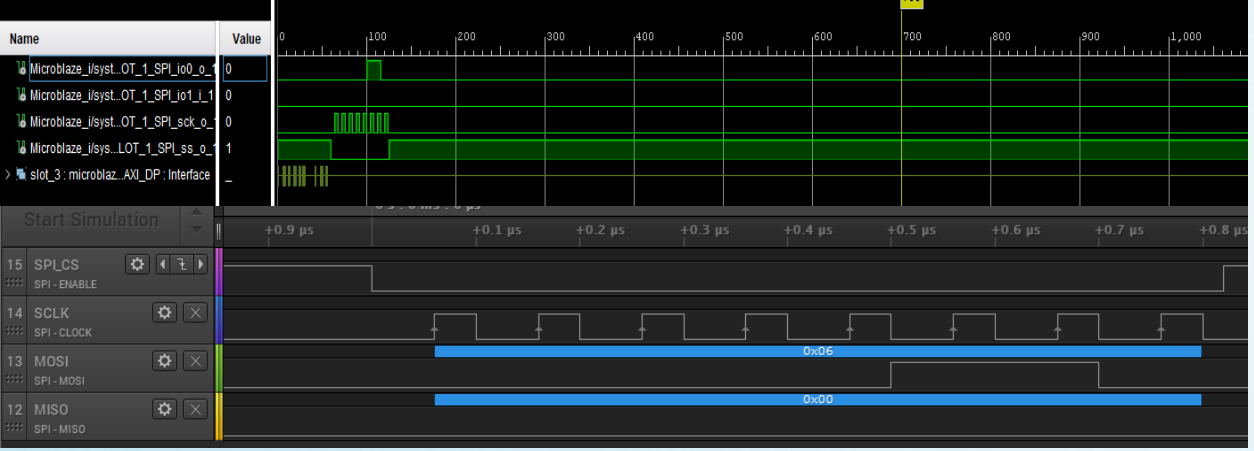
CODEFLOW CHART

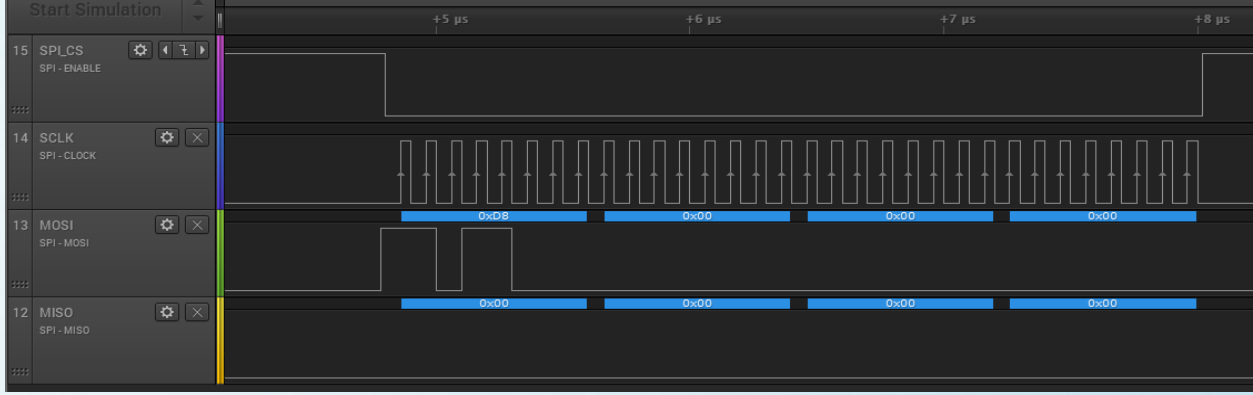


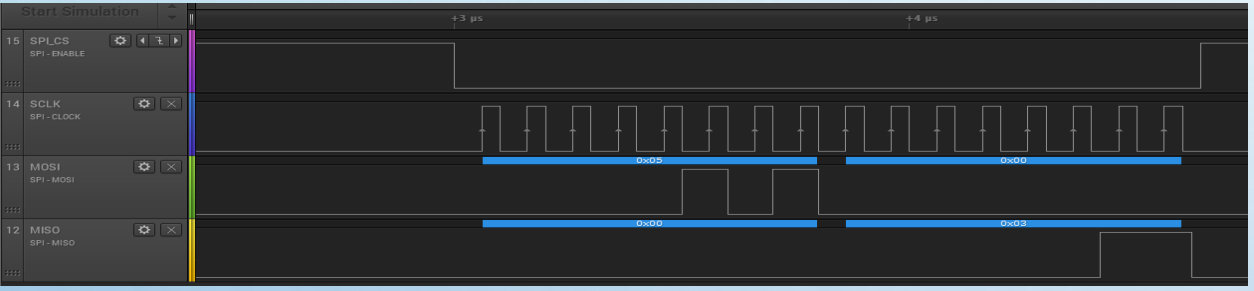
Code flow diagram and debug prints of Loopback Test

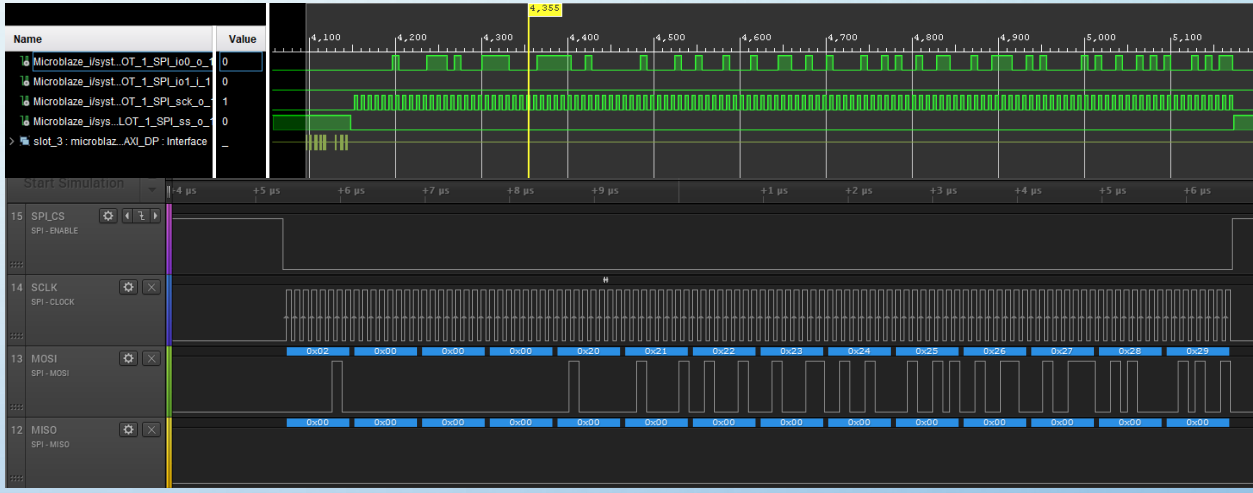


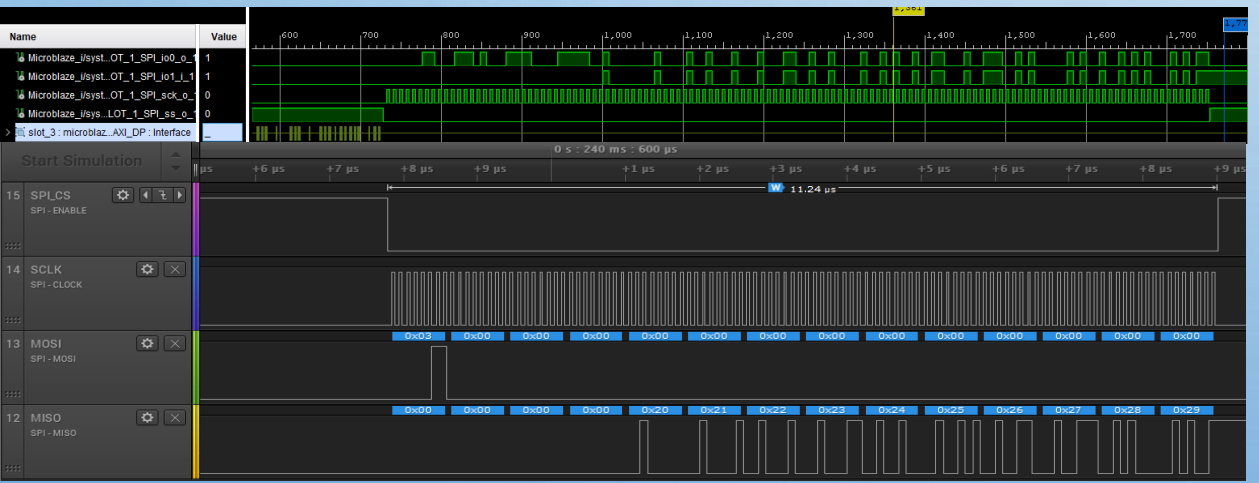
Code flow diagram and debug prints of Flash Read Write Test











Time [s]	Protocol	Decoded Protocol Result
6E-08	SPI	MOSI 0x06; MISO 0x00
2.49E-05	SPI	MOSI 0xD8; MISO: 0x00
2.57E-05	SPI	MOSI: 0x00; MISO: 0x00
2.65E-05	SPI	MOSI: 0x00; MISO: 0x00
2.73E-05	SPI	MOSI: 0x00; MISO: 0x00
5.31E-05	SPI	MOSI: 0x05; MISO: 0x00
5.39E-05	SPI	MOSI: 0x00; MISO: 0x03
0.240207	SPI	MOSI: 0x05; MISO: 0x00
0.240207	SPI	MOSI: 0x00; MISO: 0x00
0.240222	SPI	MOSI: 0x06; MISO: 0x00
0.240535	SPI	MOSI: 0x02; MISO: 0x00
0.240536	SPI	MOSI: 0x00; MISO: 0x00
0.240537	SPI	MOSI: 0x00; MISO: 0x00
0.240538	SPI	MOSI: 0x00; MISO: 0x00
0.240539	SPI	MOSI: 0x20; MISO: 0x00
0.240539	SPI	MOSI: 0x21; MISO: 0x00
0.24054	SPI	MOSI: 0x22; MISO: 0x00
0.240541	SPI	MOSI: 0x23; MISO: 0x00
0.240542	SPI	MOSI: 0x24; MISO: 0x00

0.240543	SPI	MOSI: 0x25; MISO: 0x00
0.240543	SPI	MOSI: 0x26; MISO: 0x00
0.240544	SPI	MOSI: 0x27; MISO: 0x00
0.240545	SPI	MOSI: 0x28; MISO: 0x00
0.240546	SPI	MOSI: 0x29; MISO: 0x00
0.240598	SPI	MOSI: 0x03; MISO: 0x00
0.240599	SPI	MOSI: 0x00; MISO: 0x00
0.240599	SPI	MOSI: 0x00; MISO: 0x00
0.2406	SPI	MOSI: 0x00; MISO: 0x00
0.240601	SPI	MOSI: 0x00; MISO: 0x20
0.240602	SPI	MOSI: 0x00; MISO: 0x21
0.240603	SPI	MOSI: 0x00; MISO: 0x22
0.240603	SPI	MOSI: 0x00; MISO: 0x23
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0.240606	SPI	MOSI: 0x00; MISO: 0x26
0.240607	SPI	MOSI: 0x00; MISO: 0x27
0.240607	SPI	MOSI: 0x00; MISO: 0x28
0.240608	SPI	MOSI: 0x00; MISO: 0x29

CONCLUSION:

- THIS PROJECT SUCCESSFULLY IMPLEMENTED A SPI IP IN FPGA PLATFORM AND DEVELOPED STANDALONE NON-OS C BASED TESTCASE TO TEST THE INTERFACE WITH THE SPI FLASH.
- THIS QUALIFIES THE IP IS SUITABLE FOR THE TARGETED APPLICATION OF CONTROLLING AN INDUSTRIAL GRADE ETHERCAT PHY CHIP VIA THIS SPI MASTER IP.
- IN REAL TIME APPLICATION THIS SPI MASTER IS GOING TO CONTROL A HIGH SPEED ETHERCAT BUS VIA SPI SLAVE INTERFACE PROVIDED TO IT.
- AS PART OF THIS PROJECT, TESTED THE CODE DEVELOPED AND PRESENTED THE RESULT IN DIFFERENT SECTIONS.
- FOR DEMO AND RESULTS PRESENTATION, A DIFFERENT DEVELOPMENT BOARDS (BASED ON XC7A100T) ARE USED DUE TO RESOURCE CONSTRAINTS.