

**Dissertation / Project / Project Work Title:  
Virtual prototyping and Emulation of conceptual  
IP**

**Course No. ESZG628T**

**Course Title: Dissertation / Project / Project Work**

**Dissertation / Project /Project Work Done by:**

**Student Name: Senthil Kumar M**

**BITS ID: 2022HT01062**

**Degree Program: M.Tech in Embedded Systems**

**Research Area: Hardware and Software Co-Design**

**Dissertation / Project Work carried out at:**

**Analog Devices India Pvt Ltd, Bangalore**



**BIRLA INSTITUTE OF TECHNOLOGY & SCIENCE,  
PILANI  
VIDYA VIHAR, PILANI, RAJASTHAN -  
333031.**

**January 2024**

## Contents

1. Broad Area of Work	3
2. Background	3
3. Objectives	3
4. Scope of Work	4
5. Plan of Work	4
6. Literature References	5
7. Particulars of the Supervisor and Examiner	6
8. Remarks of the Supervisor	6

## 1. Broad Area of Work

This research project explores the implementation of the Fast Fourier Transform (FFT) algorithm on both the SystemC modeling platform and Field-Programmable Gate Arrays (FPGAs). The study delves into key aspects of the design process, comparing and contrasting the characteristics of SystemC, a high-level system modeling language, with the intricacies of FPGA hardware implementation.

The abstraction level of SystemC provides a conducive environment for rapid prototyping and iterative development. It allows for the high-level modeling of complex systems and algorithms, fostering flexibility and ease of design modifications. In contrast, FPGA implementation demands a low-level hardware description using Hardware Description Languages (HDLs), necessitating a more structured and rigorous development process.

Simulation and debugging play crucial roles in the design cycle. SystemC facilitates efficient simulation and debugging at a high level, offering user-friendly tools for analysis. On the other hand, FPGA debugging involves more intricate processes, including simulation before synthesis and the utilization of specialized hardware debugging tools.

Performance analysis is approached differently in each domain. SystemC allows for the estimation of timing and throughput at a system level, abstracting away detailed hardware characteristics. In FPGA design, precise performance metrics, including timing, throughput, and resource utilization, are critical considerations, with tools providing detailed reports on hardware resources.

The implementation of parallelism and pipelining is a notable distinction. While SystemC allows for the modeling of these concepts, FPGA inherently supports parallelism, and explicit implementation of pipelining is crucial for optimizing design efficiency.

Timing constraints and real-time analysis are fundamental aspects of both SystemC and FPGA design, but their treatment differs. SystemC abstracts timing constraints during simulation, while FPGA tools rigorously analyze and report timing violations, necessitating adjustments for compliance. Real-time requirements are a focal point for FPGA designs, requiring adherence to stringent timing constraints.

Power analysis, another critical consideration, is approached differently in each context. SystemC provides high-level estimates based on simulation activities, while FPGA tools

offer detailed insights into power consumption, including dynamic and static power.

## **2. Background**

Digital signal processing plays a crucial role in various applications, including communication systems, audio processing, and image processing. The FFT algorithm is fundamental for efficiently computing the discrete Fourier transform, and its implementation can benefit from both high-level system modeling (SystemC) and dedicated hardware (FPGA). Understanding the trade-offs and characteristics of each approach is essential for optimizing performance in signal processing applications.

## **3. Objectives**

The objectives of my project are as follows:

- To implement the FFT algorithm using SystemC for high-level system modeling.
- To implement the FFT algorithm on FPGA, emphasizing low-level hardware description and optimization.
- To compare and contrast the characteristics, advantages, and limitations of the SystemC and FPGA implementations.
- To assess factors such as abstraction level, simulation capabilities, performance analysis, and real-time constraints in both approaches.

## **4. Scope of Work**

The scope includes developing detailed SystemC models for the FFT algorithm and translating these models into FPGA hardware using Hardware Description Languages (HDLs). The study encompasses simulation, debugging, and performance analysis in both environments. The research also explores the impact of parallelism, pipelining, timing constraints, and real-time requirements. Power consumption analysis is conducted for

both SystemC simulation and FPGA hardware implementation

## 5. Plan of Work

Phases	Start Date-End Date	Work to be done
Dissertation Outline	13 Jan 2019 – 21 Jan 2019	Literature Review and prepare Dissertation Outline
Design & Development	22 Jan 2019 – 15 Feb 2019	Design & Development Activity
Testing	16 Feb 2019 – 13 Mar 2019	Software Testing, User Evaluation & Conclusion
Dissertation Review	14 Mar 2019-25 Mar 2019	Submit Dissertation to Supervisor & Additional Examiner for review and feedback
Submission	26 Mar 2019-30 Mar 2019	Final Review and submission of Dissertation

## 6. Literature References

[1] Khushboo Pichhode, Mukesh D. Patil, Divya Shah, Chaurasiya Rohit B. "FPGA Implementation of Efficient Vedic Multiplier", *International Conference on Information Processing*, December 2015.

- This paper explores the development of an efficient signed multiplier using Vedic mathematics principles and carry select adder (CSeA) architecture. The authors address the need for high-speed multiplication in various computing applications, emphasizing the significance of multipliers in digital signal processing and related fields.
- The introduction provides context by highlighting the importance of multipliers in modern computing applications and the ongoing research efforts to enhance their speed and efficiency. It mentions the challenges of power dissipation and delays associated with conventional multipliers, setting the stage for exploring alternative design approaches.
- The authors introduce Vedic mathematics as an ancient Indian mathematical system that offers efficient techniques for multiplication and other arithmetic operations. They discuss the historical background of Vedic mathematics and its relevance to modern computing, citing its application in digital signal processing and image processing tasks.
- The literature review section discusses prior research efforts in multiplier design, including the Booth multiplier and other algorithms proposed for high-speed multiplication. It also references existing studies on Vedic multiplication techniques, both for unsigned and signed binary numbers. The limitations of previous methods, such as high delay in multiplier blocks, are highlighted as motivation for the proposed work.

[2] Jung Y, Yoon H and Kim J, "New Efficient FFT Algorithm and Pipeline Implementation Results for OFDM/DMT Applications", *IEEE Transactions on Consumer Electronics*, vol. 49, no. 1, pp.14-20, February 2003.

- This paper presents a novel Fast Fourier Transform (FFT) algorithm optimized for Orthogonal Frequency Division Multiplexing (OFDM) and Discrete Multi-Tone (DMT) applications. It discusses the proposed algorithm's pipeline implementation results and compares them with conventional approaches, focusing on hardware efficiency and processing rates.
- The MDC pipelined FFT processor with the proposed algorithm is analyzed in

detail. The processor consists of radix-4 and radix-2 butterfly units, delay commutators, and twiddle factor multipliers. Logic synthesis results demonstrate a significant reduction in gate count compared to conventional radix-4 algorithms, indicating improved hardware efficiency and area utilization.

- This paper concludes by highlighting the advantages of the proposed FFT algorithm for OFDM/DMT applications. The algorithm's ability to achieve higher processing rates and reduce hardware complexity makes it well-suited for systems like WLAN, DAB/DVB, and ADSL/VDSL. The comparison with conventional algorithms underscores the efficiency and effectiveness of the proposed approach in terms of logic gate count and processing speed.

[3] Lee Hand In-Cheol P, "Balanced Binary-Tree Decomposition for Area-Efficient Pipelined FFT Processing", *IEEE Transactions on Circuits and Systems—I: Regular Papers*, vol.54, no. 4, pp.889-900, April 2007

- This paper presents an area-efficient algorithm for pipelined processing of the Fast Fourier Transform (FFT) and discusses various implementation techniques aimed at reducing hardware complexity and area requirements. The paper addresses the growing demand for FFT processing in communication systems, especially in applications like digital video broadcasting-terrestrial (DVB-T) and orthogonal frequency division multiplexing (OFDM) systems.
- It discusses the Cooley-Tukey (CT) algorithm, a fundamental approach for FFT computation, and its variants including radix-2, radix-4, and mixed-radix algorithms. It provides insights into various FFT algorithms and their signal flow graphs, highlighting their hardware complexity and efficiency
- It introduces a balanced binary-tree decomposition algorithm aimed at minimizing the total size of twiddle factor tables. It presents a binary tree representation to illustrate the decomposition procedure and discusses the concept of balanced decomposition to reduce hardware complexity.

[4] Arunkumar P. Chavan, Rahul Verma, Nishanth S. Bhat "High Speed 32-bit Vedic Multiplier for DSP Applications", *International Journal of Computer Applications*, Vol.135- No.7, February 2016.

- This paper explores the design and implementation of high-speed Vedic multipliers for efficient digital signal processing (DSP) applications. The abstract highlights the significance of reducing mathematical operations' execution time and power consumption in digital signal processing, with a focus on

multiplication as a fundamental arithmetic operation. The authors propose two high-speed 32-bit Vedic multipliers designed based on the Urdhva-Triyakbhayam sutra, achieving significant reductions in speed when compared to conventional multipliers. The design is implemented using Verilog HDL and synthesized using Cadence tools.

- It summarizes the alternate designs of multiplier cells and their implementation using Verilog HDL. It underscores the advantages of the proposed multipliers in terms of processing time, making them suitable for high-speed digital signal processing applications.
- In summary, the paper provides valuable insights into the design and implementation of high-speed Vedic multipliers, showcasing their efficiency and effectiveness in digital signal processing tasks. It contributes to the ongoing research in optimizing arithmetic operations for high-performance computing applications.

[5] Stephen. M and Roger. W, "Power Efficient, FPGA Implementations of Transform Algorithms for Radar-Based Digital Receiver Applications", *IEEE Transactions on Industrial Informatics*, vol. 9, no. 3, pp. 1591-1600, Aug. 2013.

- This paper highlights the critical need for power-efficient solutions in defense and security systems, emphasizing the challenges of meeting processing demands while staying within power constraints. They propose a methodology focused on exploiting data redundancy and dynamic performance adjustments to achieve power-efficient FPGA realizations with improved sampling rates, particularly for radar-based digital receivers.
- It emphasizes the attractiveness of FPGA-based solutions for industrial electronics, especially in image and data processing, and defense applications where processing demands exceed the capabilities of traditional multiprocessor systems. The authors stress the limitations of Application Specific Integrated Circuits (ASICs) due to high non-recurring engineering costs, making FPGAs a more cost-effective and adaptable solution.
- Key contributions of the paper include:
  - Analyzing power consumption and processing requirements for a commercial digital receiver solution for Radar applications.
  - Introducing techniques to efficiently exploit hardware resources based on the dynamic range of input data, resulting in increased operational



capacity and resource efficiency.

- Proposing a methodology that leverages index space separation and dynamic range configuration techniques to reduce power consumption and enhance functionality within power constraints, demonstrated for an industrial Radar receiver.

[6] Swartzlander. E.E, and Hani. H.M. Saleh, "FFT Implementation with Fused Floating-Point Operations", *IEEE Transactions on Computers*, vol. 61, no. 2, pp.284-288, February 2012.

- This paper presents an innovative approach to implementing Fast Fourier Transform (FFT) processors using fused floating-point operations. Authored by E.E. Swartzlander Jr. and H.H.M. Saleh, it introduces two fused floating-point operations, namely the Fused Floating-Point Two-Term Dot Product Unit (Fused DP) and the Fused Floating-Point Add-Subtract Unit (Fused AS), and applies them to FFT processors.
- The authors highlight the significance of floating-point arithmetic in providing a wide dynamic range and flexibility in FFT processors, particularly in collaboration with general-purpose processors using the IEEE-754 standard 32-bit floating-point format. The paper emphasizes the need for efficient implementation of butterfly units, which are crucial for FFT computation, with a focus on reducing circuit area and delay while maintaining accuracy.
- This paper presents a comprehensive exploration of fused floating-point arithmetic units and their application to FFT processors. The proposed fused operations offer tangible benefits in terms of area efficiency, latency reduction, and improved numerical accuracy, making them promising candidates for FFT implementation on FPGA and system-level designs. The study contributes valuable insights into optimizing FFT processors for signal processing applications.

## 7. Particulars of the Supervisor and Examiner

	Supervisor	Additional Examiner
Name	Rajiv Nadig	Tony O Brien
Qualification	M Tech in VLSI Design Tool and Technology	Bachelor of Engineering in Electronic Engineering
Designation	Director, Digital Signal Engineering	Staff Engineer, Product Applications
Employing Organization and Location	Analog Devices Inc, Wilmington, USA	Analog Devices Inc, Cock, Ireland
Phone No.(with STD Code)		+353 (87) 9697881
Email Address	rajiv.nadig@analog.com	tony-x.obrien@analog.com

## 8. Remarks of the Supervisor

This project offers a well-articulated and insightful exploration of the implementation of the Fast Fourier Transform (FFT) algorithm on both the SystemC modeling platform and Field-Programmable Gate Arrays (FPGAs). The student skillfully compares and contrasts the key aspects of the design process, shedding light on the characteristics of SystemC as a high-level system modeling language and the complexities associated with FPGA hardware implementation.

### Information about the Supervisor:

Mr. Rajiv Nadig holds a postgraduate degree in VLSI design tools and technology from IIT Delhi and is a seasoned expert in the field of ASIC design. With over 23 years of experience, he has demonstrated his proficiency in VLSI design, specializing in various products, particularly in Analog design

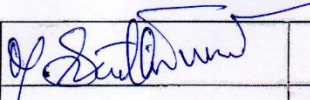

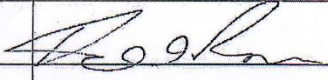
**BIRLA INSTITUTE OF TECHNOLOGY & SCIENCE, PILANI**  
**WORK INTEGRATED LEARNING PROGRAMMES (WILP) DIVISION**  
**SECOND SEMESTER OF ACADEMIC YEAR 2021-2022**

**ESZG628T : M.Tech in Embedded Systems OUTLINE**

<b>STUDENT ID No.</b>	2022HT01062
<b>NAME OF THE STUDENT</b>	M Senthil Kumar
<b>STUDENT'S EMAIL ADDRESS</b>	2022ht01062@wilp.bits-pilani.ac.in
<b>STUDENT'S EMPLOYING ORGANIZATION &amp; LOCATION</b>	Analog Devices, India Pvt Ltd, Bangalore
<b>SUPERVISOR'S NAME</b>	Rajiv Nadig
<b>SUPERVISOR'S EMPLOYING ORGANIZATION &amp; LOCATION</b>	Analog Devices Inc, Wilmington, USA
<b>SUPERVISOR'S EMAIL ADDRESS</b>	rajiv.nadig@analog.com
<b>ADDITIONAL EXAMINER'S NAME</b>	Tony O'Brien
<b>ADDITIONAL EXAMINER'S EMPLOYING ORGANIZATION &amp; LOCATION</b>	Analog Devices Inc, Cork, Ireland
<b>ADDITIONAL EXAMINER'S EMAIL ADDRESS</b>	tony-x.obrien@analog.com
<b>DISSERTATION / PROJECT / PROJECT WORK TITLE</b>	Virtual prototyping and Emulation of conceptual IP

Please prepare the outline as a separate document with the following sections along with the above identification information.

1. Cover Page with Student ID No., Name, Course Number, Course Title and Dissertation / Project / Project Work Title, Broad Academic Area of Work.
2. Background (Relevance of the Project to the current work environment in the employing organization)
3. Objectives
4. Scope of Work (To be done by the student independently)
5. Plan of Work (Work to be done during the semester)
6. Literature References
7. Particulars of the Supervisor and Additional Examiner
8. Remarks of the Supervisor

		
<b>Signature of Student</b>	<b>Signature of Supervisor</b>	<b>Signature of Additional Examiner</b>
<b>Name: M Senthil Kumar</b>	<b>Name: Rajiv Nadig</b>	<b>Name: Tony O'Brien</b>