Dissertation Title:

**Creating and deploying an open standard SPI on an FPGA, involving C based test case development for emulation**

**Course No.: MELZG628T**

**Course Title: Dissertation**

**Dissertation Done by: SELVA KUMAR S**

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**BITS ID: 2022HT80170**

**Degree Program: M.Tech. Microelectronics**

**Research Area: IP Emulation and Validation**

**Dissertation carried out at: Qualcomm Technologies Pvt. Ltd, Bengaluru**



**BIRLA INSTITUTE OF TECHNOLOGY & SCIENCE, PILANI**

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**(Jan 2024)**

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# Broad Area of Work

This dissertation is about the Emulation and validation of an SoC in a FPGA environment. The purpose of this dissertation is to qualify the RTL digital logic, before the Tape-out of the silicon. Because fixing a logical bug after the tape out or silicon arrival is going to be a costlier solution for the Semiconductor company. In this project, a simple SoC consist of open standard SPI IP which is provided in Xilinx IP integrator and a hardware ecosystem to develop Embedded C based test software is development.

# Background

Qualifying the RTL logic before Tape out will reduce the probability of logical bugs in the RTL code. To ensure this headache already there is a methodology called Design Verification. But due to speed limits and coverage limitations there are huge possibilities of bug escalation. Verification is also a simulation-based qualification which have its own constraints. In this scenario, to verify the Digital logic, it will be synthesized for FPGA platform where the gate logics are implemented as close as desired SoC. The beauty of FPGA is that the execution of testcases will be faster as like silicon when compared to DV platform. The only constraint is it needs some modifications in RTL to meet the timings in the FPGA. But these modifications will not affect the functionality of the RTL in the Silicon.

SPI is one of the customizable IP provided by the Xilinx IP Integrator tool. This SPI IP is referred as design under test (DUT) for this dissertation.

To qualify this IP in a SoC part it needs a complete ecosystem that is a simple processor to boot the code and simple memory to store the code and run time dynamic data and a system bus to interconnect all the subsystem. In this dissertation this eco-system is built as part of IP customization.

On top of this ecosystem the core intension of the dissertation that is the Testcase application is going to run. Testcases will be developed from test spec which is based on the actual specification of the Custom IP in the SoC

# Objectives

The objectives of my project are as follows:

* + - Creating a custom SPI IP from Xilinx IP Integrator
    - Creating an ecosystem to validate this IP
    - Understanding the hardware specification of IP
    - Writing a test spec from the Hardware Specification
    - Creating the testcases to qualify the IP
    - Collecting the Output waveforms from the Xilinx ILA

# Scope of Work

Scope of this dissertation is to design a simple SoC with a Custom IP (SPI) and required ecosystem to validate the IP and portrait the IP qualification KPIs. It also includes the C based testcases to measure the KPIs and test specifications and testcase development.

# Plan of Work

|  |  |  |
| --- | --- | --- |
| **Phases** | **Start Date-End Date** | **Work to be done** |
| Dissertation Outline | 13 Jan 2024 – 20 Jan 2024 | Literature Review and prepare Dissertation Outline |
| Design & Development | 22 Jan 2024 – 15 Feb 2024 | Design & Development Activity |
| Testing | 16 Feb 2024 – 13 Mar 2024 | Software Testing, User Evaluation & Conclusion |
| Dissertation Review | 14 Mar 2024 -25 Mar 2024 | Submit Dissertation to Supervisor & Additional Examiner for review and feedback |
| Submission | 26 Mar 2024-30 Mar 2024 | Final Review and submission of Dissertation |

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# Literature References

The state art is the base for any successful research project. In current project, the literature inclined towards the new domain of conversational information retrieval is considered. The following are referred journals from the preliminary literature review.

1. *Xilinx.com,* *AXI Quad SPI v3.2 LogiCORE IP Product Guide PG153 April 26, 2022.*
2. *Xilinx.com, MicroBlaze Processor Reference Guide.* *UG984 (v2021.2) October 27, 2021*
3. *Peter Marwedel, Embedded System Design, Springer 2003.*
4. *Quick Start Guide: MicroBlaze Soft Processor Presets.*
5. *7 Series FPGAs Data Sheet: Overview, DS180 (v2.6.1) September 8, 2020*
6. *Volnei A. Pedroni, Programming FPGAs: Getting Started with Verilog by Simon Monk, 2020.*
7. *Orhan Gazi, A.Çağrı Arlı ,State Machines using VHDL: FPGA Implementation of Serial Communication and Display Protocols, Springer 2021.*
8. *Kamal, Raj, Embedded Systems: Architecture, Programming & Design, Tata McGraw Hill, 2nd Ed., 2008*
9. *Wolf, Wayne, Computers as Components – Principles of Embedded Computing System Design, Second Edition, Morgan-Kaufmann, 2010.*

# Particulars of the Supervisor and Examiner

|  |  |  |
| --- | --- | --- |
|  | **Supervisor** | **Additional Examiner** |
| Name | Siva Selvamani | Siva Selvamani |
| Qualification | M. Tech in Embedded Systems and Technologies | M. Tech in Embedded Systems and Technologies |
| Designation | Staff Engineer - SVE | Staff Engineer - SVE |
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# Remarks of the Supervisor

This project is an innovative initiative within the organization. The outcome covered by this project seems to be interesting so that we are commissioning for our future projects in the organization. This idea is reducing the efforts spent and efficiently deliver the Organization’s deliverables. The main objective of this project is quality which is essential for the company. So as the supervisor I approved this project.

**BIRLA INSTITUTE OF TECHNOLOGY & SCIENCE, PILANI**

**WORK INTEGRATED LEARNING PROGRAMMES (WILP) DIVISION**

**SECOND SEMESTER OF ACADEMIC YEAR 2023-2024**

**ESZG628T : M.Tech in Embedded Systems OUTLINE**

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Please prepare the outline as a separate document with the following sections along with the above identification information.

1. Cover Page with Student ID No., Name, Course Number, Course Title and Dissertation / Project / Project Work Title, Broad Academic Area of Work.

2. Background (Relevance of the Project to the current work environment in the employing organization)

3. Objectives

4. Scope of Work (To be done by the student independently)

5. Plan of Work (Work to be done during the semester)

6. Literature References

7. Particulars of the Supervisor and Additional Examiner

8. Remarks of the Supervisor

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|  | ` |  |
| **Signature of Student** | **Signature of Supervisor** | **Signature of Additional Examiner** |
| **Name: Selvakumar** | **Name: Siva Selvamani** | **Name: Siva Selvamani** |