Report: Finite State Machine

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EE102-01 Lab 7

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Purpose:

The intent of this lab was to study the essentials of the finite state machine and design a finite state machine on a breadboard by using flip-flops and logic gates. Additionally, this work will grant a familiarity with the Moore and Mealy machines and how it operates and the implementation of this circuit on a breadboard.

Methodology:

In order to proceed with this lab work, one needed to design a finite state machine by their choice, and there are several different ways to implement a finite state machine according to the desired outcome machine can be either a Moore or a Mealy machine. The task has been chosen as creating a T-flip-flop using the necessary amount of D-flip-flops. Therefore, when implementing this design, there will be only one input required and a single output.

Design Specifications:

While implementing this design, one input and one output were used, and this design can be summarized as a Moore machine since the initial inputs are not affecting the output directly. Therefore, this idea refers to the previously mentioned finite state machine, which is a Moore machine. The input and output can be briefly explained as one being the data input of the T-flip-flop and the other being the output of the flip-flop. The state diagram and state table can be found in the following figures.

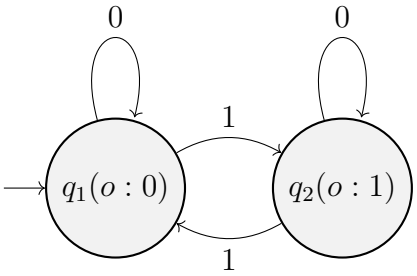


Figure 1: State diagram of the design.

The states and outputs have been listed and converted into a state table as following:

- State q1: OFF : Output=0
- State q2: ON : Output=1

Present State	Next State i=0	Next State i=1	Output
0	0	1	0
1	1	0	1

Figure 2: State table of the design.

Subsequently, after writing the state table of the following state diagram is and computing the Karnough map for D input of the D-flip-flop following circuit has been encountered:

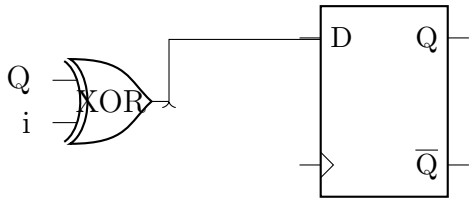
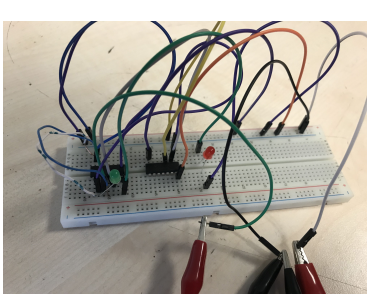


Figure 3: Circuit of the design.

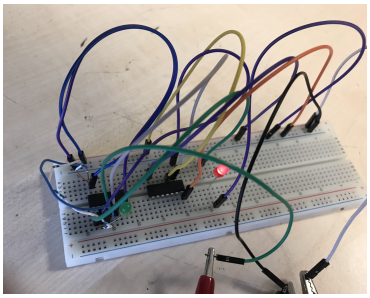
In order to implement the design on the breadboard several components were required and those components were chosen as 74HC74 which is a D-flip-flop and 74HC86 as two input XOR gate.

Results:

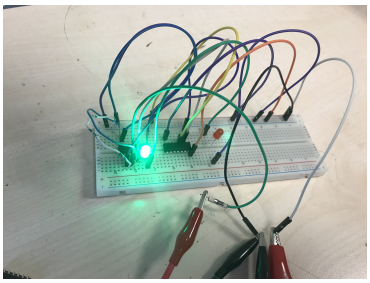
The suggested circuit has been implemented on the breadboard by using required gates and connections then states and outputs have been tested following images are the demonstration of the circuit on the breadboard. To, show the circuit working more clearly there are two LEDs connected in the circuit and red LED is the output of the finite state machine in this case output of T-flip-flop and, green LED is the data input of the D-flip-flop.



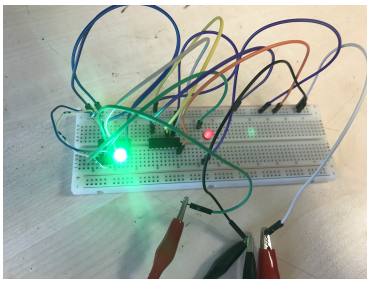
(a) At state 0 and i=0.



(b) At state 0 and i=1.



(c) At state 1 and i=0.



(d) At state 1 and i=1.

Figure 4: Working circuit on the breadboard.

Conclusion:

Designing a finite state machine has been learned while doing this lab and implementing it with ICs on breadboard. Throughout this lab work, several concepts have been reinforced, such as how a Moore machine works, how to design and implement such a circuit, and how to combine a combinational and a sequential circuit fundamentally.

References:

- LogicGates.pdf Accessed from Moodle.
- https://github.com/CankutBoraTuncer/Bilkent-EEE102-Labs