

Report: Circuit Theory Lab 4

Bilkent University Electrical and Electronics Department
EE202-03 Lab 4

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Purpose

In this lab, the objective is to design a circuit that can generate the voltage waveform depicted in Figure 1. The circuit design will be based on OPAMPS and RC circuits.

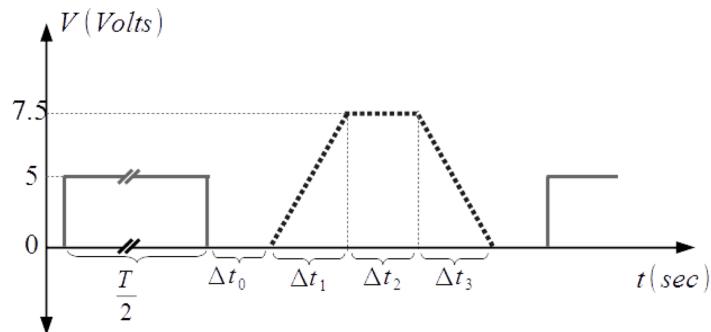


Figure 1: Desired waveform.

Software Implementation

Introduction

The designed circuit must satisfy the necessary conditions that can be seen in Figure 1. Additionally, in Figure 1, the input signal (represented by a solid gray line) consists of a square pulse. The output signal, depicted by dashed lines, displays one complete period.

- Here are the values,
 - $\Delta t_0 = 3ms$, $\Delta t_1 = 2ms$
 - $\Delta t_2 = 3ms$, $\Delta t_3 = 2ms$
 - Input peak voltage: 5V
 - Output peak voltage: 7.5V
 - Input frequency: $f \leq 50\text{Hz}$

Analysis

For the analysis section, the designed circuit combines several different ideas. The analysis part will investigate each of them separately.

Comparator OPAMP and RC Circuit Idea

For this circuit, the waveform needs to start after 3ms the falling edge of the input pulse. Therefore, one can achieve the delayed output by utilizing the comparator OPAMP and RC circuit. The equations and the drawing of the circuit will clarify the idea.

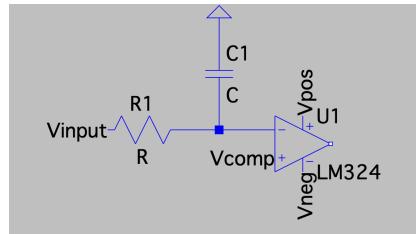


Figure 2: Comparator and RC circuit design.

A comparator OPAMP is a component that examines two input voltages and generates a high or low voltage depending on the comparison outcome. Its main function is to determine whether the voltage at the non-inverting input is greater than that at the inverting input and produce a corresponding output signal. When the voltage at the non-inverting input surpasses the voltage at the inverting input, the comparator output becomes high. Conversely, when the voltage at the inverting input is higher, the output goes to a low state.

When combined with an RC circuit, a delayed waveform can be created. The RC circuit gradually changes the voltage across it over time. The delayed waveform is achieved by connecting the output of the RC circuit to the inverting input of the comparator OPAMP.

Suppose Δt amount of delay needs to be created. Note that the RC circuit equation can be found by solving this differential equation $CdV/dt + V/R = V_{in}$ from this equation, one can find: $V(t) = V_f - (V_f - V_i)e^{-\frac{t}{RC}}$ and the following equations will use this general solution of RC circuit where $V_f = 0V$ and $V_i = 5V$. Then, one can use the following calculation to determine the resistor and capacitor value.

$$V_{comp} = 5e^{-\frac{t}{RC}} \Rightarrow t = RC \ln(5/V_{comp}) \Rightarrow RC = t/\ln(5/V_{comp})$$

Thus by using the desired delay values, one can get these equalities.

Note: The V_{comp} has been chosen as 1V (the reason why 1V is chosen will be explained in the Integrator OPAMP Idea part), and two delayed waveforms need to be created, one with a 3ms delay and another with an 8ms delay.

- For $\Delta t_0 = 3ms$

Calculations: $RC = t/\ln(5/V_{comp}) \Rightarrow RC = 3ms/\ln(5/1) = 1.86 * 10^{-6}$

Results: According to standard values in the lab $R_1 = 180k\Omega$ and $C_1 = 10nF$.

- For $\Delta t_0 + \Delta t_1 + \Delta t_2 = 8ms$

Calculations: $RC = t/\ln(5/V_{comp}) \Rightarrow RC = 8ms/\ln(5/1) = 4.97 * 10^{-6}$

Results: According to standard values in the lab $R_2 = 470\Omega$ and $C_2 = 11nF$.

Note that the values chosen considering the lab standard values difference are smaller than 5%.

Integrator OPAMP Idea

An integrator OPAMP is a circuit that performs the mathematical operation of integration on an input voltage signal. It accumulates the input voltage over time using a feedback capacitor, resulting in an output voltage that represents the integral of the input signal. By continuously summing the areas under the input signal's curve, the integrator OPAMP is able to integrate voltage signals with varying characteristics over time. This is achieved by charging or discharging the feedback capacitor in response to changes in the input voltage.

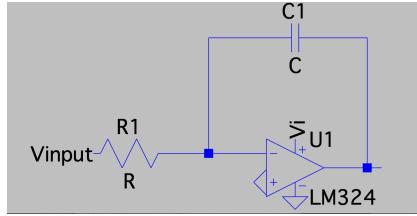


Figure 3: Integrator OPAMP circuit.

The integrator OPAMP will be used to generate the desired slopes in the output waveform. Since the input waveform is a square waveform the slope will be linear as desired.

Since, for the output signal, the slopes of the rising edge and falling edge are the same, calculations for determining the capacitor and resistor values can be done once. Let slope be m.

$$m = y/x \Rightarrow 7.5V/2ms \Rightarrow m = \frac{15}{4 * 10^{-3}} = 3750$$

Thus using the integrator OPAMP equality,

$$V_{out} = -\frac{1}{RC} \int_0^t V_{in} dt \xrightarrow{d/dx} \frac{dV_{out}}{dt} = \frac{V_{in}}{RC} = -m = -3750$$

Knowing that V_{in} is a square wave with $V_{max} = 5V$ and $V_{min} = -5V$,

$$\frac{-5}{RC} = -3750 \Rightarrow RC = 1.3 * 10^{-3}$$

So by choosing $C = 2.2nF$, then $R = 680k\Omega$. To achieve saturation at 7.5V and 0V in the circuit, these values have been selected as the desired saturation voltages. Note that, OPAMP consists of multiple transistors that contain non-linear and non-ideal components, including threshold voltages. This results in the output voltage of the OPAMP being lower than the positive saturation voltage, even when the OPAMP is in the positive saturation region. This characteristic of OPAMP is particularly important in the context of this lab. Therefore, the plus saturation voltage is set at 9V because the OPAMP uses 1.5V from the plus saturation voltage. The voltages connected to the comparator are 6.5V due to the previously mentioned reason for OPAMP not being ideal.

Subtractor OPAMP Idea

This section of the circuit involves subtracting two signals, resulting in the emergence of a trapezoid-shaped waveform.

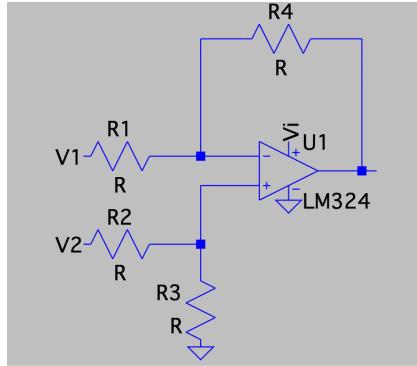


Figure 4: Subtractor OPAMP circuit.

Which yields the following equality,

$$V_{out} = -V_1 \left(\frac{R_4}{R_1} \right) + V_2 \left(\frac{R_3}{R_2 + R_3} \right) \left(\frac{R_1 + R_4}{R_1} \right)$$

Since the output voltage doesn't need to be amplified, the resistor values can be chosen as all equal and $R_1 = R_2 = R_3 = R_4 = 100k\Omega$. As long as the resistor values are the same, the value is not important theoretically, so easy to access $100k\Omega$ is chosen.

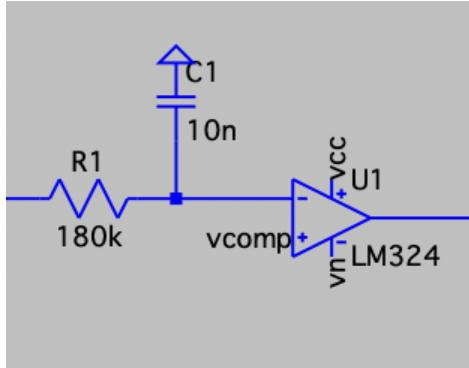
Simulation

As explained in the analysis section in the simulation part, the combination of the ideas and the complete circuit will be shown and simulated. The following figures include the implementation of the LTSpice tool from the previously explained analysis part.

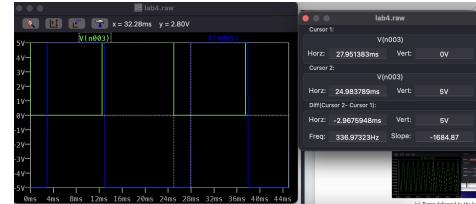
Note that the figures below may seem little, but since they are high quality, the reader may zoom in as much as they wish. The size of the figures is as they are because of aesthetic concerns. If plots are not as visible as required, please kindly zoom in.

Comparator OPAMP and RC Circuit Idea

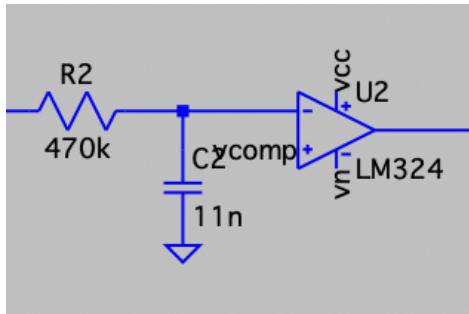
This part consists of the LTSpice simulation of the comparator OPAMP and RC circuit.



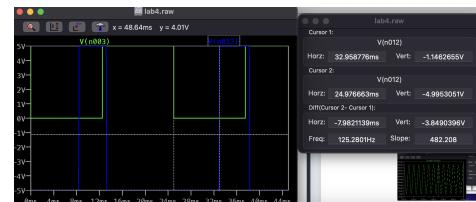
(a) Circuit with 3ms delay.



(b) Circuit with 3ms delay simulation.



(c) Circuit with 8ms delay.



(d) Circuit with 8ms delay simulation.

Figure 5: Comparator OPAMP and RC Circuit simulations.

From the simulations with the chosen values of components, a 3ms delay was generated as 2.97ms, which has a 1% error. 8ms delay was generated as 7.98ms which has a 0.25% error rate.

Integrator OPAMP Idea

This part consists of the integrator OPAMP and its simulation in the LTSpice tool.

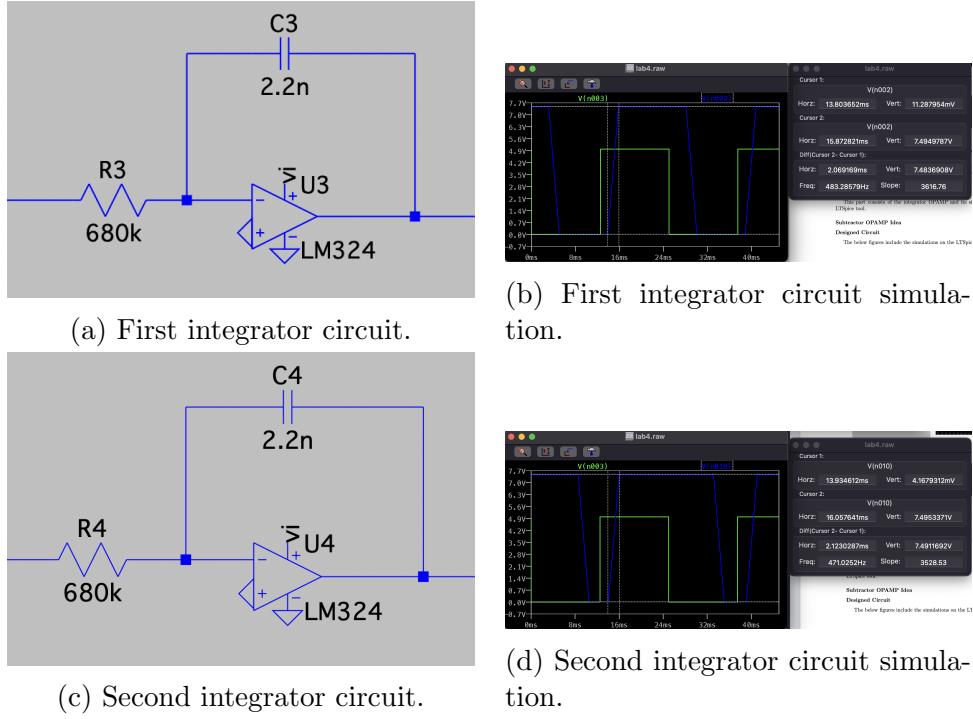


Figure 6: Integrator OPAMP simulations.

From the simulations with the chosen values of components, for the first integrator circuit, the slope of the waveform was supposed to be $\Delta t_1 = 2ms$, and it is measured 2.06ms which gives a 3% error. For second integrator circuit the slope is also needed to be 2ms and it is 2.12ms which yields 6% error.

Subtractor OPAMP Idea

This part consists of subtractor OPAMP and its simulation in LTSpice tool.

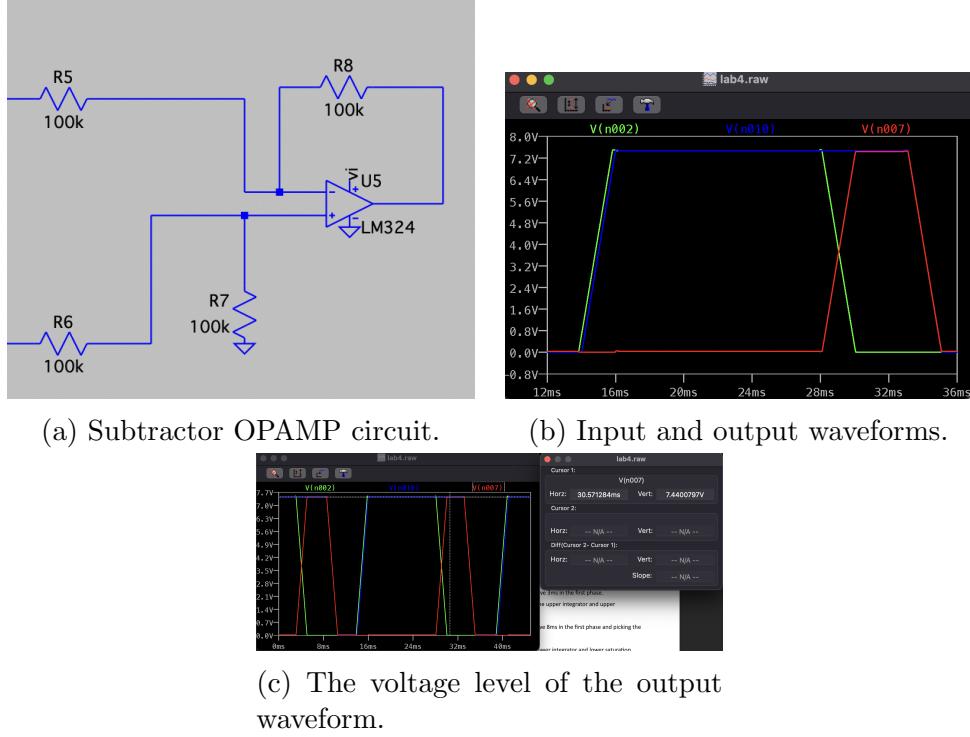


Figure 7: Subtractor OPAMP simulations.

From the simulation figures it is evident that subtractor works as intended and it satisfies the peak voltage by being 7.44V which has 0.8% error.

Designed Circuit

In this part simulation of the complete circuit will be done and the check of whether it satisfies the conditions and error rates will be shown.

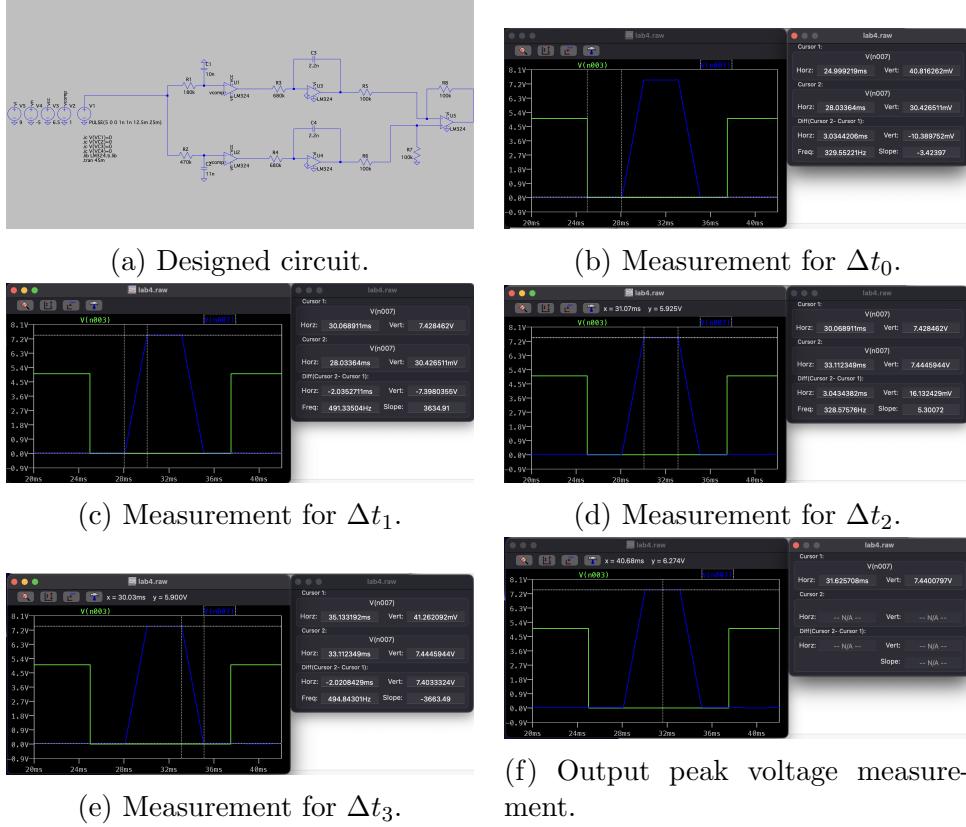


Figure 8: Simulations of the designed circuit.

In following table the errors and allowed error margin will be shown.

	Expected	Measured	Error
Δt_0	3ms	3.03ms	1%
Δt_1	2ms	2.04ms	2%
Δt_2	3ms	3.04ms	1.3%
Δt_3	2ms	2.02ms	1%
V_{max}	7.5V	7.44V	0.8%

Table 1: Table of errors and values.

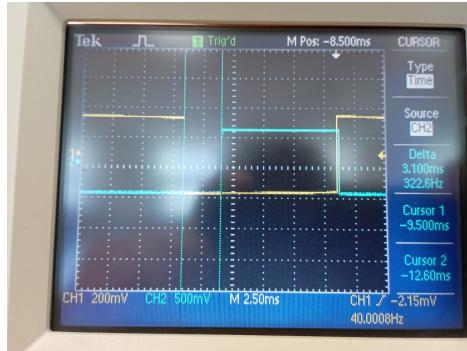
From the table it is evident that proposed circuit is satisfactory since in all areas error rates smaller than 10%.

Hardware Implementation

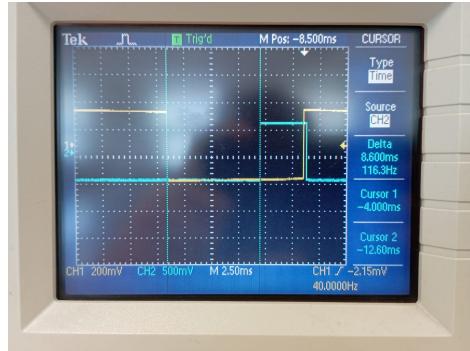
The hardware implementation consists of the above-described software results' application.

Intermediate Outputs

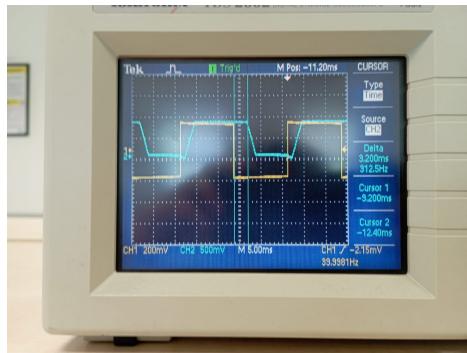
This part consists of the intermediate outputs from hardware implementation such as comparator OPAMP outputs and integrator OPAMP outputs.



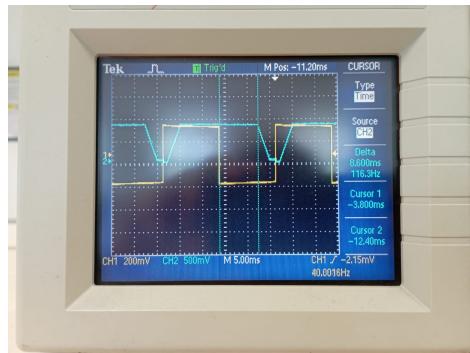
(a) First comparator OPAMP output 3ms delay.



(b) Second comparator OPAMP output 8ms delay.



(c) First integrator OPAMP output waveform.



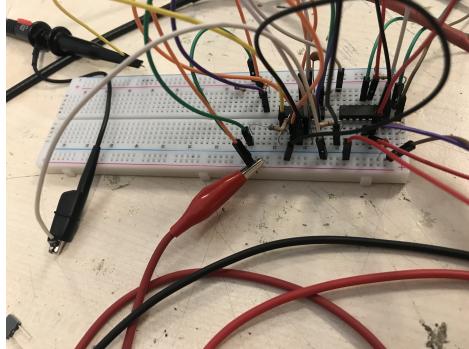
(d) Second integrator OPAMP output waveform.

Figure 9: Intermediate steps figures.

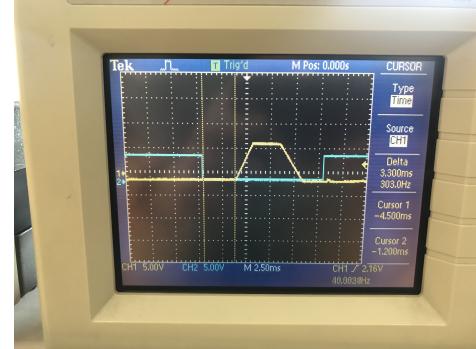
From figures it can be obtained that first comparator required to create 3ms delay and it produces 3.1ms which gives 3% error. The second comparator required to create 8ms delay and it creates 8.6ms delay which gives 7.5% error.

Designed Circuit

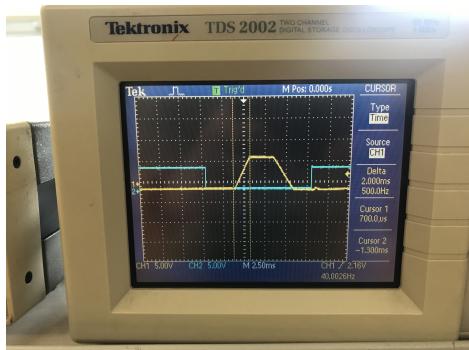
This part shows the final circuit and the generated output waveform.



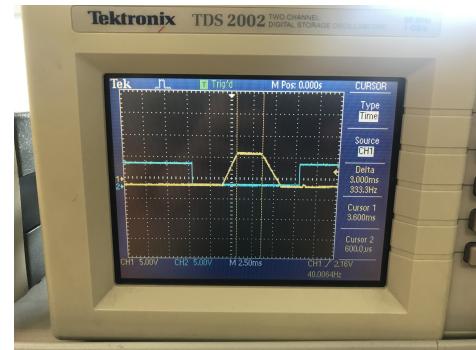
(a) Designed circuit.



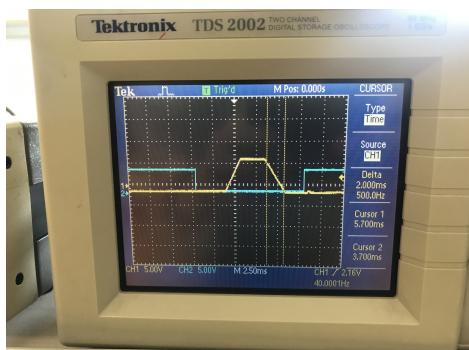
(b) Measurement for Δt_0 .



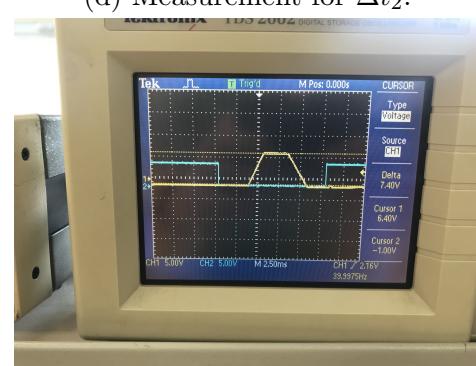
(c) Measurement for Δt_1 .



(d) Measurement for Δt_2 .



(e) Measurement for Δt_3 .



(f) Output peak voltage measurement.

Figure 10: Designed circuit.

In following table the errors and allowed error margin will be shown.

	Expected	Measured	Error
Δt_0	3ms	3.3ms	10%
Δt_1	2ms	2ms	0%
Δt_2	3ms	3ms	0%
Δt_3	2ms	2ms	0%
V_{max}	7.5V	6.4V	14.6%

Table 2: Table of errors and values for hardware implementation.

From the table it is evident that proposed circuit is satisfactory since in all areas error rates smaller than 20%.

Conclusion

The objective of the laboratory experiment was to generate a trapezoid waveform using a square input signal with an amplitude of 2.5 V, ranging between +5 V and 0 V. To achieve this goal, three types of OPAMP configurations were utilized: the comparator OPAMP, integrator OPAMP, and subtractor OPAMP. The functionality and principles of operation for each OPAMP were thoroughly examined. However, during the experiment, various errors were encountered in both the software and hardware components, potentially stemming from the components used, such as oscilloscope probes and breadboard. Additionally, discrepancies were observed, such as rounding up resistor values in software implementation or rounding values to standard values in hardware implementation. Minimizing these discrepancies could lead to reduced errors. Overall, this laboratory provided valuable insights into the application of these OPAMP types and their collective use to achieve the aforementioned objective.

References

- Analog Electronics, H. Koymen and A. Atalar, Accessed from Moodle.