Gowin DDR3 Memory Interface IP

User Guide

IPUG281-2.2E, 09/12/2023

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Revision History

Date	Version	Description
08/24/2018	1.0E	Initial version published.
03/12/2019	1.1E	Description of DDR3 1:4 clock ratio about continuous burst added.
07/12/2019	1.2E	● Address format modified. ● Read and write efficiency description added.
01/06/2020	1.3E	Static parameter options modified.
06/30/2021	1.4E	● memory_clk and pll_lock ports added. ● Design source code file updated.
11/25/2021	1.5E	● The timing descriptions of cmd_en and cmd_ready modified. ● The timing descriptions of wr_data_en and wr_data_rdy modified.
08/12/2022	1.6E	● The timing descriptions of user interface updated. ● The descriptions for continuous burst mode and non-continuous burst mode of the controllers added.
10/17/2022	1.7E	wr_data_wren modified to wr_data_en, clk modified to clk_out, and wr_data_ready modified to wr_data_rdy in the timing diagrams.
06/08/2023	2.0E	● The description of GW5AST-138 device added. ● pll_stop signal added. ● Chapter 8 Reference Design and Chapter 9 File Delivery removed.
08/18/2023	2.1E	● GW5A-25 device added. ● Burst_Number_Enable option removed. ● The descriptions of app_burst_number interface signals removed.
09/12/2023	2.2E	GW5A-25 devices support pll_stop.

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1 About This Guide

1.1 Purpose

The purpose of Gowin DDR3 Memory Interface IP User Guide is to help you quickly learn the features and usage of Gowin DDR3 Memory Interface IP by providing the descriptions of the functions, ports, timing, GUI, and reference design. The software screenshots in this manual are based on V 1.9.9 Beta-3. As the software is subject to change without notice, some information may not remain relevant and may need to be adjusted according to the software that is in use.

1.2 Related Documents

The latest user guides are available on the GOWINSEMI Website. You can find the related documents at www.gowinsemi.com:

- DS102, GW2A series of FPGA Products Data Sheet
- DS226, GW2AR series of FPGA Products Data Sheet
- DS1104, GW5AST series of FPGA Products Data Sheet
- DS1103, GW5A series of FPGA Products Data Sheet
- SUG100, Gowin Software User Guide

1.3 Terminology and Abbreviations

The terminology and abbreviations used in this manual are as shown in Table 1-1.

Table 1-1 Terminology and Abbreviations

Terminology and Abbreviations	Meaning
ECC	Error Correcting Code
FIFO	First Input First Output
GSR	Global System Reset
IP	Intellectual Property
LUT	Look-up Table
RAM	Random Access Memory

1.4 Support and Feedback

Gowin Semiconductor provides customers with comprehensive technical support. If you have any questions, comments, or suggestions, please feel free to contact us directly by the following ways.

Website: www.gowinsemi.com

E-mail: support@gowinsemi.com

2 Overview

Gowin DDR3 Memory Interface IP is a commonly used DDR3 memory interface IP that complies with the JESD79-3F standard protocol. The IP design includes DDR3 memory controller (MC) and the corresponding physical interface (PHY). Gowin DDR3 Memory Interface IP provides you with a general command interface which can connect with the memory chip to access and save data.

Table 2-1 Gowin DDR3 Memory Interface IP

Gowin DDR3 Memory Interface IP	
Logic Resource	Please refer to Table 3-1.
Delivered Doc.	
Design Files	Verilog (encrypted)
Reference Design	Verilog
TestBench	Verilog
Test and Design Flow	
Synthesis Software	GowinSynthesis
Application Software	Gowin Software (V1.9.9 Beta-3 and above)

Note!

For the devices supported, you can click here to get the information.

3 Features and Performance

3.1 Features

- Supports GW2A-18, GW2AR-18, GW2A-55, GW5A-25, and GW5AST-138 devices
- Interfaces to the industrial standard DDR3 SDRAM devices and modules that are compatible with the JESD79-3F specification
- Supports memory data path width of 8 bits, 16 bits, 24 bits, 32 bits, 40 bits, 48 bits, 56 bits, 64 bits, and 72 bits
- Supports the single row RDIMM, UDIMM, and SODIMM memory modules
- Supports x8 and x16 data width memory chips
- Programs 4, 8, or OTF burst lengths
- Supports 1:2 and 1:4 clock ratio for GW2A-18, GW2A-55, and GW2AR-18, and supports 1:4 clock ratio for GW5AST-138
- Supports ECC
- Configurable CL
- Configurable AL
- Configurable CWL
- Configurable t_{FAW}
- Configurable t_{RAS}
- Configurable t_{RCD}
- Configurable t_{RFC}
- Configurable t_{RRD}
- Configurable t_{RTP}
- Configurable t_{WTR}
- Supports dynamic on-chip ODT
- Supports automatic refreshing and user startup refreshing and the interval of automatic refreshing is configurable

3.2 Operating Frequency and Bandwidth Efficiency

The data rate of the DDR3 SDRAM that Gowin DDR3 Memory Interface supports is as follows:

- 533 Mbps supported in 1:2 clock ratio mode.
- 533 Mbps and 800 Mbps supported in 1:4 clock ratio mode.

The bandwidth efficiency of Gowin DDR3 Memory Interface IP is as follows:

- In 1:2 clock ratio mode with a burst length of 4, the bandwidth efficiency is 50%.
- In 1:2 clock ratio mode with a burst length of 8, the bandwidth efficiency is 90%.
- In 1:4 clock ratio mode, the bandwidth efficiency is 90%.

Gowin DDR3 Memory Interface IP employs the Verilog language, and it is applied to GW2A-18, GW2AR-18, GW2A-55, and GW5AST-138 devices. The resource utilization is as shown in Table 3-1. For the application verification on other Gowin devices, refer to later release information.

Table 3-1 Resource Utilization

DQ_WIDTH	LUTs	REGs	I/O	f_{MAX}	Device	Speed Grade
8(x8)	1061	1009	151	600 Mbps	GW2A-55/ GW2A-18	-6 -7 -8
16(x8)	1312	1365	231			
24(x8)	1557	1721	311			
32(x8)	1639	2077	391			
40(x8)	1845	2433	471			
48(x8)	2060	2789	551			
56(x8)	2271	3145	631			
64(x8)	2483	3501	711			
72(x8)	2694	3857	791			

Note!

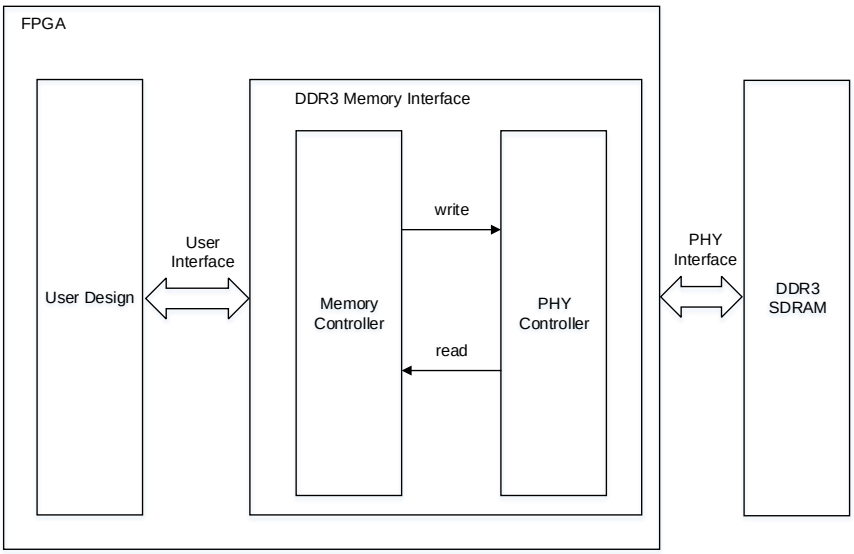
In Table 3-1, Gowin DDR3 Memory Interface was configured with a user address width of 29 bits, DRAM width of x8 and the clock ratio of 1:2; When the clock ratio is 1:4, the resource is about twice as much as the one in the table.

4 Functional Description

4.1 Structure

The structure of Gowin DDR3 Memory Interface IP is as shown in Figure 4-1. It includes Memory Controller and Physical Interface modules, etc. The User Design in the Figure 4-1 is the user design in the FPGA that needs to be connected to an external DDR3 SDRAM chip.

Figure 4-1 DDR3 Memory Interface IP Structure Diagram



4.2 Memory Controller

Memory Controller is located at MC layer, realizing protocol layer functions. Internal state machine is for BANK, ROW, COL, and refresh control. Memory Controller receives user-side read and write commands, stores the commands in FIFO logic internally, converts read and write commands into detectable interface timings on PHY side, and inputs to PHY side.

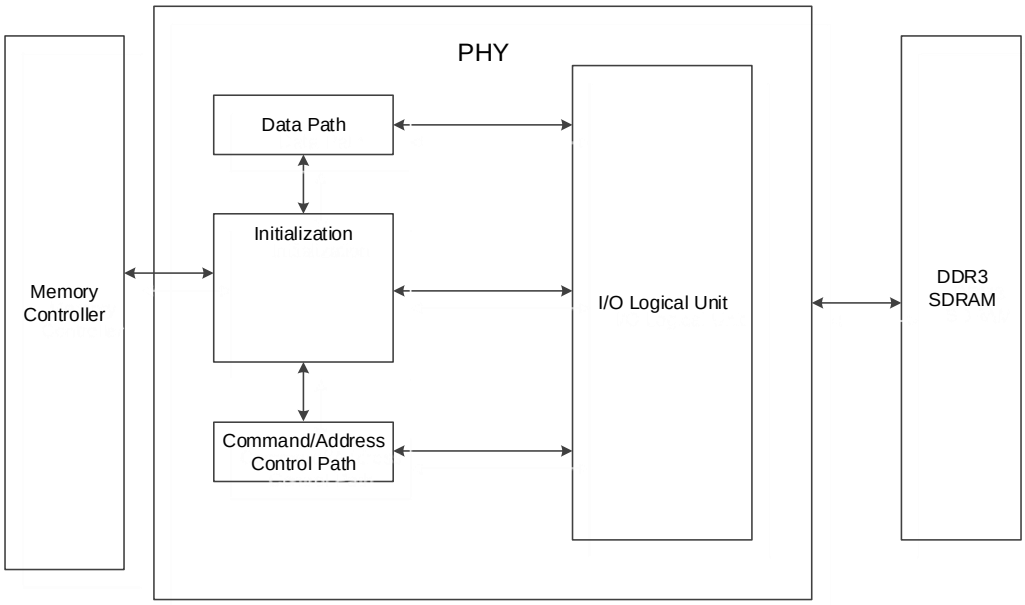
4.3 PHY

The PHY provides the physical definition and interface between MC and external DDR3 SDRAM, receives commands from the memory

controller on MC layer, and provides the DDR3 SDRAM chip with interface timing.

The structure of PHY includes four modules: initialization module, data path, command address control path, and I/O logic module, as shown in Figure 4-2.

Figure 4-2 DDR3 PHY Basic Structure Diagram



4.3.1 Initialization Unit

The initialization module is mainly used for initialization and read calibration after DDR3 SDRAM power-on. After initialization and read calibration are finished, the "init_calib_complete" signal will be high from low, indicating that the initialization has been completed.

Note!

Read/write operations are not allowed to be performed until the init_calib_complete signal is pulled up.

Power-on Initialization

According to the JESD79-3F protocol, there is a need to initialize the DDR3 SDRAM (chip or DIMM) after power-on. This includes the reset, clock enable, mode register configuration, and ZQ calibration.

4.3.2 Data Path Unit

Data path includes write data path and read data path.

4.3.3 Control Path Unit

The command/address control path is a single path that receives the command and address signal sent by the Memory Controller and cooperates with the data path to process the write and read data delay parameters and sends the commands to the I/O logic module.

4.3.4 I/O Logical Unit

The Logic I/O module is mainly used to convert the clock domain of

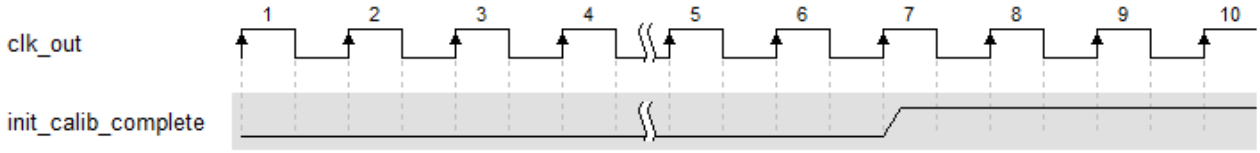
the data, command, and address signals received from the data path and command/address path.

4.4 User Interface

4.4.1 Initialization Interface

Init_calib_complete: The DDR3 SDRAM needs to be calibrated before write and read. Therefore, after power-on, PHY will initialize and calibrate the DDR3 SDRAM, and the init_calib_complete is pulled high after the initialization is completed, as shown in Figure 4-3.

Figure 4-3 Initialization Completion Signal Timing Diagram



4.4.2 Command and Address Interface

Command

You can write commands to IP via cmd and cmd_en, and the controller initiates read and write to the DDR3 chip according to the order of the write commands.

- Cmd is the command port;
- Cmd_en is the enable signal of the command, active-high.

See Table 4-1 for the meanings of cmd：

Table 4-1 Cmd

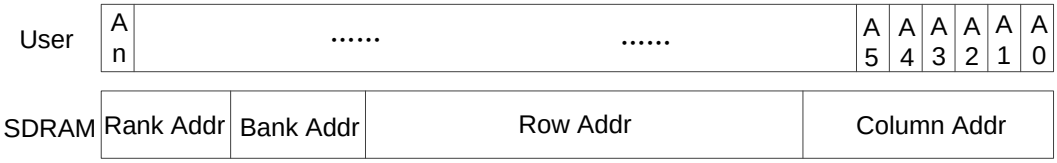
Command	cmd[2:0]
Read	3’b001
Write	3’b000

Address

Addr is the user-side address bus which is written to the controller together with cmd. Addr is valid when cmd_en is valid.

In the application, a mapping relationship exists between the address bus of user interfaces and Bank, Rank, Row, Column of the physical memory. In this design, the array is in Rank-Bank-Row-Column order, and the addressing scheme is as shown in Figure 4-4. You should note the order of the addresses provided in the application.

Figure 4-4 Addressing Scheme in Rank-Bank-Row-Column Order



Addr is the DDR address, i.e. addr directly reflects the DDR memory address. When DDR3 burst_mode is configured with BC4, one write/read needs to write/read 4 dq data to DDR, so one DDR write/read occupies 4 addresses. When DDR3 burst_mode is configured with BL8, one write/read needs to write/read 8 dq data to DDR, so one DDR write/read occupies 8 addresses. You should note the control of the addresses provided in the application.

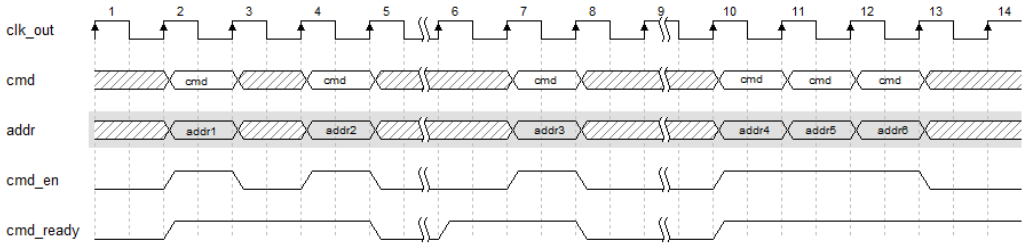
Address and Command Timing with 1:2 Clock Ratio

If clock ratio is 1:2 and cmd_ready is high, it indicates that the DDR controller can receive user commands.

When cmd_en and cmd_ready is 1, write cmd and addr to IP. addr1 and addr2 have no relationship and do not have to be neighboring addresses.

The timing of the command, address, and enable signals is as shown in Figure 4-5.

Figure 4-5 Command, Address, and Enable Signal Timing-A



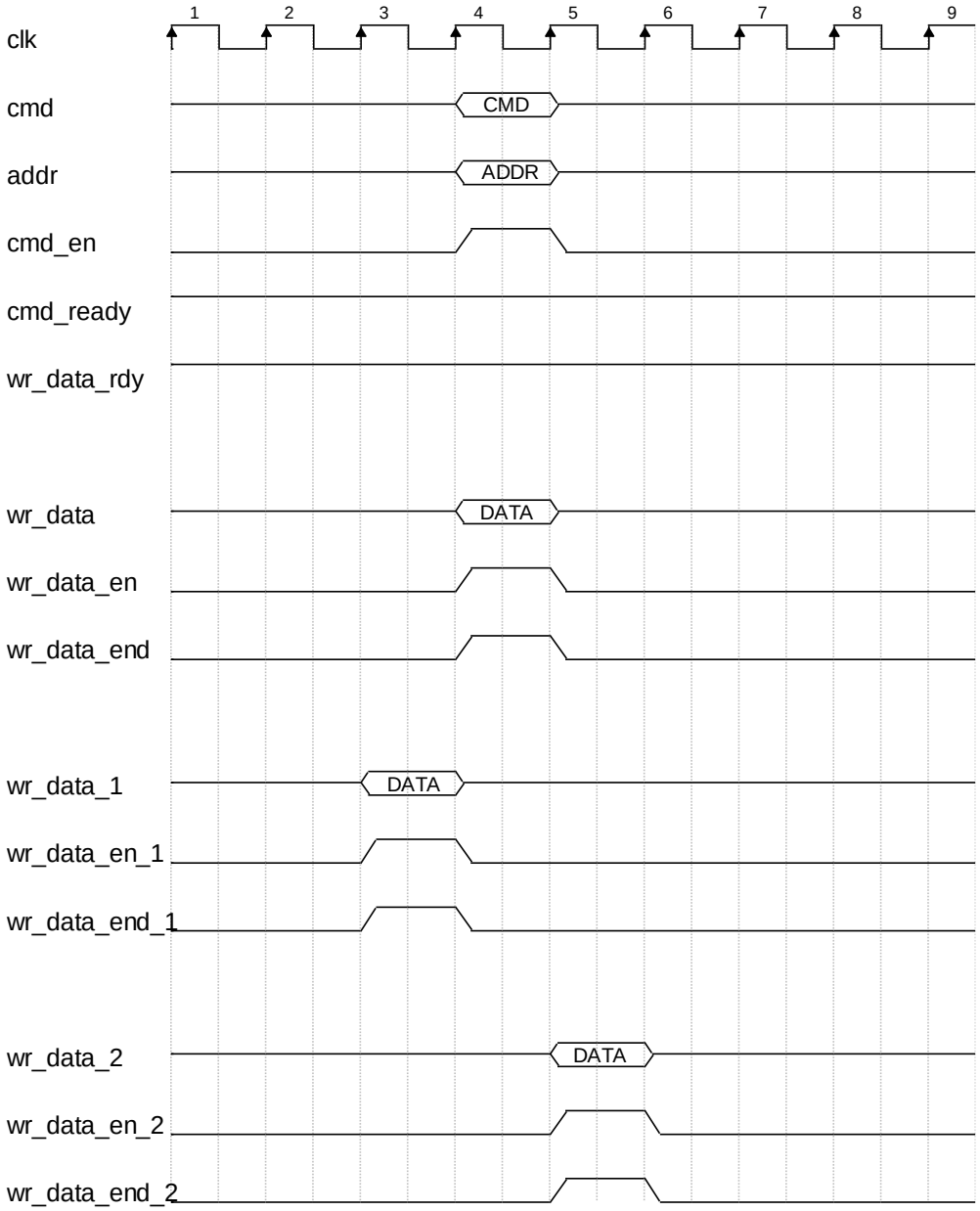
Address and Command Timing with 1:4 Clock Ratio

The address and command timing is the same as that in 1:2 clock ratio. See the timing as shown in Figure 4-5.

4.4.3 The Location Relationship Between Command and Write Data

The location relationship between command and write data is as shown in Figure 4-6.

Figure 4-6 The Location Relationship Between cmd and Data



4.4.4 Write Data Interface

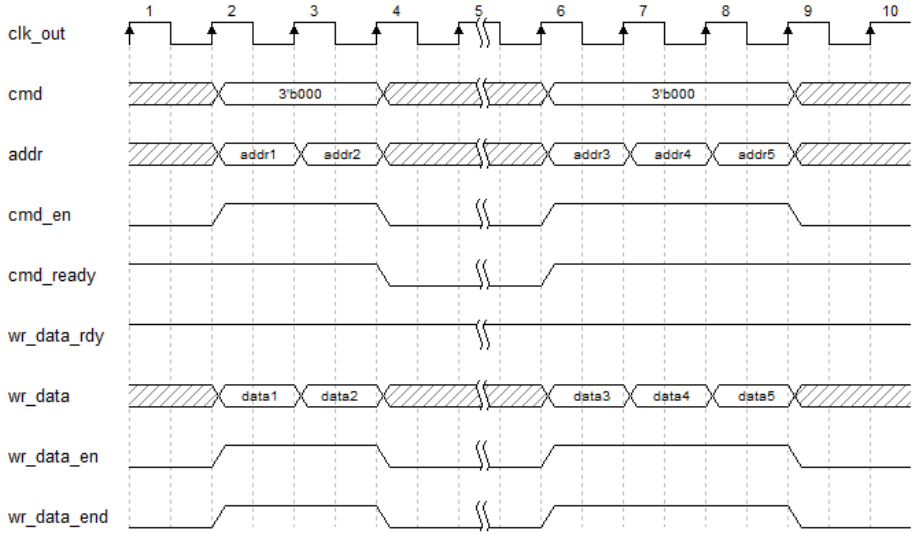
- wr_data: Data bus interface. You can write the data need to be stored in DDR through this interface.
- wr_data_en: Data write enable interface. wr_data is active-high.
- wr_data_end: It indicates the data on wr_data bus in current cycle is the last write data currently.
- wr_data_rdy: when wr_data_rdy is high, it indicates the controller can receive user data. You can write data in controller through wr_data, wr_data_en, and wr_data_end interfaces.

When the clock ratio is 1:2, the burst_mode is configured with BC4, and the bit width ratio of wr_data to dq data is 1:4. At this time, one wr_data can meet one burst write for DDR. wr_data_en and wr_data_end

have the same action, so you can write 1 to wr_data_en and wr_data_end at the same time when writing data.

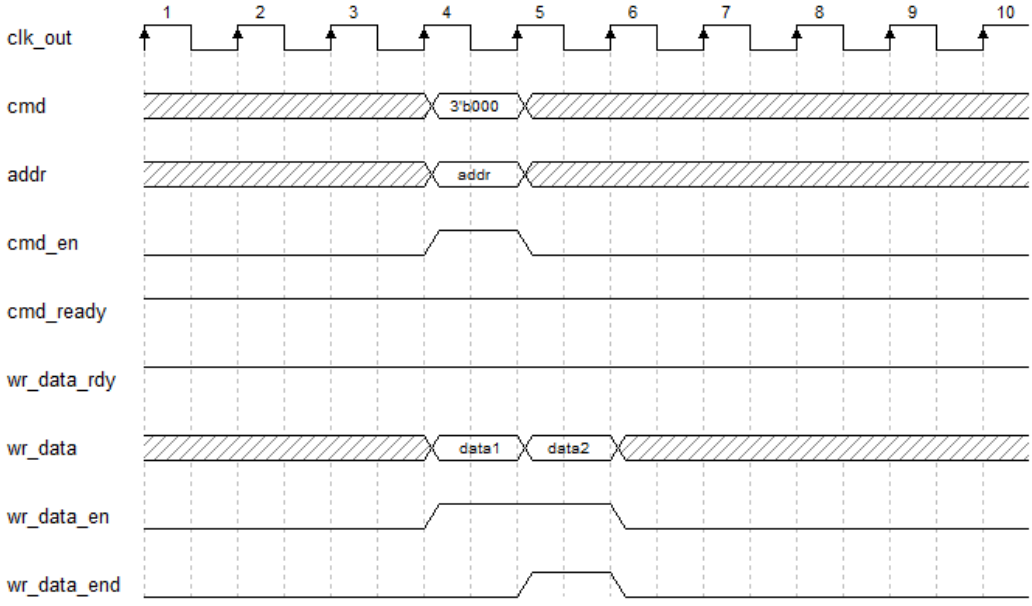
When the clock ratio is 1:4 and the burst_mode is configured with BL8, the situation is the same as the above example. See Figure 4-7 for the timing.

Figure 4-7 Write Data Timing with 1:2 Clock Ratio and Burst_Mode=BC4 or 1:4 Clock Ratio



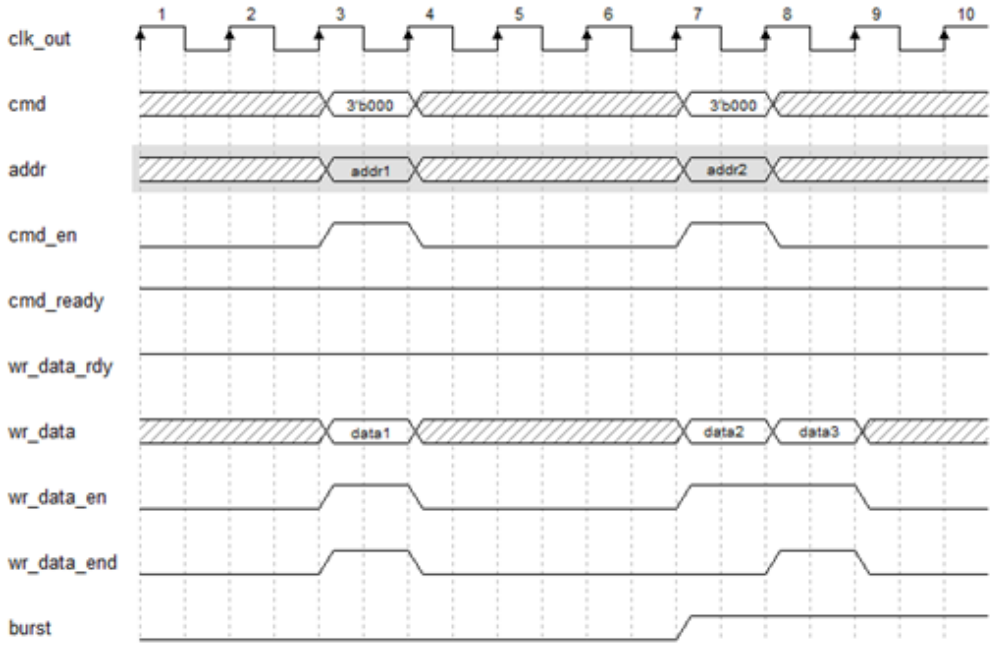
When the clock ratio is 1:2 and burst_mode is configured with BL8, the bit-width ratio of wr_data to dq data is 1:4. At this time, DDR needs two wr_data for one burst write. Then wr_data_en should last for two consecutive cycles, and the second cycle will write wr_data_end to 1. See Figure 4-8 for the timing.

Figure 4-8 Write Data Timing with 1:2 Clock Ratio and Burst Mode=BL8



Only when the clock ratio is 1:2, burst_mode is supported to be configured with OTF mode. In this mode, the port signal burst is 0 indicating the current DDR chip burst_mode is BC4; the port signal burst is 1 indicates the current DDR chip burst_mode is BL8. At this time, you should control the wr_data _en and wr_data_end signals according to the situation. See Figure 4-9 for the timing.

Figure 4-9 Write Data Timing with 1:2 Clock Ratio and Burst Mode=OTF



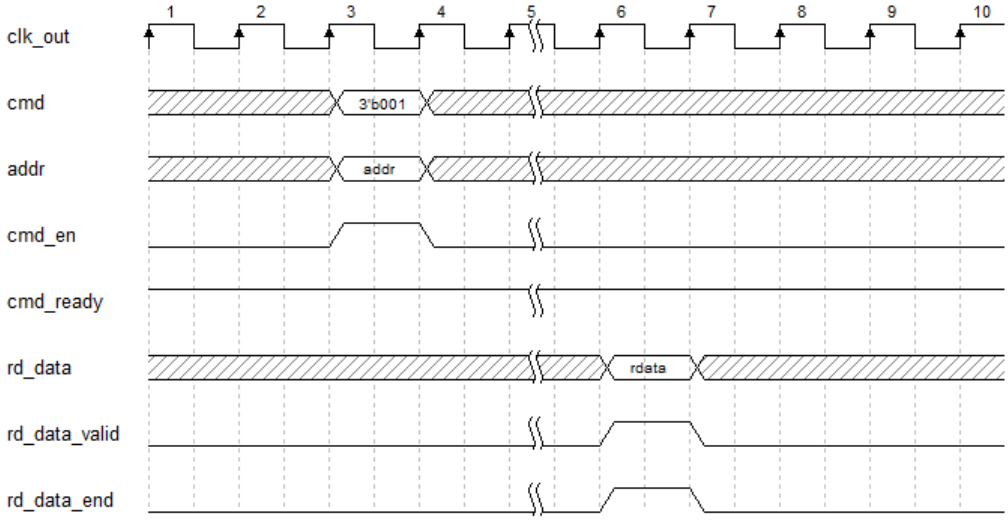
4.4.5 Read Data

You can read the data from the DDR3 SDRAM using the user interfaces, including rd_data, rd_data_valid, and rd_data_end.

- The rd_data is the returned read data port.
- The rd_data_valid port is the valid read data port. When it is high, it indicates the returned rd_data is valid at this time.
- The rd_data_end port indicates the last set of returned data in the current burst_mode, active-high.

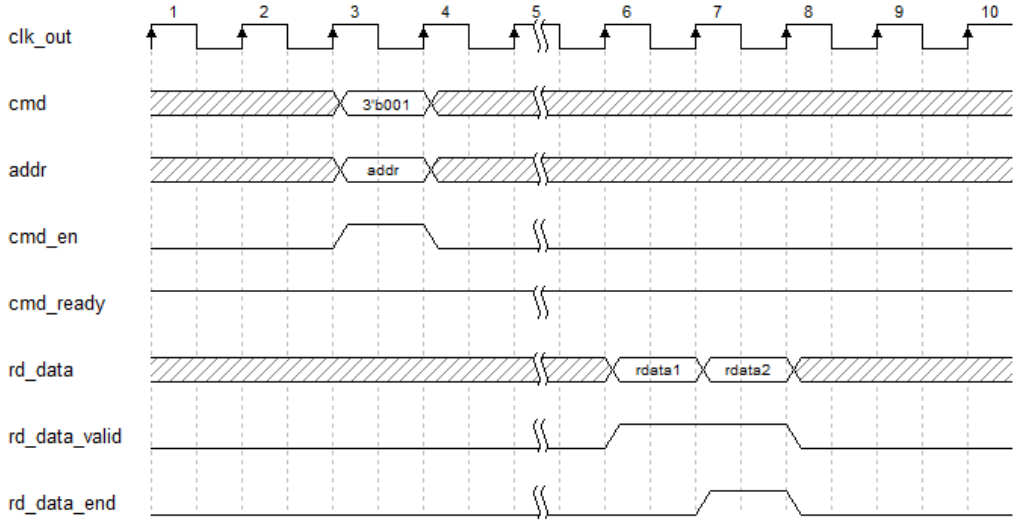
Similar to the write operation, when clock ratio is 1:2 and users configure the burst length with BL4, read data occupies one clk cycle, as shown in Figure 4-10.

Figure 4-10 Read Data Timing with 1:2 Clock Ratio and Burst Mode=BC4



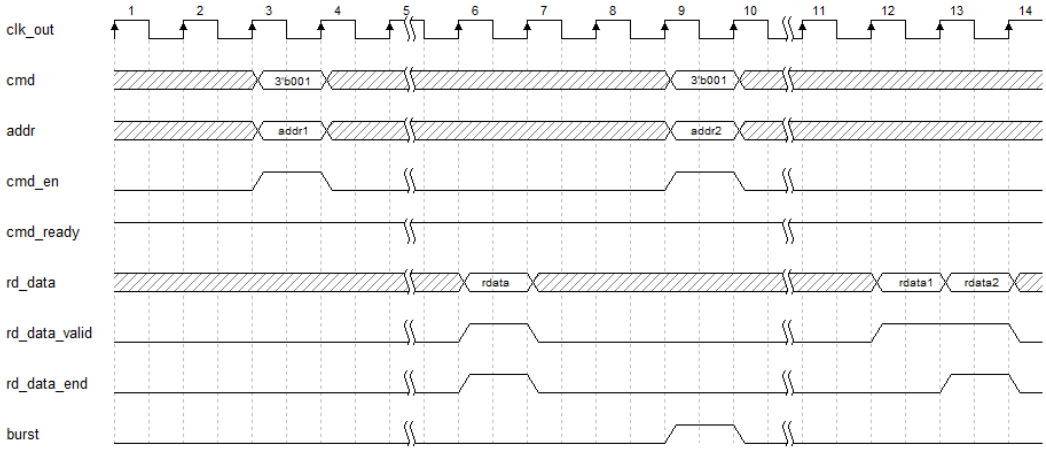
Similar to the write operation, when clock ratio is 1:2 and users configure the burst length with BL8, read data occupies two clk cycles, as shown in Figure 4-11.

Figure 4-11 Read Data Timing with 1:2 Clock Ratio and Burst Mode=BL8



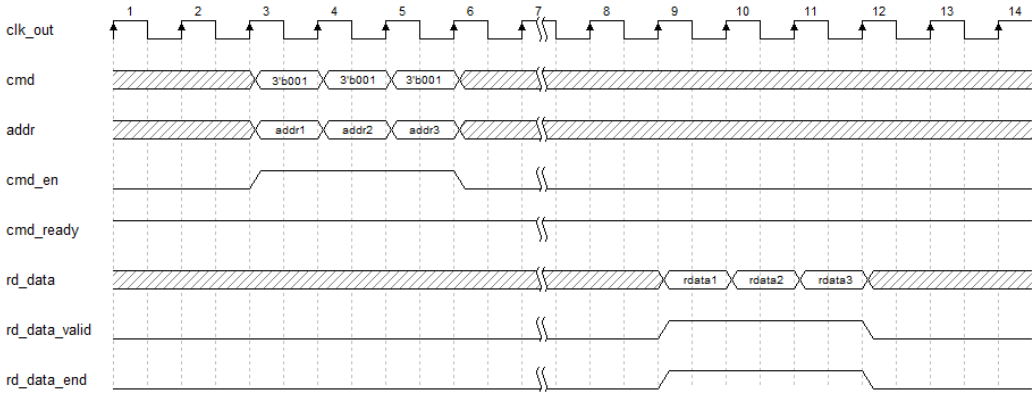
When clock ratio is 1:2 and users configure the burst mode with OTF (i.e., users can control the burst port to switch BL4 and BL8), when cmd_en is valid, burst 0 indicates read BL4 and the read data occupies one clk cycle; burst 1 indicates read BL8 and the read data occupies two clk cycles, as shown in Figure 4-12.

Figure 4-12 Read Data Timing with 1:2 Clock Ratio and Burst Mode= OTF



When the clock ratio is 1:4, the read data is returned sequentially according to the read command order, as shown in Figure 4-13.

Figure 4-13 Read Data Timing in Non-continuous Burst Mode with 1:4 Clock Ratio



4.4.6 Refresh

Refresh

The DDR3 SDRAM array needs to continually refresh to ensure the data is not lost. Therefore, Gowin DDR3 Memory Interface IP is required to send the refresh instruction to DDR3 SDRAM periodically. Gowin DDR3 Memory Interface IP requires ad interval of t_{REFI} time to generate refresh command; after the refresh command is generated, MC will precharge all banks after executing the last read/write command, and then execute Refresh command. The refresh operation has higher priority.

Self-Refresh

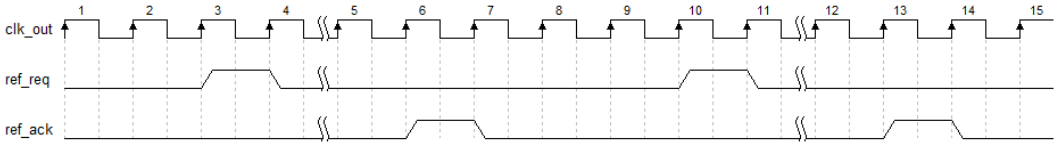
You can send a self-refresh request through the sr_req port and configure DDR3 SDRAM with self-refresh mode. In the self-refresh mode, DDR3 SDRAM will automatically refresh the memory array without a refresh instruction from Gowin DDR3 Memory Interface IP.

Gowin DDR3 Memory Interface IP will return the sr_ack signal to users after the self-refresh configuration of DDR3 SDRAM is completed, indicating that the DDR3 SDRAM is configured with self-refresh mode.

User Refresh

You can use this option to configure the refresh mode with user refresh mode. "USER_REFRESH" needs to be configured with "ON." You can send a refresh request to MC through ref_req port at any time without additional commands to MC through cmd port. When user refresh instruction is sent, ref_req need to hold at high level for one cycle. After the refresh instruction is sent, MC will feedback ref_ack signal which will hold at high level for one cycle, as shown in Figure 4-14.

Figure 4-14 User Refresh Timing



The user refresh operation may affect the instructions that MC has received or is executing. Before user refresh operation, MC completes the command operation being executed first. You should consider the coordination between the user refresh and other instructions to avoid t_{REFI} violation.

Considering the worst case, you can operate user refresh with reference to the following formula. Command a certain time to complete the transmission, which can be roughly calculated by parameters such as t_{RCD}, CL, data transmission time, t_{RP}, etc. And the user refresh should be completed before the time parameter t_{REFI} is violated, so the maximum interval between two user refresh times can be calculated by following formula.

$$t_{REFI} - (t_{RCD} + (CL + 4) \times t_{CK} + t_{RP}) \times nBA$$

In application, if a user refresh starts, you need to start a user refresh immediately after the DDR3 SDRAM completes initialization to establish the time base for subsequent user refresh requests.

5 IP Usage Notes

5.1 Clock and Reset

5.1.1 Clock

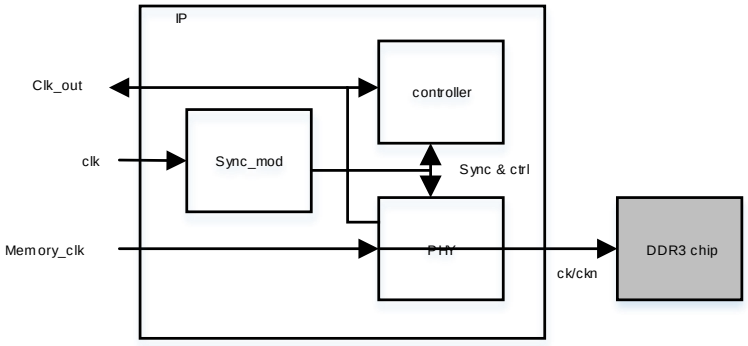
The IP has three clocks, two input clocks, clk and memory_clk, and one output clock, clk_out.

As shown in Figure 5-1, clk is used to generate some synchronization and control signals which act on the main body of the IP logic (PHY layer and Memory controller). clk is required to be a low-speed continuous clock with a recommended value of 50MHz, and the input of the on-board crystal can be connected to clk.

memory_clk is the high speed clock that uses HCLK resources to drive the PHY and output to the DDR3 chip.

clk_out is the divided clock of memory_clk; when clk_ratio=4:1, clk_out is the clock divided by four for memory_clk, using PCLK resource. clk_out is used as the logic processing clock for IP and output to user logic. IP User interface operations should be synchronized with clk_out.

Figure 5-1 Clock

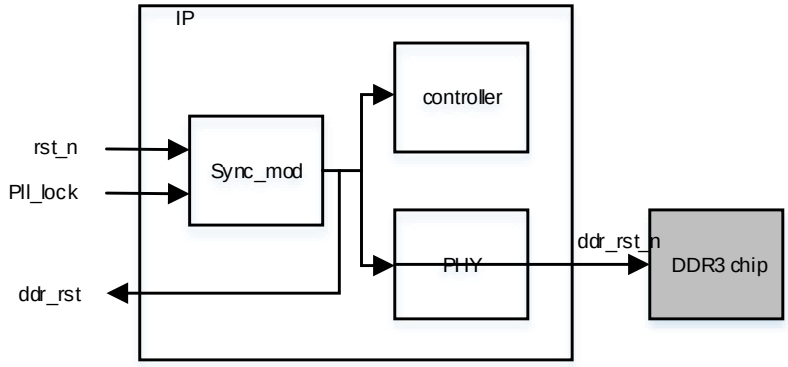


5.1.2 Reset

The IP has input signals rst_n and pll_lock and output signal ddr_rst. As shown in Figure 5-2, rst_n and pll_lock perform an or operation to generate ddr_rst as the global reset of IP, and output to the user. Any reset logic can be connected to rst_n; pll_lock can only be connected to the LOCK signal of PLL. If pll_lock is not connected to the LOCK signal of

PLL, the IP will not be able to detect the clock whether it is stable or not, and at this point It is easy to have DDR initialization failure.

Figure 5-2 Reset



5.2 pll_stop

pll_stop is a control signal present for the 5A(S)(T) device; it is a switch to control memory_clk, active-low. As shown in Figure 5-3 and Figure 5-4, when 138K devices are used, pll_stop is directly connected to enclk2 of PLL. When 25K devices are used, pll_stop needs to be connected to the adapter module, pll_mDRP_intf, to indirectly control the clkout2 output of PLL. The clk of pll_mDRP_intf is the same as the mdclk and clkin of PLL.

Figure 5-3 138k pll_stop

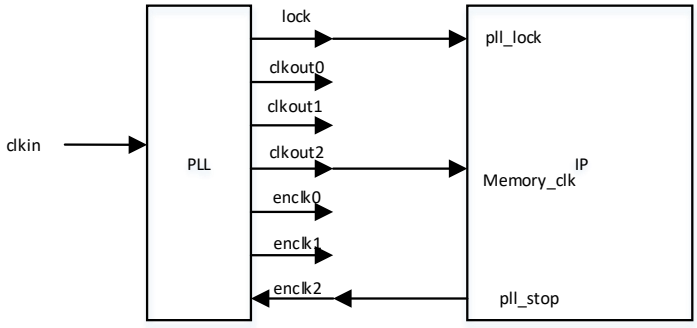
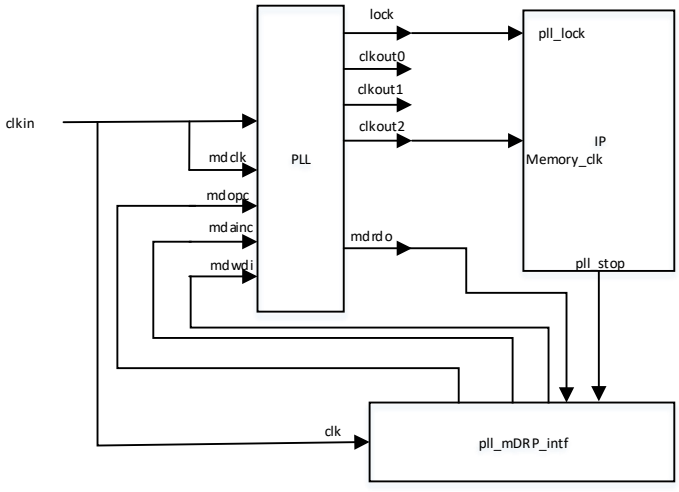


Figure 5-4 25K pll_stop



pll_mDRP_intf module is in the reference design of Gowin_DDR3_Memory_Interface_RefDesign, please download from official website.

6 Port List

The I/O ports of the Gowin DDR3 Memory Interface IP are as shown in Table 6-1.

Table 6-1 IO Port List of Gowin DDR3 Memory Interface IP

Signal	Data Width	I/O	Description
User Interface			
addr	ADDR_WIDTH	Input	Address input, configure parameter to set the signal width
cmd	3	Input	Command channel
cmd_en	1	Input	Command and address enable signals 0: invalid 1: valid
cmd_ready	1	Output	High indicates Memory Interface can receive commands and addresses.
rd_data	APP_DATA_WIDTH	Output	Read data channel
rd_data_end	1	Output	High indicates the end cycle of the current rd_data.
rd_data_valid	1	Output	rd_data valid signal: 0: invalid 1: valid
burst	1	Input	OTF control port, BL8 mode when 1'b1; BL4 mode when 1'b0, valid only in OTF mode
wr_data	APP_DATA_WIDTH	Input	Write data channel
wr_data_end	1	Input	High level indicates that the current clock cycle is the last cycle of this wr_data.
wr_data_mask	APP_MASK_WIDTH	Input	wr_data mask 0: disable 1: enable
wr_data_rdy	1	Output	High indicates MC can receive

Signal	Data Width	I/O	Description
			the user data.
wr_data_en	1	Input	wr_data write enable signal: 0: disable 1: enable
sr_req	1	Input	Self-refresh request
sr_ack	1	Output	Refresh the acknowledgement signal
ref_req	1	Input	User refresh request
ref_ack	1	Output	User refresh the acknowledgement signal
clk	1	Input	Reference input clock, generally PCB crystal input, 50M recommended.
memory_clk	1	Input	Memory interface frequency input by user; when GW2A devices used, this clock can be either the output clock of PLL or other clock; when GW5A devices used, this clock must be output from clkout2 of PLL.
pll_stop	1	output	For the details, you can see 5.2 pll_stop
pll_lock	1	Input	If memory_clk is PLL multiplication input, this interface is connected to the pll_lock of PLL, if you do not use PLL, this interface is connected to high level.
rst_n	1	Input	System reset input signal 0: enable 1: disable
init_calib_complete	1	Output	Initialization completed signal
clk_out	1	Output	User design clock with a frequency of 1/2 Memory Clk
ecc_err	APP_DATA_WIDTH/32	Output	ECC indicates signal output
ddr_rst	1	Output	The reset signal that IP processed is used for user design, high reset.
DDR3 SDRAM Interface			
O_ddr_addr	ROW_WIDTH	Output	Row address (activation command), Column address (read/write command)
O_ddr_bank	BANK_WIDTH	Output	Bank address
O_ddr_cs_n	CS_WIDTH	Output	Chip selected, active-low.
O_ddr_ras_n	1	Output	Row address selection signal

Signal	Data Width	I/O	Description
O_ddr_cas_n	1	Output	Column address selection signal
O_ddr_we_n	1	Output	Row write enable
O_ddr_ck	CK_WIDTH	Output	A clock signal provided to DDR3 SDRAM
O_ddr_ck_n	CK_WIDTH	Output	Compose a differential signal with ddr_ck
O_ddr_cke	CKE_WIDTH	Output	DDR3 SDRAM clock enable signal
O_ddr_odt	ODT_WIDTH	Output	Terminating resistor control of memory signal
O_ddr_reset_n	1	Output	DDR3 SDRAM reset signal
O_ddr_dm	DM_WIDTH	Output	DDR3 SDRAM data masking signal
IO_ddr_dq	DQ_WIDTH	Bidirection	DDR3 SDRAM data
IO_ddr_dq	DQS_WIDTH	Bidirection	DDR3 SDRAM data strobe signal
IO_ddr_dqs_n	DQS_WIDTH	Bidirection	Compose a differential signal with ddr_dqs

7 Parameter Configuration

Gowin DDR3 Memory Interface IP supports DDR3 SDRAM devices. You need to configure various of static parameters and timing parameters of Gowin DDR3 Memory Interface according to the design requirements, as shown in Table 7-1 and Table 7-2.

Table 7-1 Static Parameter Options of Gowin DDR3 Memory Interface

Name	Description	Options
Memory Type	Memory type	MT41J128M16JT-125k Custom
Memory Clock	Chip Interface Clock Frequency	Write according to the chip operating clock and demand
CLK Ratio	Ratio of user interface clock frequency to chip interface clock frequency	1:4, 1:2
DIMM Type	Chip DIMM Type	Components, RDIMMs, UDIMMs, SODIMMs
Dq Width	Dq Data Bit Width	8, 16, 24, 32, 40, 48, 56, 64, 72
Dram Width	Data bit width of single chip	4, 8, 16
Rand Address	Rand Address	Select 1 for single and dual rank devices
Bank Address	Memory BANK address width	Select according to DDR3 SDRAM chip
Row Address	Memory line address width	Select according to DDR3 SDRAM chip
Column Address	Memory column address width	Select according to DDR3 SDRAM chip
Burst Mode	Chip Burst Mode	"4", "8", "OTF"; 4 or OTF is supported when clock ratio is 1:2; 8 is supported when clock ratio is 1:4.
Burst Type	Chip Burst Type	"Sequential" "Interleaved"
CAS latency	CAS delay time	5，6，7，8
Additive latency	Additive delay time	0, CL-1, CL-2

Name	Description	Options
CW Latency	CWL delay time	Choose according to the actual situation.
RTT NOM	Nominal ODT value	"OFF": OFF "20": 20 "30": 30 "40": 40 "60": 60 "120": 120
RTT WR	The Dynamic ODT value in Multiple-RANK used for the write interface. For Single-Component design, RTT_WR is invalid.	"OFF": RTT_WR disabled "120": RZQ/2 "60": RZQ/4
USER_REFRESH	Whether to control the refresh operation by the user	"ON", "OFF"

Table 7-2 DDR3 Time Parameter

Name	Description
t_{CK}	Memory interface clock period (ps)
t_{CKE}	Minimum pulse time of CKE signal (ps)
t_{FAW}	The interval between simultaneous activation commands of more than four lines in the same rank is allowed, so the minimum value should be no less than four times the $t_{RRD.}$
t_{RAS}	Time from ACTIVE to PRECHARGE
t_{RCD}	Time from ACTIVE to READ/WRITE
t_{REFI}	Memory refresh interval
t_{RFC}	The interval from REFRESH to ACTIVE/REFRESH
t_{RP}	PRECHARGE cycle
t_{RRD}	The interval from ACTIVE to ACTIVE
t_{RTP}	The interval from READ to PRECHARGE
t_{WTR}	The interval from WRITE to READ
AL	Additive latency
CL	CAS latency

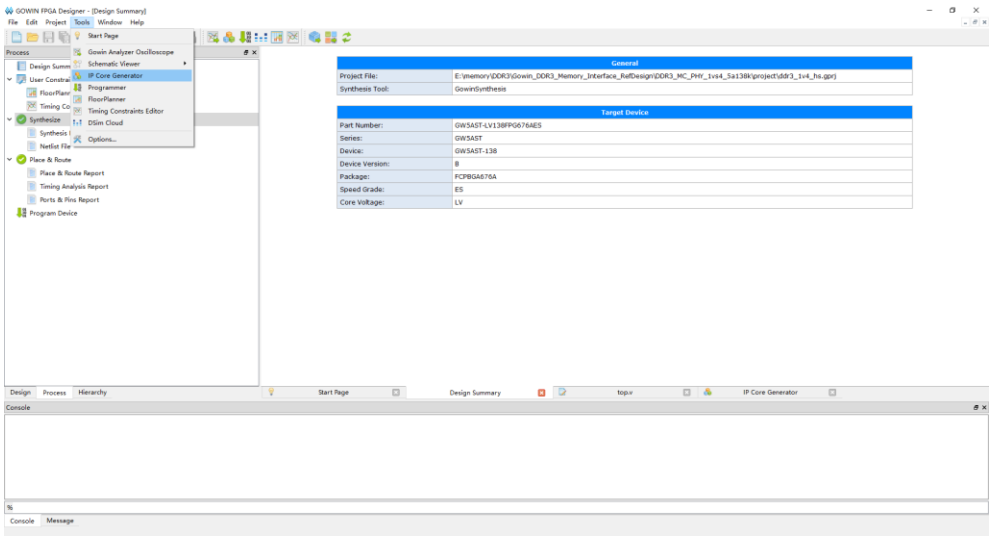
8 Interface Configuration

You can invoke and configure the Gowin DDR3 Memory Interface IP using the IP Core Generator tool in the IDE. This chapter takes AD3U160022G11 memory chip as an example, introduces the main configuration interface, configuration flow and the meaning of each configuration option (Take the clock ratio of 1:2 as an example).

1. Open IP Core Generator

After creating the project, click the "Tools" tab in the upper left, click “IP Core Generator” to open Gowin IP Core Generator via the drop-down list, as shown in Figure 8-1.

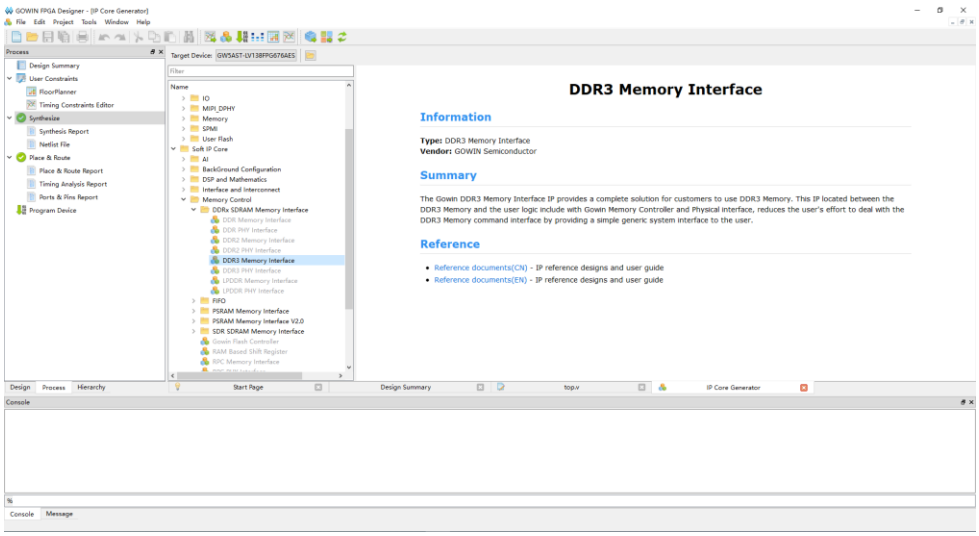
Figure 8-1 Open IP Core Generator



2. Open the DDR3 Memory Interface IP core.

Click DDR option, double-click DDR3 Memory Interface. The configuration interface of DDR3 Memory Interface IP core is as shown in Figure 8-2.

Figure 8-2 Open DDR3 Memory Interface IP Core

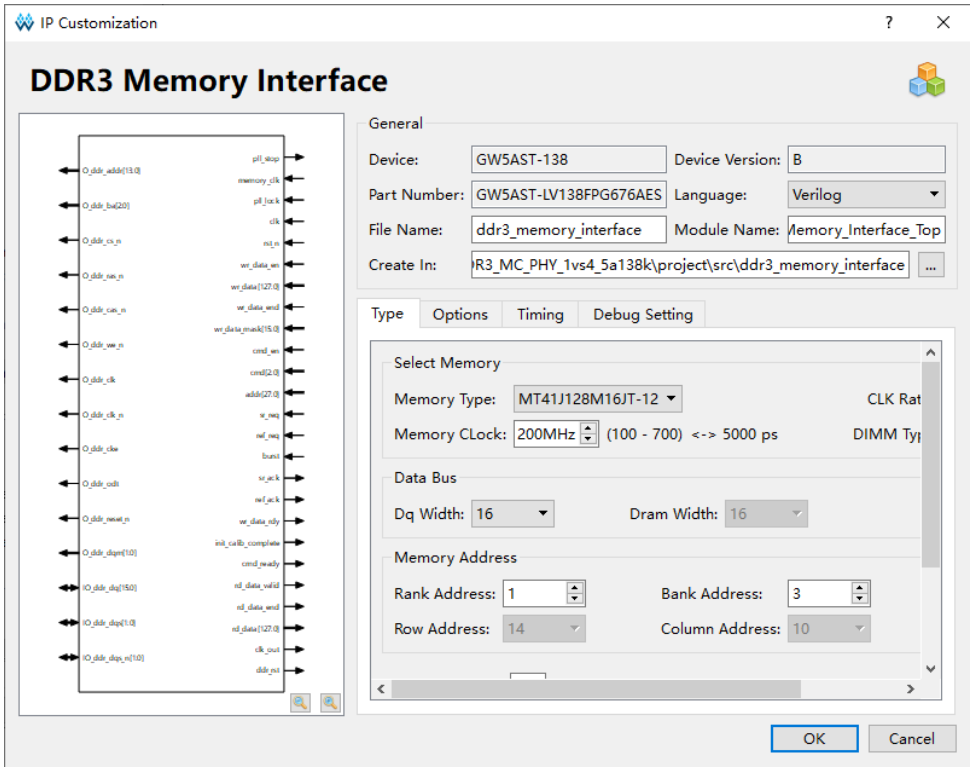


3. DDR3 Memory Interface IP Core Interface

The interface diagram of the DDR3 Memory Interface IP core is on the left, as shown in Figure 8-3.

The left is the interface of DDR3 Memory Controller and the user end. You can connect your design to the DDR3 Memory Interface IP to send/receive commands and data. The right is the interface of the PHY and DDR3 chip. You can save and access data by connecting the DDR3 Memory Interface IP and DDR3 chip. With different configuration information, the signal bit width and the signal number will change accordingly.

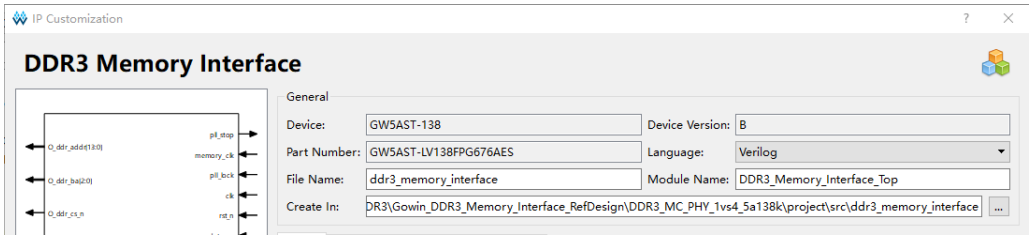
Figure 8-3 IP Core Interface



4. Configure Basic Information

See the basic information in the upper part of the configuration interface. The Module Name displays the top-level file name of the generated project, and the default is "ddr3_memory_interface_top", and you can modify the name. The File Name displays the folder generated by the IP core, which contains the files required by DDR3 Memory Interface IP core, and the default is "v", and you can modify the path. Create IN displays the path of IP core folder. The default is "\project path\src\DDR3_Memory_Interface", and you can modify the path. "Add to Current Project" in the lower right is used to ask you whether to add the generated IP to your project. The default is checked, as shown in Figure 8-4.

Figure 8-4 Basic Information Configuration Interface

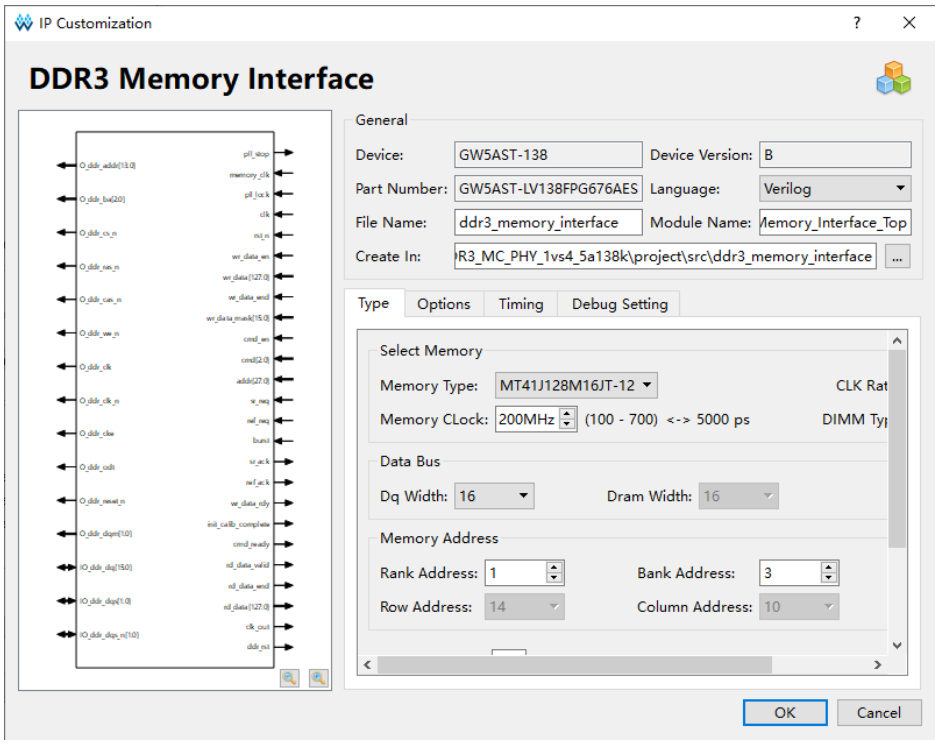


5. Type Options

In the Type Option, you need to configure the basic information for the DDR3 memory chip.

- Select Memory Option
- Data Bus Option
- Memory Address Option: In the Memory Address option, you can mainly fill in the Address information of the Rank, Bank, Row, and Column of the DDR3 Memory chips. After choosing the type of DDR3 Memory chip, GUI will be automatically fill in; if you choose the Custom, you need to optionally choose according to the DDR3 Memory type.
- Non-configurable items are grayed out.

Figure 8-5 Type Tab

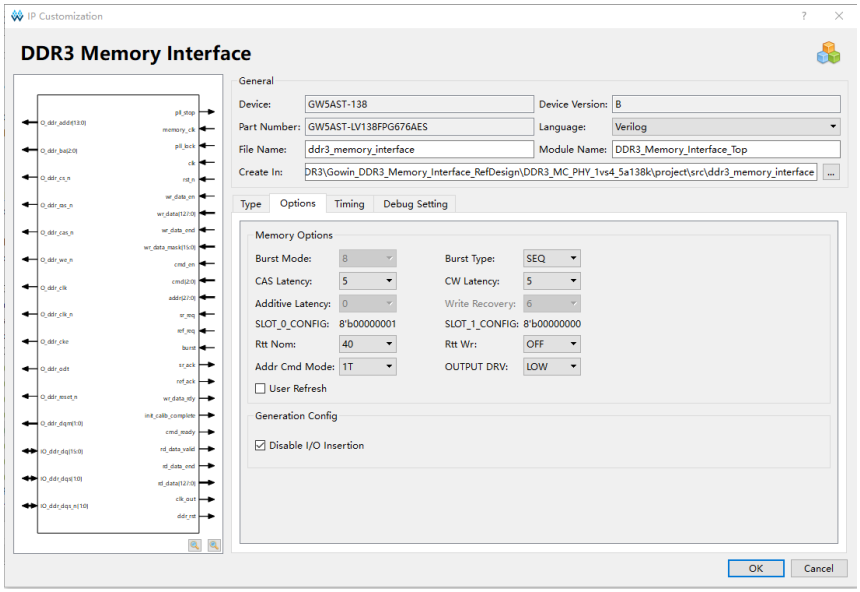


6. Options is as shown in Figure 8-6, and take "MT41J128M16JT-125K" memory chip as an example.

   - Memory option
   - Generation Config Option

   When checked, in the generated IP, IBUF, OBUF, and the other primitives are not inserted, you can directly use port to connect to the logic, checked by default.

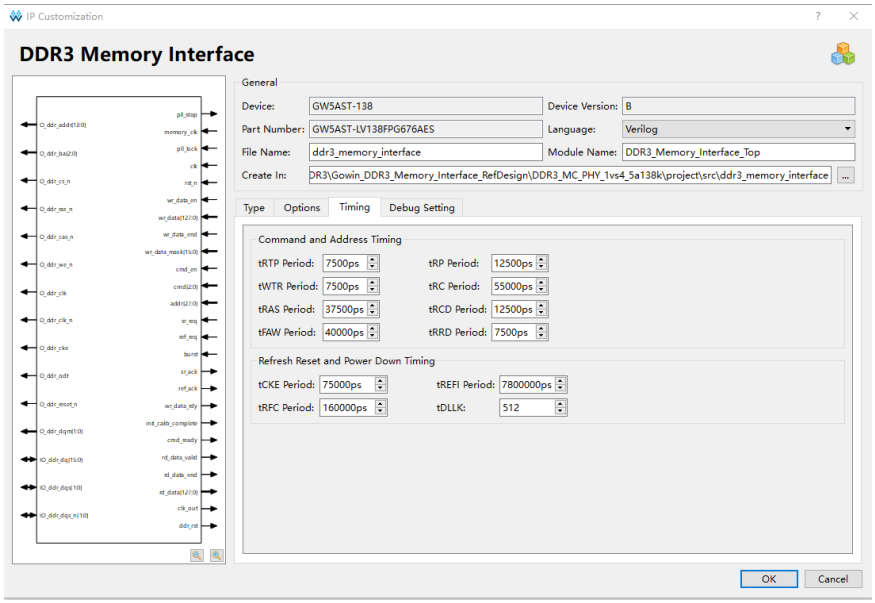
Figure 8-6 Options Tab



7. Timing Option

- Command and Address Timing Option
- Refresh, Reset and Power Timing option

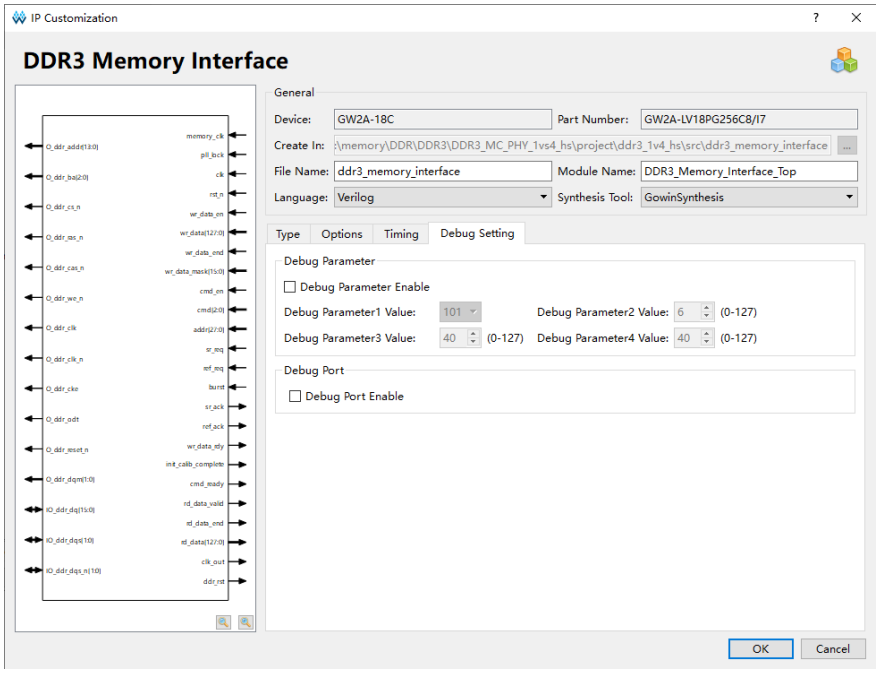
Figure 8-7 Timing Tab



8. Debug Setting Option

- This option is used to enable debug interface and debug parameters.

Figure 8-8 Debug Setting Options

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