Gowin Customized PHY IP

User Guide

IPUG1024-1.5E, 05/17/2024

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Revision History

Date	Version	Description
07/21/2023	1.0E	Initial version published.
09/08/2023	1.1E	Analog Front End (AFE) configuration option added.
10/12/2023	1.2E	● The range of TX Line Rate updated to 0.025Gbps~12.5Gbps. ● TX Line Rate Ratio option and its descriptions added.
03/07/2024	1.3E	Descriptions of AFE configuration option added.
04/12/2024	1.4E	Descriptions of DRP added.
05/17/2024	1.5E	Descriptions of Clock Schematic and Reconfiguration added.

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1 About This Guide

1.1 Purpose

Gowin Customized PHY IP User Guide is to help you learn the features and usage of Gowin Customized PHY IP by providing descriptions of features, functions, GUI, and reference design, etc. The software screenshots in this manual are based on 1.9.9.03. As the software is subject to change without notice, some information may not remain relevant and may need to be adjusted according to the software that is in use.

1.2 Related Documents

You can find the related documents at www.gowinsemi.com:

- SUG100, Gowin Software User Guide
- DS981, GW5AT series of FPGA Products Data Sheet
- DS1104, GW5AST series of FPGA Products Data Sheet

1.3 Terminology and Abbreviations

Table 1-1 shows the abbreviations and terminology used in this manual.

Table 1-1 Terminology and Abbreviations

Terminology and Abbreviations	Meaning
AFE	Analog Front End
ATT	Attenuator
FFE	Feed-Forward Equalization
FPGA	Field Programmable Gate Array
IP	Intellectual Property
PCS	Physical Coding Sublayer
CDR	Clock and Data Recovery
RXEQ	Receive Equalization

1.4 Support and Feedback

Gowin Semiconductor provides customers with comprehensive technical support. If you have any questions, comments, or suggestions, please feel free to contact us directly using the information provided below.

Website: www.gowinsemi.com

E-mail: support@gowinsemi.com

2 Function

2.1 Overview

Gowin Customized PHY IP supports flexible configuration of Gowin SerDes functions such as Line Rate, Reference Clock, Data Width, 8B10B Encoding/Decoding, Channel Bonding, and RX Clock Correction, etc.

Table 2-1 Gowin Customized PHY IP Overview

Gowin Customized IP	
Logic Resource	See 2.3 Resource Utilization
Delivered Doc.	
Design Files	Verilog (encrypted)
Reference Design	Verilog
TestBench	Verilog
Test and Design Flow	
Synthesis Software	GowinSynthesis
Application Software	Gowin Software (V1.9.9 Beta-1 and above)

Note!

For the devices supported, you can click here to get the information.

2.2 Features

- Supports line rate configuration with the range of 1Gbps~12.5Gbps
- Supports low TX line rate, with a minimum of 25 Mbps
- Supports reference clock frequency configuration with the range of 50MHz~800MHz
- Supports PLL with options of CPLL or QPLL
- Supports user data widths of 8/10/16/20/32/40/64/80
- Supports 8B10B encoding and decoding
- Supports Word Alignment
- Supports Channel Bonding
- Supports RX Clock Correction

2.3 Resource Utilization

Gowin Customized PHY IP is used to only configure SerDes and does not occupy any Fabric resources.

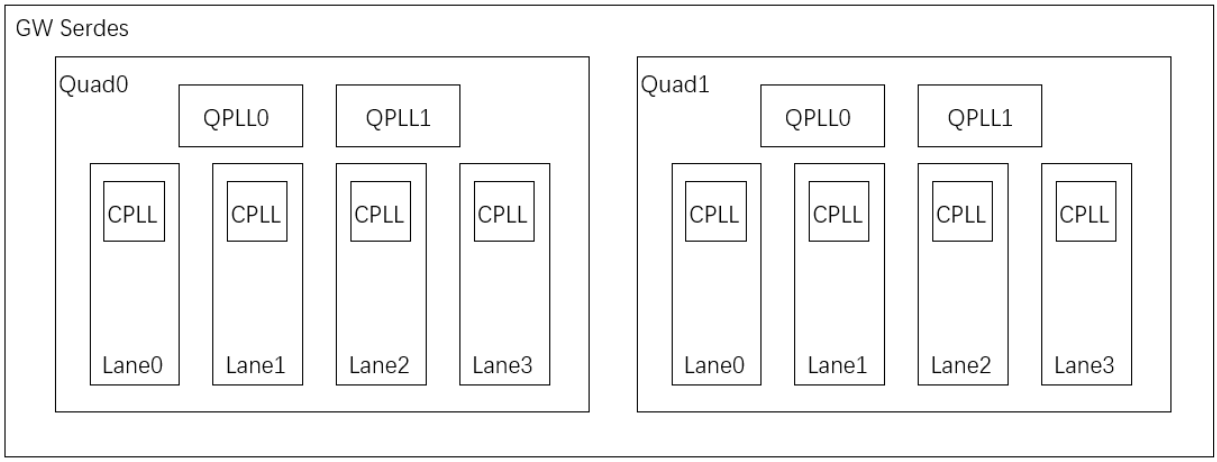
3 Functional Description

3.1 System Block Diagram

Gowin SerDes includes 2 Quads, and each Quad contains 4 separate lanes; there are a total of 8 lanes available to users. Each Quad contains 2 QPLLs and 4 CPLLs, where the QPLLs can be shared by the 4 lanes of the Quad where it is located, and the CPLLs can only be used by the lane where it is located.

Each Quad has two independent reference clock input pins, and the input reference clock can be used as the reference clock source for QPLL and CPLL. The SerDes block diagram is shown in Figure 3-1.

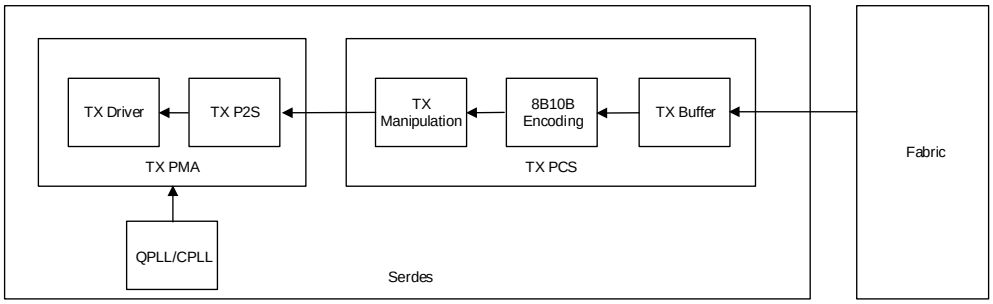
Figure 3-1 SerDes Block Diagram



3.2 Modules

3.2.1 Transmit

Figure 3-2 Transmit in SerDes

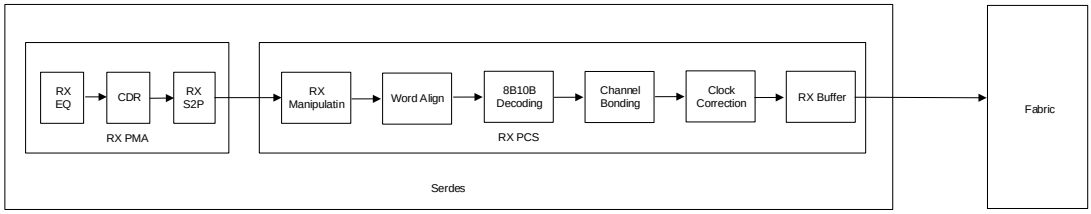


As shown above, the transmit consists of the following five modules:

- TX Driver: Provides the driver for the analog of the transmit lane to convert the serial data to differential data to output to the IO of chip.
- TX P2S: Converts TX parallel data of PCS to serial data and outputs to TX Driver, and the parallel data supports 8/10/16/20 bit widths.
- TX Manipulation: Before the data is transmitted to the TX P2S, parallel data can be manipulated such as bit polarity inversion, high and low bit swapping, and byte inversion; and this module supports bypass.
- 8B10B Encoding: Realizes 8B10B encoding, and this module supports bypass.
- TX Buffer: Realizes the TX data width conversion, and supports 1:1, 1:2, 1:4 ratios. At the same time, the frequency of the clock output to the Fabric is reduced according to the ratio.

3.2.2 Receive

Figure 3-3 Receive in SerDes



As shown above, the receive consists of the following five modules:

- RXEQ: Equalizes the RX differential data to provide a stable eye diagram for CDR module.
- CDR: Extracts the clock of RX data and aligns the data center position.
- S2P: Converts the RX serial data to parallel data and outputs to PCS, and the parallel data supports 8/10/16/20 bit widths.
- RX Manipulation: After the data enters PCS, parallel data can be

manipulated such as bit polarity inversion, high and low bit swapping, byte inversion, and this module supports bypass.

- Word Align: Slips auto-received data to achieve the function of aligning K character, and this module supports bypass.
- 8B10B Decoding: 8B10B decodes RX data, and this module supports bypass.
- Channel Bonding: Aligns RX data of multiple channels, and this module supports bypass.
- Clock Correction: Realizes clock correction for RX data by adding or removing certain fields, and this module supports bypass.
- RX Buffer: Realizes RX data width conversion, and supports 1:1, 1:2, 1:4 ratios; at the same time, the frequency of the clock output to the Fabric is reduced according to the ratio.

3.3 Clock

3.3.1 Transmit Clock

The transmit clock is generated by the CPLL/QPLL. When configuring the TX lane, you need to configure the TX lane rate, the PLL used (CPLL/QPLL), and the reference clock source and its frequency. Based on the above configuration, the IP configures SerDes PLL to generate a high-speed clock for data transmission. At the same time, SerDes will divide the high-speed clock according to the user configuration; then output the clock to Fabric to be used as Fabric TX clock. The frequency of the TX clock outputted to Fabric is calculated as follows:

- If the TX lane rate is ≥ 1Gbps, then

  F=TX lane rate[1]/Fabric data width

Note!

[1]The input value of TX Line Rate on the GUI.

For example, if the user configures the TX data rate to be 1.25Gbps and configures the TX parallel data width to be 40 bits, the Fabric TX clock is 1.25Gbps/40=31.25MHz.

- If the TX lane rate is < 1Gbps, then

  F=TX lane rate[1] X Ratio[2]/Fabric data width

Note!

- [1] The input value of TX Line Rate on the GUI.
- [2] The Ratio value on the GUI with the options 5x=5, 10x=10, 20x=20, 40x=40

For example, if the user configures TX data rate to be 0.5Gbps, the Ratio is configured to be 5x, and the TX parallel data width is configured to be 40 bits, then the Fabric TX clock will be (0.5Gbps×5)/40=62.5MHz.

3.3.2 Receive Clock

When configuring the RX lane, you need to configure the RX lane rate.

The RX clock is recovered from data through CDR, and the recovered serial data clock output from CDR is used for the RX S2P module. At the same time, SerDes will divide the serial data clock according to the user configuration; then output the clock to Fabric to be used as Fabric RX clock. The frequency of the RX clock outputted to Fabric is calculated as follows:

F= RX lane rate/Fabric data width

For example, if the user configures the RX data rate to be 1.25Gbps and configures the RX parallel data width to be 40 bits, the Fabric TX clock is 1.25Gbps/40=31.25MHz.

3.4 Data

3.4.1 Transmit Data

TX Data Width

TX Data Width is determined by the Internal Data Width and TX External Data Ratio options.

You can configure SerDes internal data width through Internal Data Width, and configure the ratio of TX Buffer converting the internal width to the user interface width through TX External Data Ratio. When the user selects a larger width, the priority is to configure the Internal Data Width to the maximum. For example, when you configure a bit width of 40, you need to configure Internal Data Width=20 and TX External Data Ratio=1:2.

Note!

The Internal Data Width needs to be the same for RX and TX directions.

8B10B Encoding

8B10B Encoding module can realize TX Data 8B10B encoding. When the Internal Data Width is configured to 10 or 20, the user can choose to enable/disable this function. When the Internal Data Width is configured to 8 or 16, the user cannot enable this function.

When the user disables this function, the data transmitted from the Fabric is Raw Data; when the user enables this function, the data transmitted from the Fabric is the K character indication and the data before encoding.

Channel Bonding

The Channel Bonding module can realize the bonding of multiple TX channels. When the user does not check the option, this function is disabled. When the user checks the option, SerDes uses TX Buffer to achieve this function. After enabling this function, you need to configure Master Channel; in general, you can choose any one in the selected channel. Finally, you need to configure Read Start Depth to control read

start depth of the TX Buffer.

3.4.2 Receive Data

RX Data Width

RX Data Width is determined by the Internal Data Width and RX External Data Ratio options.

You can configure SerDes internal data width through Internal Data Width, and configure the ratio of RX Buffer converting the internal width to the user interface width through RX External Data Ratio. For example, when you configure a bit width of 40, you need to configure Internal Data Width=20 and RX External Data Ratio=1:2.

Note!

The Internal Data Width needs to be the same for RX and TX directions.

Word Alignment

The Word Alignment module can realize RX data alignment. When the user enables this function, the module aligns the boundary of the RX parallel data according to the Pattern configured by the user, so that the output parallel data is consistent with the configured K character. When the user enables 8B10B decoding function, this module needs to be enabled.

8B10B Decoding

8B10B Encoding module can realize RX Data 8B10B decoding. When the Internal Data Width is configured to 10 or 20, the user can choose to enable/disable this function. When the Internal Data Width is configured to 8 or 16, the user cannot enable this function.

When the user disables this function, the data received from the Fabric is Raw Data; when the user enables this function, the data received from the Fabric is the K character indication and the data after decoding.

Channel Bonding

The Channel Bonding module can realize the bonding of multiple RX channels. When the user selects None, this function is disabled. When the user selects One Word/Two Words/Four Words, IP automatically enables this function, and the number of aligned Pattern is configured. After enabling this function, you need to configure Master Channel; in general, you can choose any one in the selected channel. Finally, align Pattern, Max Skew, and Read Start Depth. Pattern and Max Skew alignment is configured according to the specific protocol. Pattern alignment supports a maximum of 4 bytes, and the first Pattern must be a K character.

When the user enables this function, 8B10B Decoding and Word Alignment must be enabled first.

Clock Correction

The Clock Correction module can realize the conversion of RX data clock domain. When the user selects None, this function is disabled. When the user selects One Word/Two Words, IP automatically enables this

function, and the number of Correction Pattern is configured. After enabling this function, you need to configure Master Channel; in general, you can choose any one in the selected channel. Finally, configure Correction Pattern and Read Start Depth. Correction Pattern is configured according to the specific protocol. Correction Pattern supports a maximum of 2 bytes, and the first Pattern must be a K character.

The Clock Source option in RX Clock Correction page allows the user to set the RX clock source, i.e., which clock source to place the RX clock to. User option means setting Clock Source as Fabric input clock (e.g. q0_ln0_cc_clk_i) and TX option means setting Clock Source as TX clock. The q0_ln0_cc_clk_i input clock frequency is:

F=RX Lane Rate/Internal Data Width

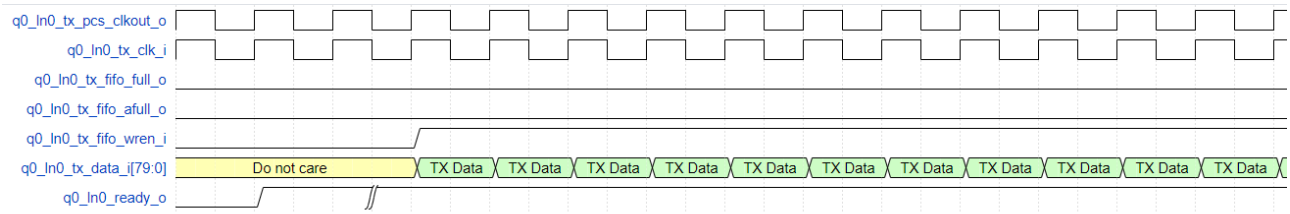
3.5 User Interface

SerDes user interface is in the form of FIFO, and its read and write operations are similar to those of FIFO.

3.5.1 Transmit Data

TX Line Rate≥1Gbps

Figure 3-4 Transmit Data Interface Timing When TX Rate≥1Gbps



As shown in Figure 3-4, Quad0 Lane0 is used as an example.

- q0_ln0_tx_pcs_clkout_o is the SerDes PCS TX clock, which is used as the read clock for the TX Buffer.
- q0_ln0_tx_clk_i is the input clock, which is used as the write clock for TX Buffer. This clock can be directly connected to q0_ln0_tx_pcs_clkout_o to achieve the same frequency of TX Buffer read and write clocks.
- q0_ln0_tx_fifo_full_o is the TX Buffer full signal; 1 means full and 0 means non-full.
- q0_ln0_tx_fifo_afull_o is the TX Buffer almost full signal; 1 means almost full and 0 means non-almost full.
- q0_ln0_tx_fifo_wren_i is TX Buffer write enable; 1 means write valid and 0 means write invalid.
- q0_ln0_tx_data_i is the write data for TX Buffer. When q0_ln0_tx_fifo_wren_i is 1, q0_ln0_tx_data_i writes TX Buffer. When q0_ln0_tx_fifo_wren_i is 0, q0_ln0_tx_data_i does not write TX Buffer.
- q0_ln0_tx_fifo_wrusewd_o indicates how much data is stored in the

TX Buffer.

As shown in the Figure 3-4, when TX Buffer read and write clocks are at the same frequency, q0_ln0_tx_fifo_full_o and q0_ln0_tx_fifo_afull_o are constant 0, indicating that TX Buffer always has space left for data write. At this point, you can set q0_ln0_tx_fifo_wren_i to 1 and q0_ln0_tx_data_i is written as a continuous data stream.

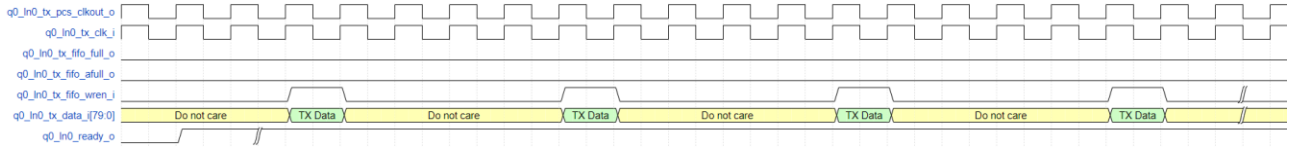
TX Line Rate < 1Gbps

When TX Line Rate < 1Gbps is configured, the corresponding Ratio configuration option on the interface is enabled. The user needs to ensure that TX Line Rate X Ratio[1] ≥ 1Gbps.

Note!

[1] The Ratio value on the GUI with the options 5x=5, 10x=10, 20x=20, 40x=40

Figure 3-5 Transmit Data Interface Timing When TX Rate＜1Gbps



As shown in Figure 3-5, using Quad0 Lane0, Ratio=5x as an example:

- q0_ln0_tx_pcs_clkout_o is the SerDes PCS TX clock, which is used as the read clock for TX Buffer.
- q0_ln0_tx_clk_i is the input clock, which is used as the write clock for TX Buffer. This clock can be directly connected to q0_ln0_tx_pcs_clkout_o to achieve the same frequency of TX Buffer read and write clocks.
- q0_ln0_tx_fifo_full_o is the TX Buffer full signal; 1 means full and 0 means non-full.
- q0_ln0_tx_fifo_full_o is the TX Buffer almost full signal; 1 means almost full and 0 means non-almost full.
- q0_ln0_tx_fifo_wren_i is the TX Buffer write enable, 1 means write valid and 0 means write invalid.
- q0_ln0_tx_data_i is the write data for TX Buffer. When q0_ln0_tx_fifo_wren_i is 1, q0_ln0_tx_data_i writes TX Buffer. When q0_ln0_tx_fifo_wren_i is 0, q0_ln0_tx _data_i does not write buffer.
- q0_ln0_tx_fifo_wrusewd_o indicates how much data is stored in the TX Buffer.

As shown in the figure, when the TX Buffer read and write clocks are at the same frequency, data can be written every 5 clock cycles, at which time q0_ln0_tx_fifo_full_o and q0_ln0_tx_fifo_afull_o are constant 0, indicating that the TX Buffer has always has space left for data write.

Similarly, when Ratio=10x, data is written every 10 clock cycles; when Ratio=20x, data is written every 20 clock cycles; when Ratio=40x, data is

written every 40 clock cycles. The above operations ensure that the TX Buffer read and write operations are performed at the same cycles, and without read empty or write full.

In addition to the above operation, users can write data according to the mode of writing to FIFO according to the design requirements. For example, when the TX Buffer is detected to be full, data can be written.

q0_ln0_tx_data_i is the TX data input with 80 bits, low first. The meaning represented by each bit is different in different encoding and bit width modes, which can be referred in Table 3-1, Table 3-2, Table 3-3.

Table 3-1 x8 Bit Width Configuration When 8B10B Encoding Disabled

q0_ln0_tx_data_i bit[n]	width=8	width=16	width=32	width=64
7~0	7~0	7~0	7~0	7~0
8	N/A	N/A	N/A	N/A
9	N/A	N/A	N/A	N/A
17~10	N/A	15~8	15~8	15~8
18	N/A	N/A	N/A	N/A
19	N/A	N/A	N/A	N/A
27~20	N/A	N/A	23~16	23~16
28	N/A	N/A	N/A	N/A
29	N/A	N/A	N/A	N/A
37~30	N/A	N/A	31~24	31~24
38	N/A	N/A	N/A	N/A
39	N/A	N/A	N/A	N/A
47~40	N/A	N/A	N/A	39~32
48	N/A	N/A	N/A	N/A
49	N/A	N/A	N/A	N/A
57~50	N/A	N/A	N/A	47~40
58	N/A	N/A	N/A	N/A
59	N/A	N/A	N/A	N/A
67~60	N/A	N/A	N/A	55~48
68	N/A	N/A	N/A	N/A
69	N/A	N/A	N/A	N/A
77~70	N/A	N/A	N/A	63~56
78	N/A	N/A	N/A	N/A
79	N/A	N/A	N/A	N/A

Note!

In a certain width mode, only the grayed bits need to be considered.

Table 3-2 x10 Bit Width Configuration When 8B10B Encoding Disabled

q0_ln0_tx_data_i bit[n]	width=10	width=20	width=40	width=80
9~0	9~0	9~0	9~0	9~0
19~10	N/A	19~10	19~10	19~10

q0_ln0_tx_data_i bit[n]	width=10	width=20	width=40	width=80
29~20	N/A	N/A	29~20	29~20
39~30	N/A	N/A	39~30	39~30
49~40	N/A	N/A	N/A	49~40
59~50	N/A	N/A	N/A	59~50
69~60	N/A	N/A	N/A	69~60
79~70	N/A	N/A	N/A	79~70

Note!

In a certain width mode, only the grayed bits need to be considered.

Table 3-3 x10 Bit Width Configuration When 8B10B Encoding Enabled

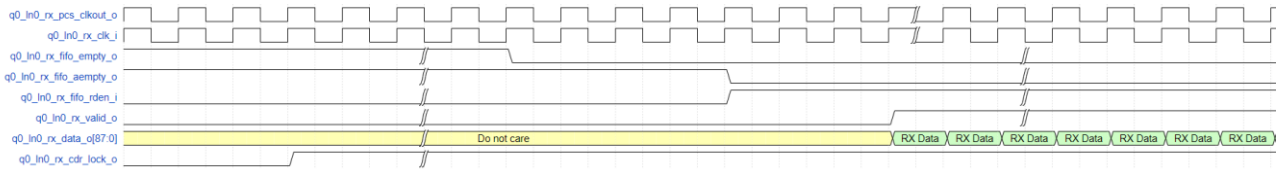
q0_ln0_tx_data_i bit[n]	width=10	width=20	width=40	width=80
7~0	Code	Code	Code	Code
8	K	K	K	K
9	N/A	N/A	N/A	N/A
17~10	N/A	Code	Code	Code
18	N/A	K	K	K
19	N/A	N/A	N/A	N/A
27~20	N/A	N/A	Code	Code
28	N/A	N/A	K	K
29	N/A	N/A	N/A	N/A
37~30	N/A	N/A	Code	Code
38	N/A	N/A	K	K
39	N/A	N/A	N/A	N/A
47~40	N/A	N/A	N/A	Code
48	N/A	N/A	N/A	K
49	N/A	N/A	N/A	N/A
57~50	N/A	N/A	N/A	Code
58	N/A	N/A	N/A	K
59	N/A	N/A	N/A	N/A
67~60	N/A	N/A	N/A	Code
68	N/A	N/A	N/A	K
69	N/A	N/A	N/A	N/A
77~70	N/A	N/A	N/A	Code
78	N/A	N/A	N/A	K
79	N/A	N/A	N/A	N/A

Note!

In a certain width mode, only the grayed bits need to be considered.

3.5.2 Receive Data

Figure 3-6 Receive Data Interface Timing



As shown in Figure 3-6, taking Quad0 Lane0 as an example, when the user monitors that q0_ln0_rx_cdr_lock_o is 1, it means that the RX CDR has entered the lock status.

- q0_ln0_rx_pcs_clkout_o is the SerDes PCS RX clock, which is used as the write clock for RX Buffer.
- q0_ln0_rx_clk_i is the input clock, which is used as the RX Buffer write clock. This clock can be directly connected to q0_ln0_rx_pcs_clkout_o to achieve the same frequency of RX Buffer read and write clocks.
- q0_ln0_rx_fifo_empty_o is the RX Buffer empty signal; 1 means empty and 0 means non-empty.
- q0_ln0_rx_fifo_aempty_o is the RX Buffer almost empty signal; 1 means almost empty and 0 means non-almost empty.
- q0_ln0_rx_fifo_rden_i is RX Buffer read enable; 1 means read valid and 0 means read invalid.
- q0_ln0_rx_data_o is the read data for RX Buffer read data. When q0_ln0_rx_fifo_rden_i is 1, read data from RX Buffer. When q0_ln0_rx_fifo_rden_i is 0, RX Buffer data is not read.
- q0_ln0_rx_valid_o indicates that q0_ln0_rx_data_o is valid. When q0_ln0_rx_fifo_rden_i is 1, the data will be output to q0_ln0_rx_data_o with a delay of 3 cycles. The user can know whether q0_ln0_rx_valid_o is valid by q0_ln0_rx_data_o. When q0_ln0_rx_valid_o is 1, q0_ln0_rx_data_o is valid. When q0_ln0_rx_valid_o is 0, q0_ln0_rx_data_o is invalid.
- q0_ln0_rx_fifo_rdusewd_o indicates how much data in the RX Buffer has not been read.

As shown in the figure, when the RX Buffer read and write clocks are in the same frequency, the user can invert q0_ln0_rx_fifo_aempty_o as q0_ln0_rx_fifo_rden_i. At this point, q0_ln0_rx_fifo_aempty_o will always be 0, and q0_ln0_rx_data_o can be read as a continuous data stream.

q0_ln0_rx_data_o is the RX data output with 88 bits, low first. The meaning represented by each bit is different in different encoding and bit width modes, which can be referred in Table 3-4, Table 3-5, and Table 3-6.

Table 3-4 x8 Bit Width Configuration When 8B10B Encoding Disabled

q0_ln0_rx_data_o bit[n]	width=8	width=16	width=32	width=64
7~0	7~0	7~0	7~0	7~0

q0_ln0_rx_data_o bit[n]	width=8	width=16	width=32	width=64
8	N/A	N/A	N/A	N/A
9	N/A	N/A	N/A	N/A
17~10	N/A	15~8	15~8	15~8
18	N/A	N/A	N/A	N/A
19	N/A	N/A	N/A	N/A
27~20	N/A	N/A	23~16	23~16
28	N/A	N/A	N/A	N/A
29	N/A	N/A	N/A	N/A
37~30	N/A	N/A	31~24	31~24
38	N/A	N/A	N/A	N/A
39	N/A	N/A	N/A	N/A
47~40	N/A	N/A	N/A	39~32
48	N/A	N/A	N/A	N/A
49	N/A	N/A	N/A	N/A
57~50	N/A	N/A	N/A	47~40
58	N/A	N/A	N/A	N/A
59	N/A	N/A	N/A	N/A
67~60	N/A	N/A	N/A	55~48
68	N/A	N/A	N/A	N/A
69	N/A	N/A	N/A	N/A
77~70	N/A	N/A	N/A	63~56
78	N/A	N/A	N/A	N/A
79	N/A	N/A	N/A	N/A
87~80	N/A	N/A	N/A	N/A

Note!

In a certain width mode, only the grayed bits need to be considered.

Table 3-5 x10 Bit Width Configuration When 8B10B Encoding Disabled

q0_ln0_rx_data_o bit[n]	width=10	width=20	width=40	width=80
9~0	9~0	9~0	9~0	9~0
19~10	N/A	19~10	19~10	19~10
29~20	N/A	N/A	29~20	29~20
39~30	N/A	N/A	39~30	39~30
49~40	N/A	N/A	N/A	49~40
59~50	N/A	N/A	N/A	59~50
69~60	N/A	N/A	N/A	69~60
79~70	N/A	N/A	N/A	79~70
87~80	N/A	N/A	N/A	N/A

Note!

In a certain width mode, only the grayed bits need to be considered.

Table 3-6 x10 Bit Width Configuration When 8B10B Encoding Enabled

q0_ln0_rx_data_o bit[n]	width=10	width=20	width=40	width=80
7~0	Code	Code	Code	Code
8	K	K	K	K
9	Disparity Error	Disparity Error	Disparity Error	Disparity Error
80	Decoder Error	Decoder Error	Decoder Error	Decoder Error
17~10	N/A	Code	Code	Code
18	N/A	K	K	K
19	N/A	Disparity Error	Disparity Error	Disparity Error
81	N/A	Decoder Error	Decoder Error	Decoder Error
27~20	N/A	N/A	Code	Code
28	N/A	N/A	K	K
29	N/A	N/A	Disparity Error	Disparity Error
82	N/A	N/A	Decoder Error	Decoder Error
37~30	N/A	N/A	Code	Code
38	N/A	N/A	K	K
39	N/A	N/A	Disparity Error	Disparity Error
83	N/A	N/A	Decoder Error	Decoder Error
47~40	N/A	N/A	N/A	Code
48	N/A	N/A	N/A	K
49	N/A	N/A	N/A	Disparity Error
84	N/A	N/A	N/A	Decoder Error
57~50	N/A	N/A	N/A	Code
58	N/A	N/A	N/A	K
59	N/A	N/A	N/A	Disparity Error
85	N/A	N/A	N/A	Decoder Error
67~60	N/A	N/A	N/A	Code
68	N/A	N/A	N/A	K
69	N/A	N/A	N/A	Disparity Error
86	N/A	N/A	N/A	Decoder Error
77~70	N/A	N/A	N/A	Code
78	N/A	N/A	N/A	K
79	N/A	N/A	N/A	Disparity Error

q0_ln0_rx_data_o bit[n]	width=10	width=20	width=40	width=80
87	N/A	N/A	N/A	Decoder Error

Note!

In a certain width mode, only the grayed bits need to be considered.

3.5.3 Status Interface

The IP provides status interfaces for users to view the channel status in real time, see details in Table 4-1.

3.6 AFE

AFE means analog front end, and the user can configure SerDes analog parameters through the interface.

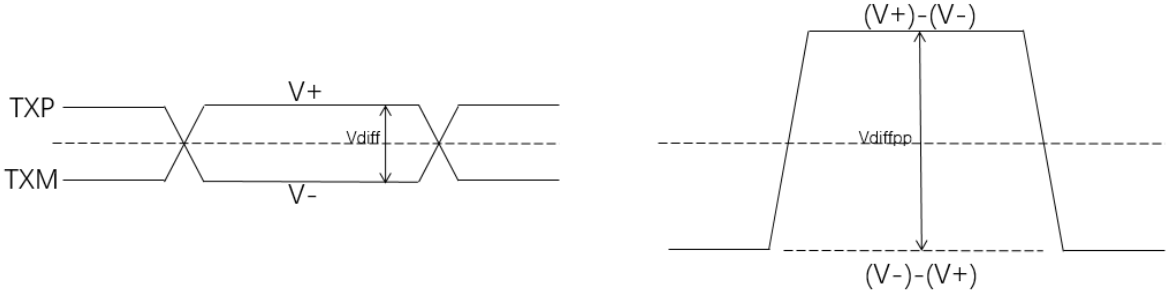
3.6.1 Transmit

On the TX side, the user can configure the differential swing and FFE parameters of the TX signals.

Transmit Differential Swing

As shown in Figure 3-7, the differential voltage of TX signal is Vdiff=(V+)-(V-), and the TX differential signal swing is Vdiffpp=2xVdiff, and the user can configure Vdiffpp through the interface with the range of 180mV~900mV.

Figure 3-7 TX Differential Signal Swing Vdiffpp



TX FFE

FFE means Feed-Forward Equalization (FFE); SerDes supports auto and manual adjustments of FFE coefficients. When the user configures FFE Mode as Auto, SerDes automatically adjusts the FFE coefficient according to the hardware environment, at this time Cm, C0 and C1 configuration is invalid. When the user configures FFE Mode as Manual, the user can manually adjust the 3-tap coefficients and configure the de-weighting of the TX signal.

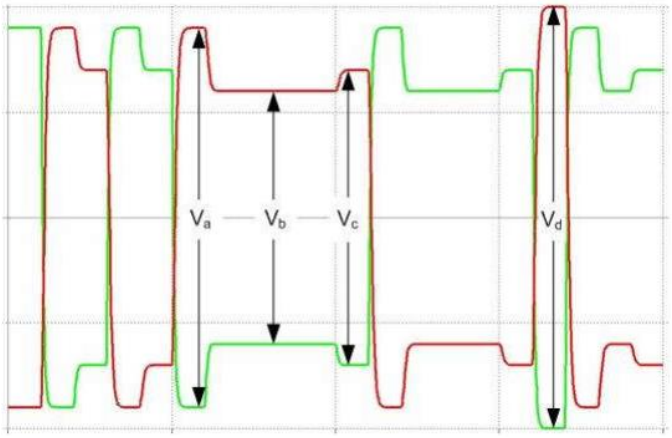
As shown in Figure 3-8, when the user configures the FFE Mode as Manual, the voltage amplitude of Va, Vb and Vc can be adjusted by adjusting the values of Cm, C0 and C1， and the calculation formula is as follows:

Va=Vdiffpp *(-Cm+C0+C1)/40

Vb=Vdiffpp *(-Cm+C0-C1)/40

Vc=Vdiffpp *(Cm+C0-C1)/40

Figure 3-8 FFE TX Voltage Definition



3.6.2 Receive

Receive Differential Signal Threshold

On the RX side, the user can configure the SD Threshold option to adjust the effective voltage threshold of RX signal. When the RX differential signal is greater than SD threshold, SerDes judges that the valid data is received; when the RX differential signal is less than SD threshold, SerDes judges that the valid data is not received, then enters the Electrical Idle state.

Receive Equalization

On the receive side, SerDes has equalization function, and users can adjust the equalizer configuration based on the data rate and channel attenuation to achieve the optimal RX status.

The equalizer in the SerDes can be divided into auto mode and manual mode. When the user configures the Equalization Mode as Auto, the equalizer operates in automatic mode. In this mode, during SerDes RX link establishment, the equalizer automatically adjusts based on the current quality of received data to achieve the optimal status. At this time, the ATT and BOOST options cannot be configured. When the user configures the Equalization Mode as Manual, the equalizer operates in manual mode. In this mode, the user needs to manually configure the ATT and BOOST options to make the equalizer to its best status.

ATT (Attenuator): Adjusts the intermediate frequency attenuation during reception. A smaller value indicates greater attenuation, with a range of 0 to 10.

BOOST (Analog Boost): Adjusts the high-frequency amplification during reception. A larger value indicates greater gain, with a range of 0 to 15.

If users configure the Equalization Mode as Manual, they need to continuously experiment with combinations of ATT and BOOST options to achieve the optimal status for SerDes reception. Therefore, it is

recommended that users prioritize using the Auto mode. If the Auto mode does not adapt itself to the optimal status, users can try the Manual mode.

BIAS

The BIAS option is used to configure the amplification parameters of the SerDes for RX signals. When the RX signal rate is high and the attenuation is significant, the user can change the configuration of this option. The higher the configuration for this option, the stronger the amplification of the signal. This option is based on the QUAD configuration. When the configuration of one Lane is changed, it simultaneously changes the configuration for all Lanes in the Quad where the current Lane is located.

3.7 Dynamic Reconfiguration Function

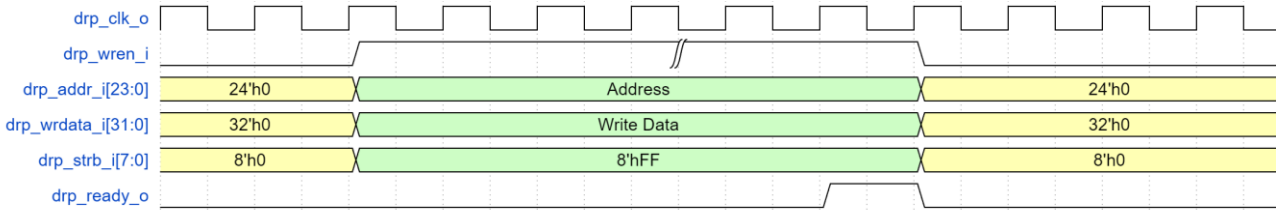
After the initialization configuration of SerDes is completed, users can dynamically configure SerDes registers to adjust SerDes function through Dynamic Reconfiguration Port (DRP) interface. When users select the "DRP Port" in the IP interface, the IP will generate the DRP interface to implement the dynamic reconfiguration function.

3.7.1 Write Operation

Users can write to SerDes registers through DRP write operation interface.

During a write operation, set drp_wren_i to 1. At the same time, write the register address to drp_addr_i; write the data to drp_wrdata_i, and write 0xFF to drp_strb_i. Maintain these signals until drp_ready_o is asserted to 1. When drp_ready_o is 1, it indicates that the write operation is completed. drp_wren_i should be immediately pulled low to terminate the operation. The timing diagram is shown in Figure 3-9.

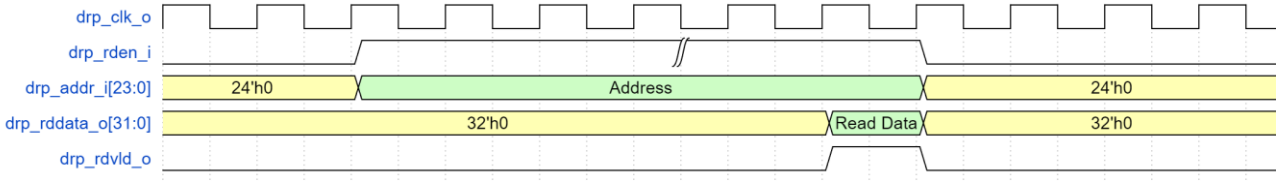
Figure 3-9 DRP Write Operation Timing Diagram



3.7.2 Read Operation

During a read operation, set drp_rden_i to 1. At the same time, write the register address to drp_addr_i[23:0]. Maintain these signals until drp_rdvld_o is asserted to 1. When drp_rdvld_o is detected as 1, the read data is returned to drp_rddata_o. Meanwhile, drp_rden_i should be immediately pulled low to terminate the operation. The timing diagram is shown in Figure 3-10.

Figure 3-10 DRP Read Operation Timing Diagram



3.7.3 Clock Schematic Option

In Gowin SerDes, each Quad has two REFMUXs, including REFMUX0 and REFMUX1. REFMUX can receive input clocks from the reference clock pins of the current Quad or from the reference clock pins of adjacent Quad. REFMUX provides reference clocks for each TX PLL and RX CDR. In applications, users can select the reference clock source and PLL on the interface, and the software automatically calculates the MUX path to complete the clock connection.

Users can view the current clock connection through "View Clock Schematic" function on the SerDes interface, as shown in Figure 3-11.

Figure 3-11 Clock Schematic

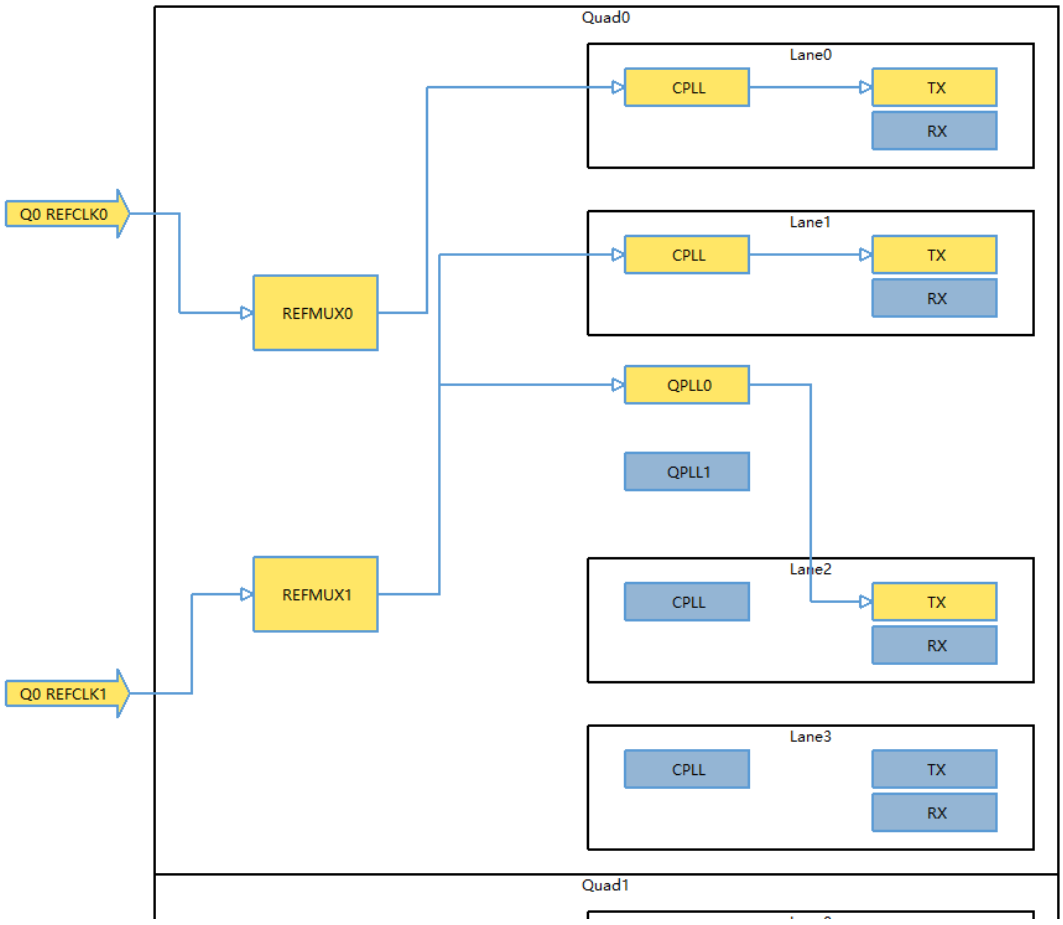


Figure 3-11 shows the clock connection with some of the functions having been configured. Occupied resources are highlighted in yellow, while unoccupied resources are highlighted in blue.

Taking Quad0 Lane0 as an example. This Lane TX uses CPLL as the TX clock source. The reference clock of CPLL comes from REFMUX0, and for REFMUX0, Q0 REFCLK0 is selected as the clock input. The reference clock source of the RX lane is selected automatically, which is not indicated in the above figure for now.

3.7.4 Reconfiguration Option

Users can click the "Reconfiguration" button on Gowin SerDes IP interface to reconfigure, select the dynamic configuration functions and enter the parameters. Finally, click "Export" to export the register addresses and value file (.csr) required for configuring the current dynamic functions.

.csr File

The .csr file is a file containing dynamic configuration register addresses and values exported by the IP. Each line represents a register address + value, in hexadecimal format. The high 24 bits represent the register address, and the low 32 bits represent the register value.

For example, a line, such as 80a00400022322, indicates that 0x80a004 is the register address, and 0x00022322 is the value to be configured at that address. Users need to write the configurations from the .csr file to the SerDes via the DRP interface in the order from top to bottom, in order to achieve the dynamic configuration of the functions.

Channel Option

Check the channel that need to be dynamically configured this time.

Reconfiguration Option

This option includes different functions, such as TX Data Rate, RX Data Rate, etc. Under each function, there is an Enable option. If the user checks the Enable option for a certain function, the exported .csr file will include the dynamic configuration registers for this function. If the user does not check the Enable option for a certain function, the exported .csr file will not include the dynamic configuration registers for this function.

The descriptions of TX Data Rate are shown below.

- TX Data Rate: Used to configure the TX data rate
- TX PLL: Used to select the current TX PLL
- Refclk MUX: Used to select the PLL reference clock source as REFMUX0 or REFMUX1.
- Q0/1 REFMUX0/1 Frequency: Used to input the frequency of the REFMUX reference clock. Only input the frequency of the selected reference clock in the Refclk MUX option; for irrelevant reference clocks, it can be input as 0.
- PMA Width: Used to select the current PMA width

The descriptions of RX Data Rate are shown below.

- RX Data Rate: Used to configure the RX data rate

- Refclk MUX: Used to select the CDR reference clock source as REFMUX0 or REFMUX1.
- Q0/1 REFMUX0/1 Frequency: Used to input the frequency of the REFMUX reference clock. Only input the frequency of the selected reference clock in the Refclk MUX option; for irrelevant reference clocks, it can be input as 0

The description of Loopback is shown below.

- Mode: Used to select loopback mode

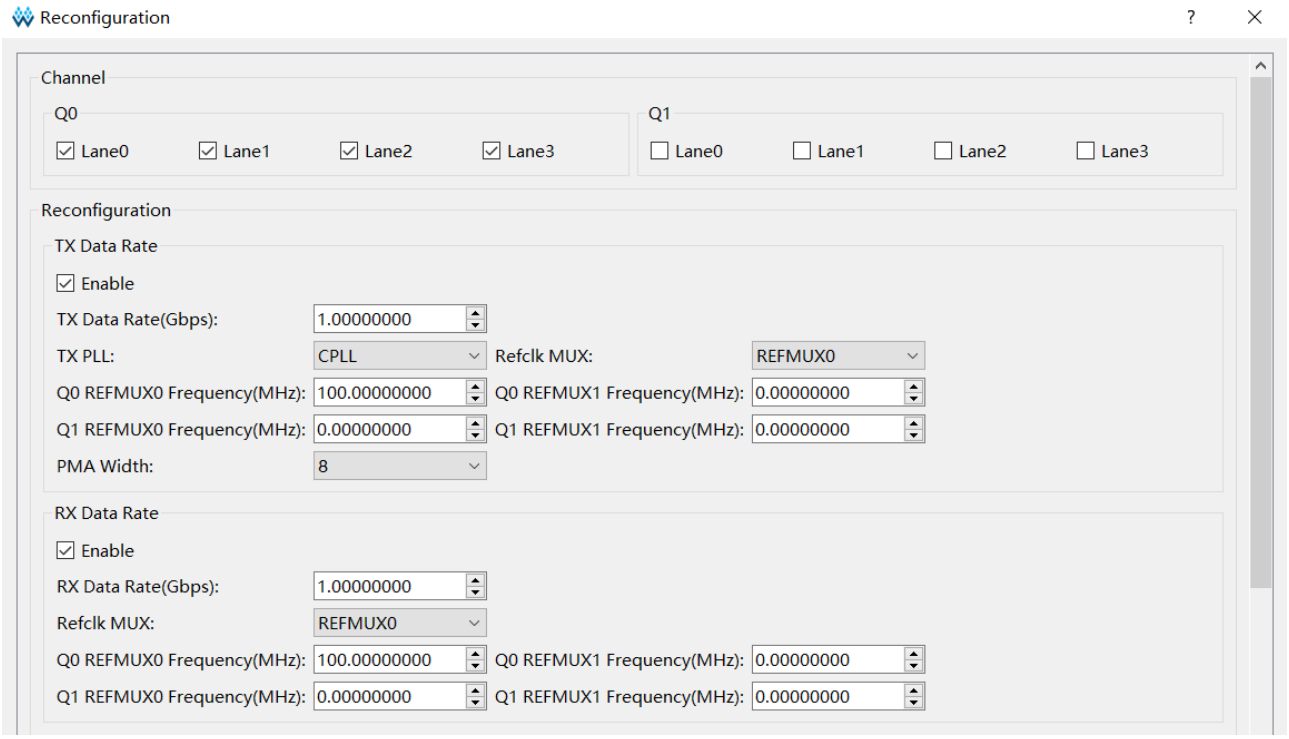
The descriptions of TX AFE are shown below.

- Mode: Used to select Auto or Manual
- TX Swing Level: Used to configure TX Swing
- FFE CM: Used to configure CM parameter, and it is valid when Manual mode is selected
- FFE C1: Used to configure C1 parameter, and it is valid when Manual mode is selected

For example, the dynamic configuration is as shown in Figure 3-12.

- The TX and RX data rate of Q0 Lane0/1/2/3 is 1Gbps
- All reference clocks come from REFMUX0
- The frequency of the reference clocks is 100MHz
- CPLL is used to provide reference clock for TX
- PMA Width is set to 8

Figure 3-12 Reconfiguration Option



4 Port List

The detailed port list of Gowin Customized PHY IP is shown in Table 4-1; taking Quad0 Lane0 as an example, for other Lanes, you can modify the serial number.

Table 4-1 I/O List of Gowin Customized PHY IP

Port Name	I/O	Data Width	Description
Clock			
q0_ln0_rx_pcs_clkout_o	output	1	Quad0 Lane0 PCS RX clock output
q0_ln0_rx_clk_i	input	1	Quad0 Lane0 RX Buffer read clock, which can be directly connected to q0_ln0_rx_pcs_clkout_o, so that the RX Buffer read and write clocks are in the same frequency
q0_ln0_tx_pcs_clkout_o	output	1	Quad0 Lane0 PCS TX clock output
q0_ln0_tx_clk_i	input	1	Quad0 Lane0 TX Buffer write clock, which can be directly connected to q0_ln0_tx_pcs_clkout_o, so that the TX Buffer read and write clocks are in the same frequency
q0_ln0_cc_clk_i	input	1	When User is selected for Clock Source option on RX Clock Correction page, the user needs to input the clock through this port as the destination clock source for the adjustment clock of RX Clock Correction module
Reset			
q0_ln0_pma_rstn_i	input	1	PMA reset input, active-low
q0_ln0_pcs_rx_rst_i	input	1	PCS reset input in RX direction, active-high
q0_ln0_pcs_tx_rst_i	input	1	PCS reset input in TX direction, active-high
RX Data Interface			
q0_ln0_rx_data_o	output	88	Quad0 Lane0 RX Buffer read data, synchronized with q0_ln0_rx_clk_i , valid when q0_ln0_rx_valid_o is 1
q0_ln0_rx_fifo_rden_i	input	1	Quad0 Lane0 read enable, synchronized with q0_ln0_rx_clk_i 1: Read valid

Port Name	I/O	Data Width	Description
			0: Read invalid
q0_ln0_rx_fifo_rdusewd_o	output	5	Remaining data indicator for Quad0 Lane0 RX Buffer
q0_ln0_rx_fifo_aempty_o	output	1	Quad0 Lane0 RX Buffer almost empty indicator 1: RX Buffer almost empty 0: RX Buffer non-almost empty
q0_ln0_rx_fifo_empty_o	output	1	Quad0 Lane0 RX Buffer empty indicator 1: RX Buffer empty 0: RX Buffer non-empty
q0_ln0_rx_valid_o	output	1	Quad0 Lane0 RX Buffer read data valid indicator, indicating whether q0_ln0_rx_data_o is valid. 1: Valid 0: Invalid
TX Data Interface			
q0_ln0_tx_data_i	input	80	Quad0 Lane0 TX Buffer write data, synchronized with q0_ln0_tx_clk_i; when q0_ln0_tx_fifo_wren_i is 1, write TX Buffer
q0_ln0_tx_fifo_wren_i	input	1	Quad0 Lane0 write enable, synchronized with q0_ln0_tx_clk_i 1: Write valid 0: Write invalid
q0_ln0_tx_fifo_wrusewd_o	output	5	Remaining data indicator for Quad0 Lane0 TX Buffer
q0_ln0_tx_fifo_afull_o	output	1	Quad0 Lane0 TX Buffer almost full indicator 1: TX Buffer almost full 0: TX Buffer non-almost full
q0_ln0_tx_fifo_full_o	output	1	Quad0 Lane0 TX Buffer full indicator 1: TX Buffer full 0: TX Buffer non-full
Control Interface			
q0_ln0_cb_start_i	input	1	This port is active when IP enables RX Channel Bonding. When the user pulls up this pin, the Channel Bonding module inside SerDes starts aligning data. The user needs to wait until the word_align_link_o of the selected channels are all 1 before simultaneously pulling up this pin of the selected channel.
Status Interface			
q0_ln0_signal_detect_o	output	1	RX differential signal status indicator 1: Valid signal input is detected 0: No valid signal input is detected and RX is in Electrical Idle.
q0_ln0_rx_cdr_lock_o	output	1	RX CDR lock indicator

Port Name	I/O	Data Width	Description
			1: CDR locked 0: CDR unlocked
q0_ln0_k_lock_o	output	1	Pre-lock indicator for RX word align module 1: Word align module in pre-lock status 0: Word align module not in pre-locked status
q0_ln0_word_align_link_o	output	1	Lock indicator for RX word align module 1: Word align module in lock status 0: Word align module not in lock status
q0_ln0_pll_lock_o	output	1	TX PLL lock indicator 1: TX PLL locked 0: TX PLL unlocked
q0_ln0_ready_o	output	1	TX channel status indicator 1: Ready 0: Not ready
Dynamic Configuration Interface			
drp_clk_o	output	1	DRP interface clock
drp_addr_i	input	24	DRP operation address, synchronized with drp_clk_o
drp_wren_i	input	1	DRP write operation enable, synchronized with drp_clk_o 1: Write operation 0: No operation
drp_wrdata_i	input	32	DRP write data, synchronized with drp_clk_o
drp_strb_i	input	8	DRP write operation enable signal, active-high, synchronized with drp_clk_o. All bits of this signal need to be set to 1 during write operation.
drp_ready_o	output	1	DRP write operation completion indicator, synchronized with drp_clk_o 1: Completed 0: Not completed
drp_rden_i	input	1	DRP read operation enable, synchronized with drp_clk_o 1: Read operation 0: No operation
drp_rdvld_o	output	1	DRP read operation data valid indicator, synchronized with drp_clk_o 1: Returned data valid 0: No valid data returned
drp_rddata_o	output	32	DRP read data, synchronized with drp_clk_o
drp_resp_o	output	1	Reserved

5 Interface Configuration

You can call and configure Gowin Customized IP using the IP core generator tool in the IDE.

1. Open SerDes IP

After creating the project, click the "Tools" tab in the upper left interface, click "IP Core Generator" from the drop-down list to open Gowin IP Core Generator, then double-click to open "Serdes IP".

2. Open Customized IP Core

After opening SerDes IP, find "Customized" in the "Protocol" drop-down list and click "Create" to open Customized IP protocol configuration interface.

3. Configure Customized IP

The Customized IP configuration interface is shown in Figure 5-1, Figure 5-2, Figure 5-3, Figure 5-4, and Figure 5-5, including "Channel, Line Rate, Refclk Selection", "Data Width, Encoding, RX Word Alignment", "Channel Bonding", "RX Clock Correction" and "AFE". You can configure Customized IP parameters on these option pages. See Table 5-1 for the descriptions of the parameters.

Figure 5-1 Channel, Line Rate, Refclk Selection

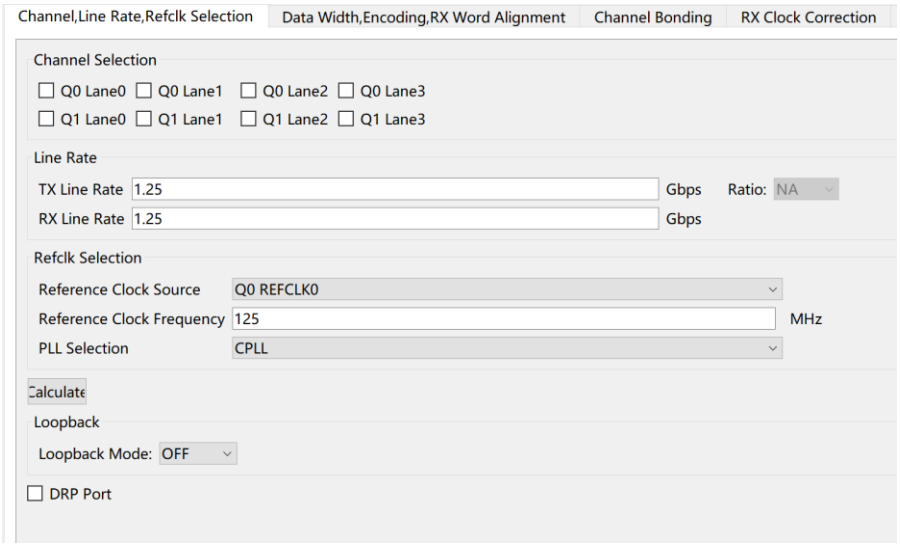


Figure 5-2 Data Width, Encoding, RX Word Alignment

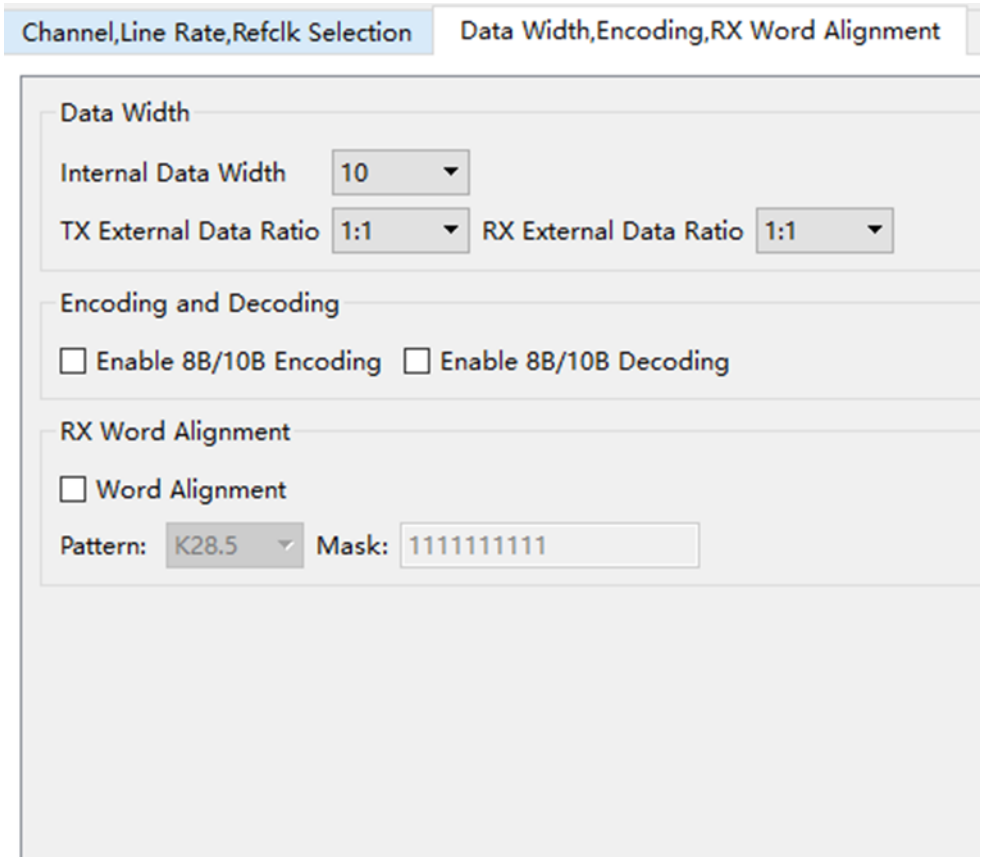


Figure 5-3 Channel Bonding

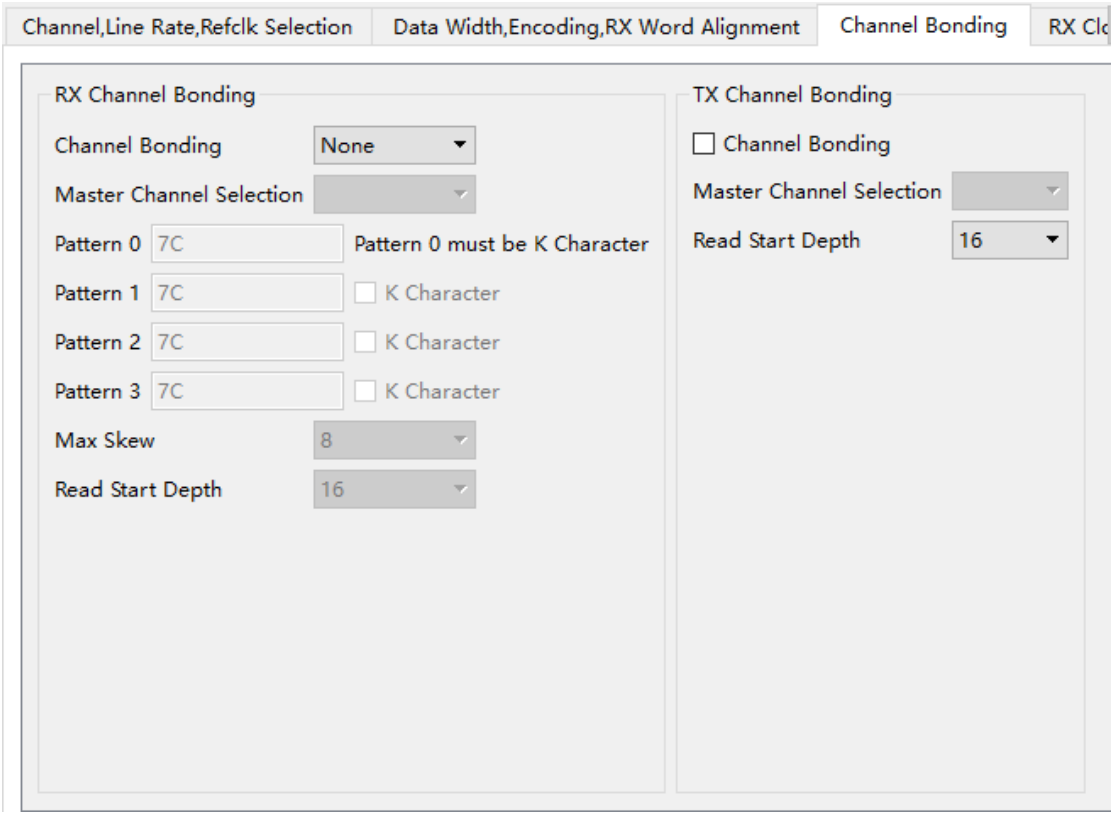


Figure 5-4 RX Clock Correction

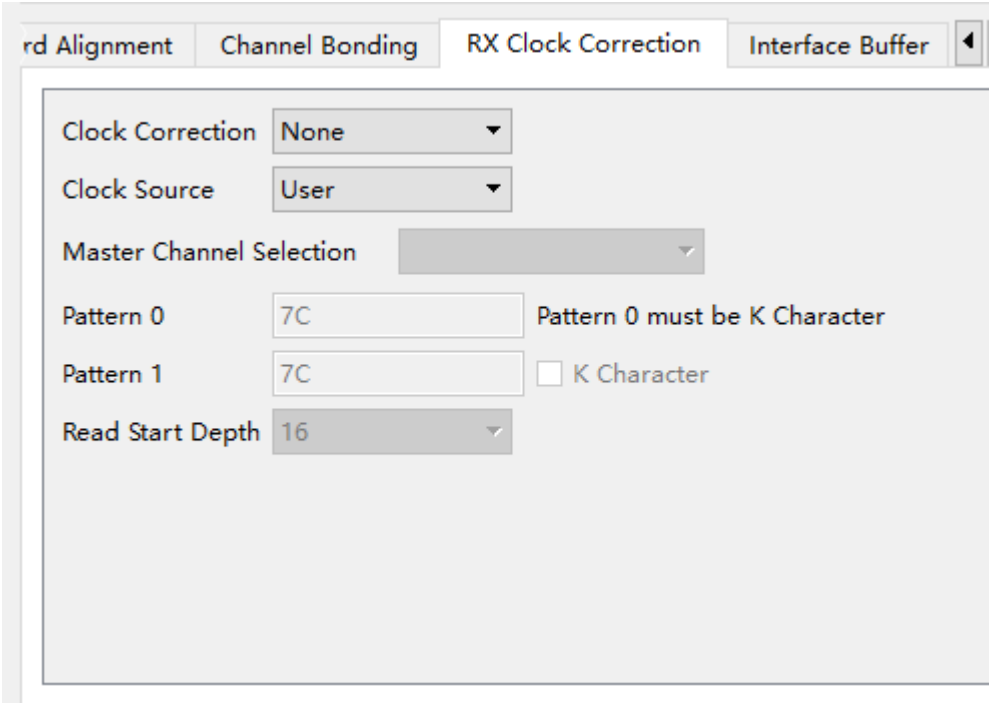
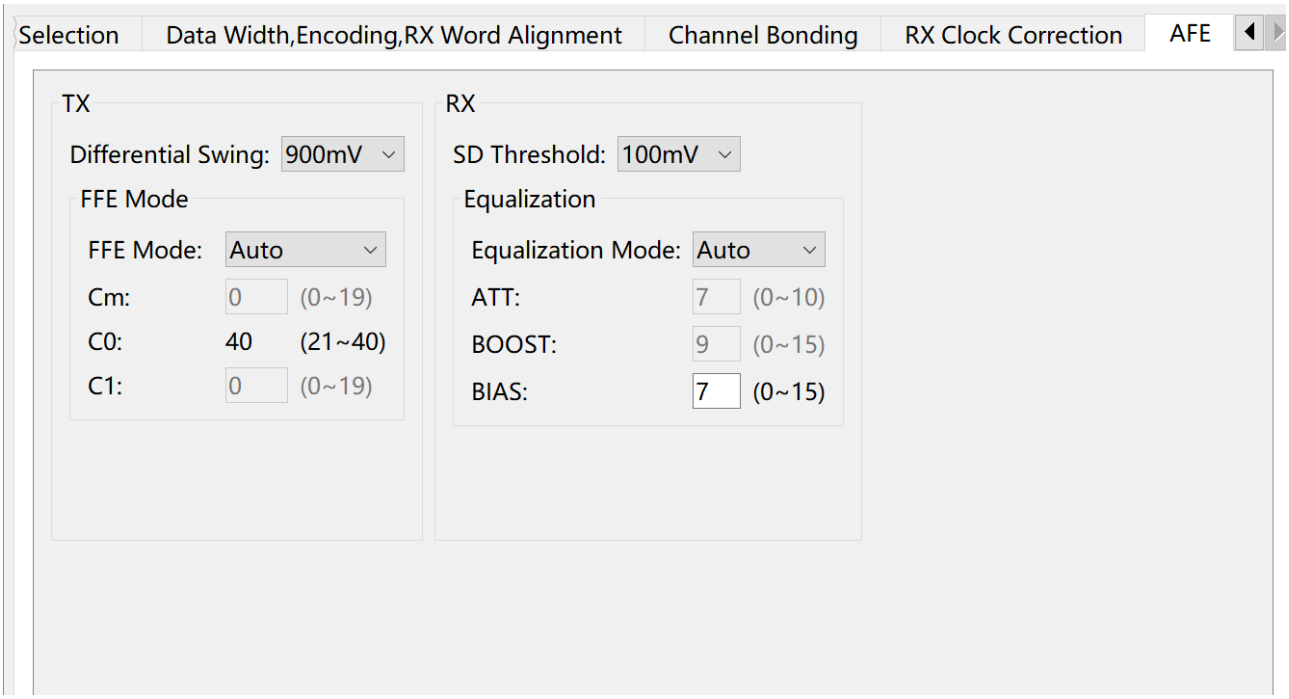


Figure 5-5 AFE



After configuring Customized IP parameters, click the "OK" button to generate the configuration associated with Customized IP.

4. Complete SerDes IP configuration

On the SerDes IP interface, the user completes the configuration of all protocols and then clicks "OK" button to complete the generation of the SerDes IP. In the SerDes IP top-level file, the signals used by this IP have

the same prefix as the Module Name of the Customized PHY IP interface.

Table 5-1 Customized IP Parameters

Name	Range	Description
Channel, Line Rate, Refclk Selection		
Channel Selection	Q0 Lane0 Q0 Lane1 Q0 Lane2 Q0 Lane3 Q1 Lane0 Q1 Lane1 Q1 Lane2 Q1 Lane3	The user can check any one or more Lanes; If the user checks one Lane, all subsequent configurations are for this Lane; if the user checks more Lanes, all subsequent configurations are for all the checked Lanes.
TX Line Rate	0.025Gbps~12.5Gbps	Transmit data
Ratio	NA 5x 10x 20x 40x	Configure the TX data rate ratio when TX Line Rate < 1Gbps. See TX Line Rate < 1Gbps for details
Configure TX line rate	1Gbps~12.5Gbps	Configure RX line rate
Reference Clock Source	Q0 REFCLK0 Q0 REFCLK1 Q1 REFCLK0 Q1 REFCLK1	Select reference clock source
Reference Clock Frequency	50~800MHz	Configure reference clock source
PLL Selection	CPLL QPLL0 QPLL1	Select PLL **Note! CPLL is recommended for a single lane; QPLL is required for multiple lanes.**
Loopback Mode	OFF LB_NES LB_FES LB_ENC	OFF: No Loopback, normal operating mode LB_NES: Loopback Near-End Side LB_FES: Loopback Far-End Side LB_ENC: Loopback Encoder
Calculate	-	Check if the reference clock frequency matches the data rate; if it matches, "Succeed" will pop up.
DRP Port	Checked/Unchecked	Checked: Enable DRP Unchecked: Disable DRP
Data Width, Encoding, RX Word Alignment		
Internal Data Width	8 10 16 20	SerDes internal data bit width
TX External Data Ratio	1:1 1:2 1:4	TX interface data width ratio TX interface data width ratio = Internal Data Width* TX External Data Ratio
RX External Data Ratio	1:1	RX interface data width ratio RX interface data width ratio = Internal Data

Name	Range	Description
	1:2 1:4	Width* RX External Data Ratio
Enable 8B/10B Encoding	Checked/Unchecked	Checked: Enable TX 8B/10B encoding Unchecked: Disable TX 8B/10B encoding
Enable 8B/10B Decoding	Checked/Unchecked	Checked: Enable RX 8B/10B decoding Unchecked: Disable RX 8B/10B decoding
Word Alignment	Checked/Unchecked	Checked: Enable RX Word Alignment Unchecked: Disable RX Word Alignment
Pattern	Valid K character such as K28.0, K28.5, etc.	Select Word Alignment type
Mask	0000000000~ 1111111111	Pattern mask; when word aligning, comparing bits where the mask is 1 and not comparing bits where the mask is 0
RX Channel Bonding		
Channel Bonding	None One Word Two Words Four Words	RX Channel Bonding enable: None: Disable Channel Bonding One Word: Enable Channel Bonding for 1 Word Two Words: Enable Channel Bonding for 2 Words Four Words: Enable Channel Bonding for 4 Words
Master Channel Selection	Lane selected	Select master channel for RX Channel Bonding
Pattern0	0x00~0xFF	The first alignment character must be K character
Pattern1/2/3	0x00~0xFF	For the 2nd/3rd/4th alignment character, it can be K character or not
K Character	Checked Unchecked	Configure whether the alignment character is K character or not Checked: K character Unchecked: Data
Max Skew	0~31	Configure the maximum skew for inter-RX channels
Read Start Depth	0~31	After bonding the data, configure the read start depth of the module
Channel Bonding		
Channel Bonding	Checked/Unchecked	TX Channel Bonding enable Checked: Enable TX Channel Bonding Unchecked: Disable TX Channel Bonding
Master Channel Selection	Lane selected	Select master channel for TX Channel Bonding
Read Start Depth	0~31	After bonding the data, configure the read start depth of TX Buffer
RX Clock Correction		
Clock Correction	None One Word Two Words	RX Clock Correction enable: None: Disable Clock Correction One Word: Enable Clock Correction for 1 Word

Name	Range	Description
		Two Words: Enable Clock Correction for 2 Words
Clock Source	User Quad TX	Select the destination clock source that needs to be synchronized with RX Clock Correction User: Set Clock Source as Fabric input clock (e.g. q0_ln0_cc_clk_i) TX: Set the Clock Source to TX clock Quad: Reserved
Master Channel Selection	Lane selected	Select master channel for RX Clock Correction
Pattern0	0x00~0xFF	The first adjustment character must be K character
Pattern1	0x00~0xFF	For the 2nd adjustment character, it can be K character or not
K Character	Checked Unchecked	Configure whether the adjustment character is K character or not Checked: K character Unchecked: Data
Read Start Depth	0~31	After adjusting data, configure the read start depth of the module
AFE		
Differential Swing	100mV~900mV	Configure TX differential signal swing Vdiffpp, Vdiffpp=2xVdiff
FFE Mode	Auto Manual	Configure TX FFE mode ● Auto: Automatic mode ● Manual: Manual mode
Cm	0~19	Transmit FFE pre-cursor
C0	21~40	Transmit FFE main-cursor
C1	0~19	Transmit FFE post-cursor
SD Threshold	25mV~200mV	Receive differential signal SD threshold
Equalization Mode	Auto Manual	Receive Equalization: ● Auto: Automatic mode ● Manual: Manual mode
ATT	0~10	Adjust the intermediate frequency attenuation during reception. A smaller value indicates greater attenuation.
BOOST	0~15	Adjust the high-frequency amplification during reception. A larger value indicates greater gain.
BIAS	0~15	Configure the amplification parameters of the SerDes for RX signals. A higher value indicates stronger signal amplification.

6 Reference Design

See the Customized PHY reference design for details at Gowinsemi website.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