

Gowin USB 2.0 SoftPHY Device Peripheral Circuit Design Application Note

Overview

This manual describes the schematic and PCB design considerations of Gowin USB 2.0 SoftPHY device peripheral circuit.

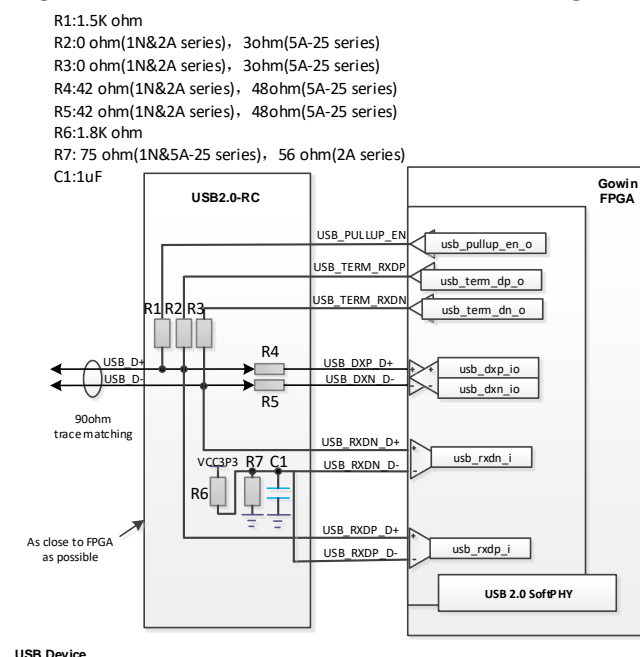
The Gowin USB 2.0 SoftPHY device peripheral circuit is called USB2.0-RC circuit for short in the application note.

Device Selection Considerations

Select GW1N/GW2A series devices with speed grade no lower than C7.

USB2.0-RC Circuit Connection Diagram

Figure 1 USB2.0-RC Circuit Connection Diagram



Note!

- The resistance accuracy is 1% and the capacitance accuracy is $\pm 20\%$.
- The package size of resistance and capacitance is recommended to be 0402.

Schematic Considerations

1. The differential pair of USB2.0-RC circuit need to place on the TRUE LVDS pins of FPGA, including USB_DXP_D+/ USB_DXP_D-, USB_RXDP_D+/ USB_RXDP_D-, USB_RXDN_D+/ USB_RXDN_D-.
2. All signals related to the USB interface on the FPGA are recommended to be placed in a bank with the best adjacent allocation. And the supply voltage of the I/O bank is 3.3V.
3. The differential pin used by USB_D+/D- requires the adjacent differential pair to be present and unused. Taking the USB_D+/D- signal of USB 2.0 as an example, if IOB12A&IOB12B pin is used, then IOB11A&IOB11B is required to be present and unused; if IOB15A&IOB15B is used, IOB14A&IOB14B is required to be present and unused.

Note!

Constraints are required for the pin whose name has the smaller number of digits.

PCB Considerations

1. The resistors and capacitors of the USB2.0-RC circuit are required to be placed as close to the FPGA as possible.
2. The differential pair impedance of USB2.0-RC circuit is 90Ω.
3. USB2.0 reference voltage signal (USB_RXDP_D-) routing is required to be placed as close to USB_RXDP_D+ signal routing as possible.
4. USB2.0 reference voltage signal (USB_RXDN_D-) routing is required to be placed as close to USB_RXDN_D+ signal routing as possible. The differential pairs in USB2.0-RC circuit do not place via holes as far as possible. If the differential pair places via holes in the routing process, 2~4 ground holes are required to be placed next to the via holes to reduce the return current path.
5. Differential pairs are required to have a complete reference ground plane.
6. The pads directly under the differential pairs are required to cut out to adapt to the signal integrity issues brought about by impedance changes.
7. The transmission lines of one differential pair are required to be as long as possible, within 10mil error control.

PCB Design Reference

For USB2.0-RC, see the [schematic of DK_USB2.0_GW2AR-LV18QN88PC8I7_GW1NSR-LV4CMG64PC7I6_V3.0](#).

Support and Feedback

Gowin Semiconductor provides customers with comprehensive technical support. If you have any questions, comments, or suggestions, please feel free to contact us directly by the following ways.

Website: www.gowinsemi.com

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Revision History

Date	Version	Description
10/14/2022	1.0E	Initial version published.
04/11/2024	1.0.1E	The resistance value for GW5A-25 devices in “Figure 1 USB2.0-RC Circuit Connection Diagram” updated.

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