

1. Description

1.1. Project

Project Name	Tim_Test
Board Name	custom
Generated with:	STM32CubeMX 6.11.0
Date	03/22/2024

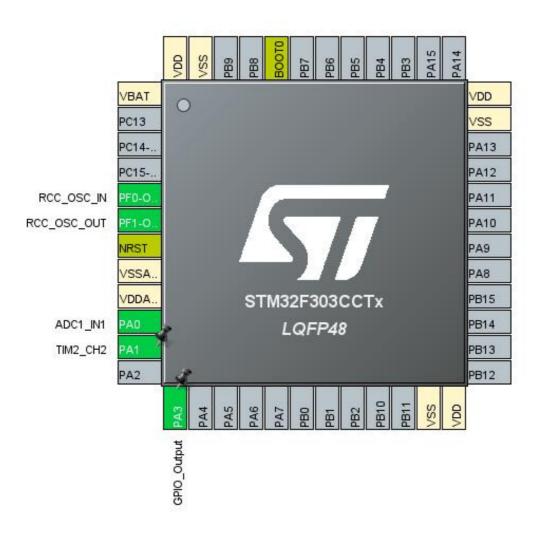
1.2. MCU

MCU Series	STM32F3
MCU Line	STM32F303
MCU name	STM32F303CCTx
MCU Package	LQFP48
MCU Pin number	48

1.3. Core(s) information

Core(s)	Arm Cortex-M4	

2. Pinout Configuration

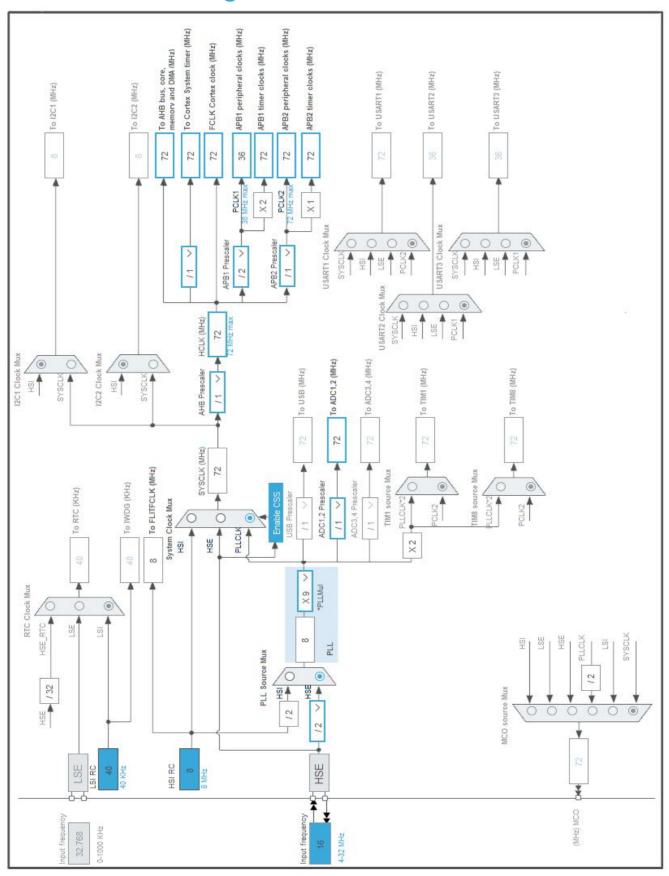


3. Pins Configuration

Pin Number LQFP48	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
1	VBAT	Power		
5	PF0-OSC_IN	I/O	RCC_OSC_IN	
6	PF1-OSC_OUT	I/O	RCC_OSC_OUT	
7	NRST	Reset		
8	VSSA/VREF-	Power		
9	VDDA/VREF+	Power		
10	PA0	I/O	ADC1_IN1	
11	PA1	I/O	TIM2_CH2	
13	PA3 *	I/O	GPIO_Output	
23	VSS	Power		
24	VDD	Power		
35	VSS	Power		
36	VDD	Power		
44	воото	Boot		
47	VSS	Power		
48	VDD	Power		

^{*} The pin is affected with an I/O function

4. Clock Tree Configuration



5. Software Project

5.1. Project Settings

Name	Value	
Project Name	Tim_Test	
Project Folder	D:\git\STM32_Test\Tim_Test	
Toolchain / IDE	STM32CubeIDE	
Firmware Package Name and Version	STM32Cube FW_F3 V1.11.4	
Application Structure	Advanced	
Generate Under Root	Yes	
Do not generate the main()	No	
Minimum Heap Size	0x200	
Minimum Stack Size	0x400	

5.2. Code Generation Settings

Name	Value
STM32Cube MCU packages and embedded software	Copy only the necessary library files
Generate peripheral initialization as a pair of '.c/.h' files	Yes
Backup previously generated files when re-generating	No
Keep User Code when re-generating	Yes
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power	No
consumption)	
Enable Full Assert	No

5.3. Advanced Settings - Generated Function Calls

Rank	Function Name	Peripheral Instance Name
1	SystemClock_Config	RCC
2	MX_GPIO_Init	GPIO
3	MX_DMA_Init	DMA
4	MX_TIM2_Init	TIM2
5	MX_ADC1_Init	ADC1
6	MX_TIM3_Init	TIM3

1. Power Consumption Calculator report

1.1. Microcontroller Selection

Series	STM32F3
Line	STM32F303
MCU	STM32F303CCTx
Datasheet	DS9118_Rev13

1.2. Parameter Selection

Temperature	25
Vdd	3.6

1.3. Battery Selection

Battery	Li-SOCL2(A3400)
Capacity	3400.0 mAh
Self Discharge	0.08 %/month
Nominal Voltage	3.6 V
Max Cont Current	100.0 mA
Max Pulse Current	200.0 mA
Cells in series	1
Cells in parallel	1

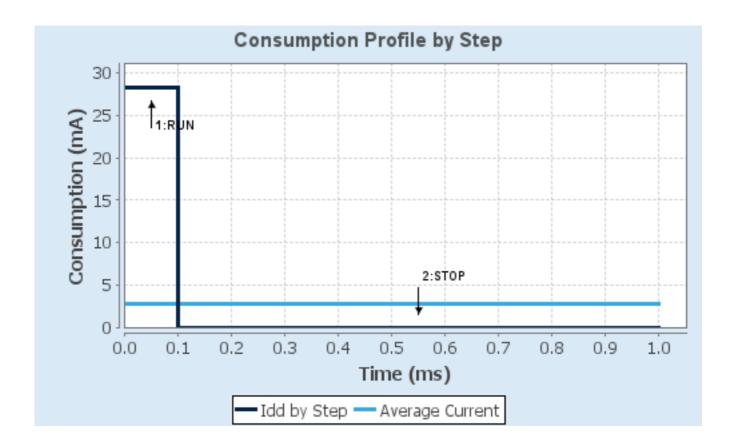
1.4. Sequence

Step	Step1	Step2
Mode	RUN	STOP
Vdd	3.6	3.6
Voltage Source	Battery	Battery
Range	No Scale	No Scale
Fetch Type	FLASH	n/a
CPU Frequency	72 MHz	0 Hz
Clock Configuration	HSE PLL	Regulator LP
Clock Source Frequency	8 MHz	0 Hz
Peripherals		
Additional Cons.	0 mA	0 mA
Average Current	28.24 mA	10.85 μΑ
Duration	0.1 ms	0.9 ms
DMIPS	63.0	0.0
Ta Max	99.41	105
Category	In DS Table	In DS Table

1.5. Results

Sequence Time	1 ms	Average Current	2.83 mA
Battery Life	1 month, 19 days,	Average DMIPS	63.0 DMIPS
	12 hours		

1.6. Chart



2. Peripherals and Middlewares Configuration

2.1. ADC1

IN1: IN1 Single-ended

2.1.1. Parameter Settings:

ADCs_Common_Settings:

Mode Independent mode

ADC_Settings:

Clock Prescaler ADC Asynchronous clock mode

Resolution ADC 12-bit resolution

Data Alignment Right alignment

Scan Conversion Mode Disabled
Continuous Conversion Mode Disabled
Discontinuous Conversion Mode Disabled

DMA Continuous Requests Enabled *

End Of Conversion Selection End of single conversion

Overrun behaviour Overrun data overwritten

Low Power Auto Wait Disabled

ADC Regular ConversionMode:

Enable Regular Conversions Enable

Number Of Conversion 1

External Trigger Conversion Source Timer 3 Trigger Out event *

External Trigger Conversion Edge Trigger detection on the rising edge

SequencerNbRanks 1
Rank 1

Channel Channel 1
Sampling Time 1.5 Cycles
Offset Number No offset
Offset 0

ADC_Injected_ConversionMode:

Enable Injected Conversions Enable
Number Of Conversions 0

Analog Watchdog 1:

Enable Analog WatchDog1 Mode false

Analog Watchdog 2:

Enable Analog WatchDog2 Mode false

Analog Watchdog 3:

Enable Analog WatchDog3 Mode false

2.2. RCC

High Speed Clock (HSE): Crystal/Ceramic Resonator

2.2.1. Parameter Settings:

System Parameters:

VDD voltage (V) 3.3
Prefetch Buffer Enabled

Flash Latency(WS) 2 WS (3 CPU cycle)

RCC Parameters:

HSI Calibration Value 16
HSE Startup Timout Value (ms) 100
LSE Startup Timout Value (ms) 5000

2.3. TIM2

Clock Source: Internal Clock
Channel2: PWM Generation CH2

2.3.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value) 0

Counter Mode Up

Counter Period (AutoReload Register - 32 bits value) 0 **

**The Process of the Period (AutoReload Register - 32 bits value) 0 **

**The Prescaler (PSC - 16 bits value) 0 **

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**The Prescaler (PSC - 16 bits value) 0 **

**The Prescaler

Internal Clock Division (CKD)

No Division

auto-reload preload

Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit) Disable (Trigger input effect not delayed)

Trigger Event Selection TRGO Reset (UG bit from TIMx_EGR)

Clear Input:

Clear Input Source Disable

PWM Generation Channel 2:

Mode PWM mode 1

Pulse (32 bits value) 0

Output compare preload Enable

Fast Mode Disable

CH Polarity High

2.4. TIM3

Clock Source : Internal Clock

2.4.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value) 0 Counter Mode Up Counter Period (AutoReload Register - 16 bits value) $0 \star$

Internal Clock Division (CKD)

auto-reload preload

Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit) Disable (Trigger input effect not delayed)

^{*} User modified value

3. System Configuration

3.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull	Max	User Label
				down	Speed	
ADC1	PA0	ADC1_IN1	Analog mode	No pull-up and no pull-down	n/a	
RCC	PF0-OSC_IN	RCC_OSC_IN	n/a	n/a	n/a	
	PF1-	RCC_OSC_OUT	n/a	n/a	n/a	
	OSC_OUT					
TIM2	PA1	TIM2_CH2	Alternate Function Push Pull	No pull-up and no pull-down	High *	
GPIO	PA3	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	

3.2. DMA configuration

DMA request	Stream	Direction	Priority
ADC1	DMA1_Channel1	Peripheral To Memory	Low

ADC1: DMA1_Channel1 DMA request Settings:

Mode: Circular *

Peripheral Increment: Disable

Memory Increment: Enable *

Peripheral Data Width: Half Word

Memory Data Width: Half Word

3.3. NVIC configuration

3.3.1. NVIC

Interrupt Table	Enable	Preenmption Priority	SubPriority	
Non maskable interrupt	true	0	0	
Hard fault interrupt	true	0	0	
Memory management fault	true	0	0	
Pre-fetch fault, memory access fault	true	0	0	
Undefined instruction or illegal state	true	0	0	
System service call via SWI instruction	true	0	0	
Debug monitor	true	0	0	
Pendable request for system service	true	0	0	
System tick timer	true	15	0	
DMA1 channel1 global interrupt	true	0	0	
ADC1 and ADC2 interrupts	true	0	0	
PVD interrupt through EXTI line16	unused			
Flash global interrupt	unused			
RCC global interrupt	unused			
TIM2 global interrupt	unused			
TIM3 global interrupt	unused			
Floating point unit interrupt	unused			

3.3.2. NVIC Code generation

Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
Non maskable interrupt	false	true	false
Hard fault interrupt	false	true	false
Memory management fault	false	true	false
Pre-fetch fault, memory access fault	false	true	false
Undefined instruction or illegal state	false	true	false
System service call via SWI instruction	false	true	false
Debug monitor	false	true	false
Pendable request for system service	false	true	false
System tick timer	false	true	true
DMA1 channel1 global interrupt	false	true	true
ADC1 and ADC2 interrupts	false	true	true

* User modified value

4. System Views

4.1. Category view

4.1.1. Current

5. Docs & Resources

Type Link

BSDL files https://www.st.com/resource/en/bsdl_model/stm32f3_bsdl.zip

System View https://www.st.com/resource/en/svd/stm32f3-svd.zip

Description

Presentations https://www.st.com/resource/en/product_presentation/stm32-

stm8_embedded_software_solutions.pdf

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tools_portfolio.pdf

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