EN2110 – Electronics III

Circuit Design & Simulation Project

Relevant Files Can be Found at: Github/Group 17

GROUP NO: 17

Name	Index no.
D.S.P.A. NIWARTHANA	180433E
T.D.R.V PERERA	180468N
P.S.M.R. DHAMMIKA	180134M

Contribution of Each Member

Index no.	Contribution
180433E	Circuit 1
180468N	Circuit 2 - 1st & 2nd parts
180134M	Circuit 2 – 3rd part

I. Circuit1: 3 – Stage Ring Oscillator

A ring oscillator is a circuit which consists of an odd number of inverters, called stages, where the output of each stage of the oscillator is fed to the input of the next stage. Additionally, the output of the final stage is provided to its input as feedback, creating a loop (a ring), which in turn causes the circuit to produce a periodic output. Here our task is to design an oscillator with 3 such stages.

1. Inverters

The basic building block of a stage is an inverter (In digital electronic terms; a NOT gate). This consists of a complimentary pair of PMOS and NMOS transistors which acts as *pull-up and pull-down networks* respectively. The expected behavior of such a CMOS inverter is as shown in truth Table 1 (Note that the voltage values can be swapped according to preference).

Table 1: Truth Table for an Inverter

In	Out	V_{in}	V_{out}
0	1	V_L	V_H
1	0	V_H	V_L

Though this can be achieved using the said MOSFETs *as switches*, these components possess parasitic elements due to their structure, which introduces a time delay to the output in practical scenarios.

As we are aware, parasitic elements are the *unintended characteristics of an electronic component* which is present in non-ideal situations, in our case unideal capacitances or resistances in MOSFETs that are being used as switches. The source and drain of a NMOS or a PMOS are insulated from the gate by an oxide film. With substrate intervening, a PN junction is formed between the source and the drain, and a parasitic body diode is said to be present. Here the related source-drain capacitance is said to be the the junction capacitance of the said parasitic body diode. Similarly, there are several capacitances (see Table 2) involved with a MOSFET values of which can be identified in their respective datasheets and Spice models available in LTspice.

Table 2: Capacitances related to MOSFETs [2]

Symbol	Expression	Meaning
C_{gs}	C_{gs}	Gate-source capacitance
C_{gd}	C_{gd}	Gate-drain Capacitance
C_{iss}	$C_{gs} + C_{gd}$	Input Capacitance
C_{oss}	$C_{ds} + C_{gd}$	Output Capacitance
C_{rss}	C_{gd}	Feedback Capacitance

The effect of these can be demonstrated by comparing an inverter with near-ideal MOSFETs (Fig. 1) with an inverter with parasitic elements (Fig. 2).

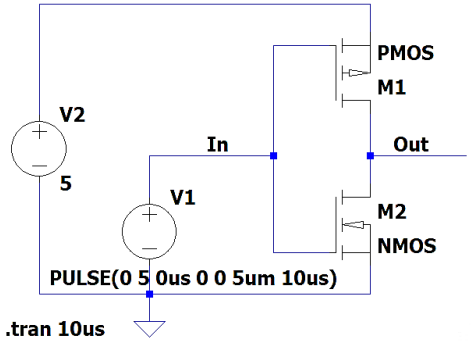

Fig. 1 Inverter Circuit with Near-ideal MOSFETs

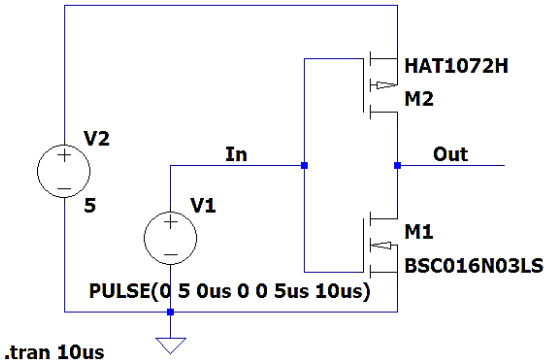

Fig. 2 Inverter Circuit with Parasitic Elements

These two circuits will yield simulation results Fig. 3 and Fig. 4 respectively. It can be observed how with the parasitic effect is in work, as the 'response change' from V_L to V_H or V_H to V_L happens after a slight delay (of about 270ns on average for this setup) as marked in Fig. 4. Another important thing to note is how this increment of parasitic effect

has contributed to increment the delay. Through further simulations, this fact that the gate delay through a MOSFET is proportional to its parasitic effect can be proven clearly. This shows how an inverter can be used in a ring oscillator with a characteristic oscillation frequency utilizing these delays as props to its oscillation.

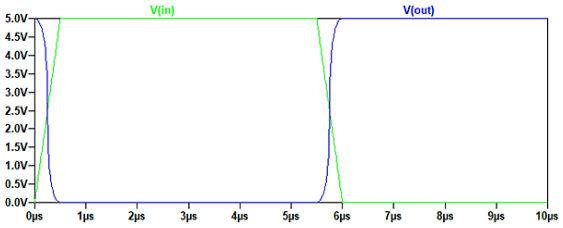

Fig. 3 Simulation of Fig. 1 Circuit (No Delay)

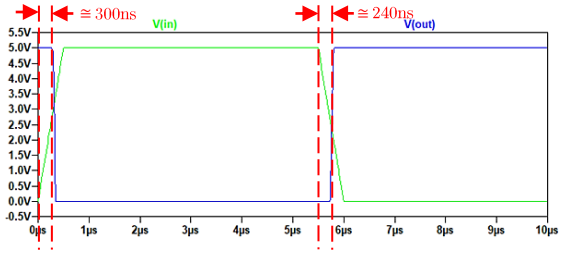

Fig. 4 Simulation of Fig. 2 Circuit (Delay Present)

In the next section, a ring-oscillator is built with 3 such inverters.

2. Ring-Oscillator Circuit

In theory [5], for an oscillator to be functional and stable a mathematical condition named the **Barkhausen stability criterion** should be satisfied. The criterion specifies that,

a. The loop voltage gain should be equal to 1 in absolute magnitude and,
b. The phase shift along the loop should be 0 or an integer multiple of 2π.

Following this criterion, each stage of our ring-oscillator will carry a phase shift of $\frac{\pi}{3}$, while the DC inversion carries a phase shift of π (Total $\frac{\pi}{3}+\frac{\pi}{3}+\frac{\pi}{3}+\pi$). A plausible circuit design with the ability to comply to said conditions is thus designed in the software LTspice as in Fig.5.

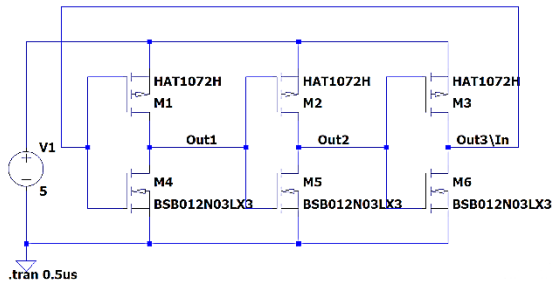

Fig. 5 3-Stage Ring Oscillator Circuit

Running the simulation yields Fig. 6,

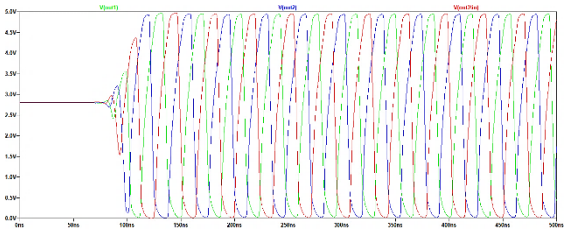

Fig. 6 Simulation Result of 3 Stage Ring Oscillator (Simulation Time: 500ns)

Whilst a closer look at when the oscillation starts can be observed in Fig. 7.

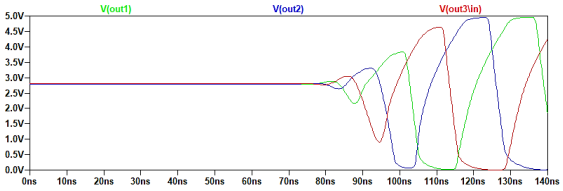

Fig. 7 Simulation Result of 3 Stage Ring Oscillator (Simulation Time: 140ns)

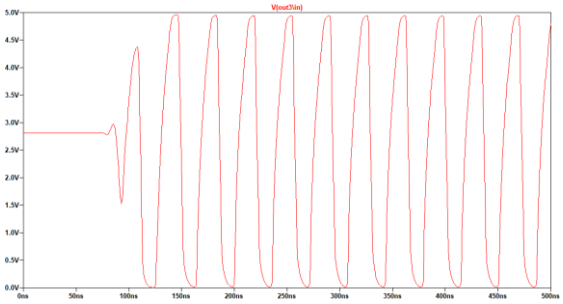

Fig. 8 Voltage Variation at the Output of the 3rd Stage ($V_{in} = V_{out3}$)

Here the wire delays are simulated to be zero (achieved by not placing addition resistances along the wires), as only the parasitic effect of the MOSFETs are of concern. It is also noteworthy that readily available MOSFET spice models are used in the circuit.

By measuring we can get the following figures, which gives us an approximate oscillation frequency of $\frac{1}{54.44ns} \cong 18.36MH_z$.

a. **Time taken to start oscillation:**
   76.51ns.

b. **Oscillation period:**
   Points selected (283.83ns, 4.997V) and (338.27ns, 4.997V)
   Period ≅ 338.27ns - 283.83ns = 54.44ns

It can also be observed that the gain is equal to unity as per the Barkhausen stability criterion.

3. Effect of Parasitic Elements

Let us consider the previously simulated circuit. HAT1072H by Renesas is used as PMOS while BSB012N03LX3 by Infineon is used as NMOS transistors. They possess characteristics shown in Table 3.

Table 3: Characteristics of Selected NMOS and PMOS Transistors

	Characteristic
PMOS	VDMOS(pchan, Rg=3, Rd=1.4m, Rs=1.1m, Vto=-2, Kp=103, lambda=.03, Cgdmax=4.2n, Cgdmin=.5n, Cgs=4.3n, Cjo=3n, Is=310p, Rb=1.8m, ksubthres=.1, mfg=Renesas, Vds=-30, Ron=3.6m, Qg=155n)
NMOS	VDMOS(Rg=0.5, Vto=2.77, Rd=612u, Rs=183u, Rb=383u, Kp=1084, Lambda=0.09, Cgdmin=155p, Cgdmax=2.32n, A=0.6, Cgs=9.61n, Cjo=8.84n, M=0.3, Is=84p, VJ=0.9, N=1.1, TT=3n, ksubthres=.1, mfg=Infineon, Vds=30, Ron=1.2m, Qg=62n)

We can observe the previously discussed parasitic capacitances and various resistances at play. Now to obtain a relationship with the parasitic effects with output characteristics we will observe the relationship with C_{gs} of NMOS with frequencies and delays related to the oscillator. Other parasitic capacitances will follow the same trend for both PMOS and NMOS.

Default values of the model can be changed, or new models can be added by editing the component model shown in Fig. 9. By editing the C_{gs} values several plots could be obtained.

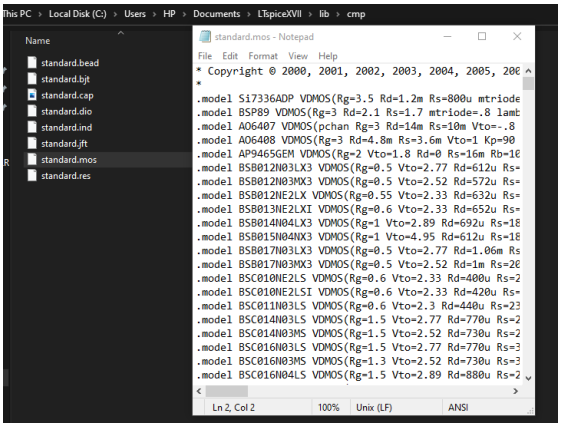

Fig. 9 Changing the Paratmeters of MOSFET Transistors

In Fig. 10 it can be seen that C_{gs} has a near proportional relationship with the time taken for the oscillation to start. It was observed that the initial voltage (2.76V) of every resultant oscillator had almost the same value despite the change in parasitic capacitance.

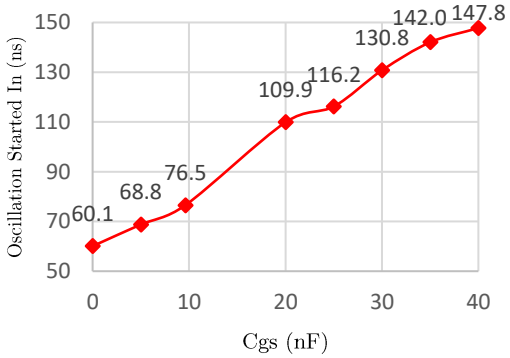

Fig. 10 Trend of time taken for the oscillations to start versus C_{gs}

Similarly, by plotting the calculated frequencies for each capacitance value (see Fig. 11) we can observe that it has a

correlation with the parasitic effect that can be approximated into an inversely proportional curve. To that end, the period should show a proportional change with the increment of C_{gs} which is observed in Fig. 12.

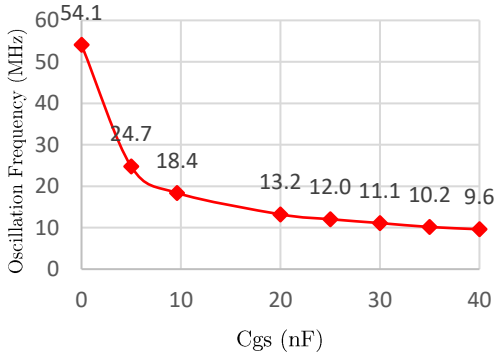

Fig. 11 Trend of oscillation frequency versus C_{gs}

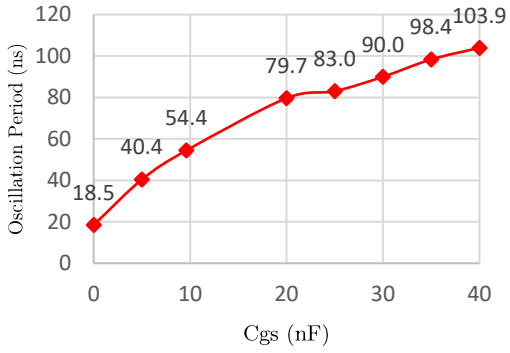

Fig. 12 Trend of time period of the oscillations versus C_{gs}

Here another thing that can be noted is how for small values of C_{gs} its effect seems to have little effect on the said output characteristics whilst after some threshold (Here around 9nF) it skyrockets.

4. Conclusion

It is observed that parasitic effect of a CMOS inverter plays a major role in building oscillators. We have demonstrated how oscillation characteristic of a 3-Stage Ring Oscillator changes with the parasitic capacitance value of used NMOS transistors. It can be concluded that changing similar parameters in MOSFETs we can increase or decrease parasitic effect contributed to the oscillator by said transistors, thereby change its frequency or time it takes to start oscillation. From literature [3] we have,

$$f_{oscillation} = \frac{1}{2N\tau_p}$$

where N is number of inverters and τ_p *is* delay from each inverter. We also have that [4],

$$\tau_p = \frac{C_L + C'_L}{G_m}$$

With G_m, C_L and C'_L being conductance equivalent to the switch, node parasitic capacitance and the capacitance of the added NMOS (We modelled this using C_{gs}). Using the above it can be shown further that the simulation results are in order as the oscillation frequency ultimately equates to,

$$f_{oscillation} = \frac{1}{2N}\frac{G_m}{C_L + C'_L}.$$

s

II. Circuit 2: PLD

Part 1: Design a programable logic block to configure it as a 'NAND' or a 'NOR' gate using a single selection bit.

Table 4: Truth table of the PLD

S	A	B	Y	
0	0	0	1	NAND
0	0	1	1	
0	1	0	1	
0	1	1	0	
1	0	0	1	NOR
1	0	1	0	
1	1	0	0	
1	1	1	0	

This Programmable Logic Block can be configured as a 'NAND' gate when the selection bit (S) is 0 and as a 'NOR' gate when the selection bit (S) is 1.

Truth table of this PLD shown in Table 4. The Boolean Expression for the output (Y) is obtained using Karnaugh maps. Then it is written in terms of NOR gates to make this a NOR-NOR PLA.

$$Y = \overline{A}.\overline{B} + \overline{S}.(\overline{A} + \overline{B})$$

$$\overline{Y} = \overline{\overline{A+B} + \overline{A+S} + \overline{B+S}}$$

To simulate this, signals were fed into the inputs S, A and B as in the truth table. 10ms time period was used to represent each state. Here we obtain the intended output as in the truth table.

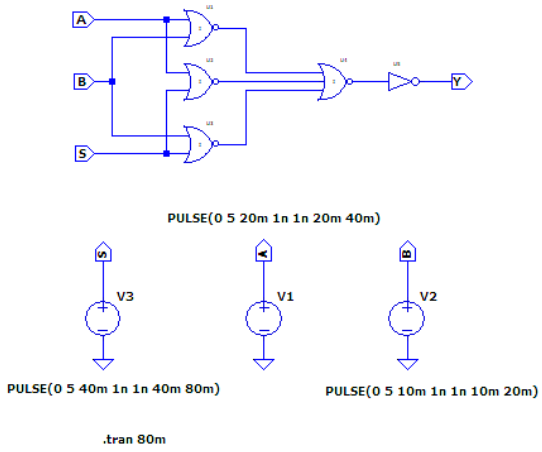

Fig. 13 PLD circuit configurable as NAND or NOR

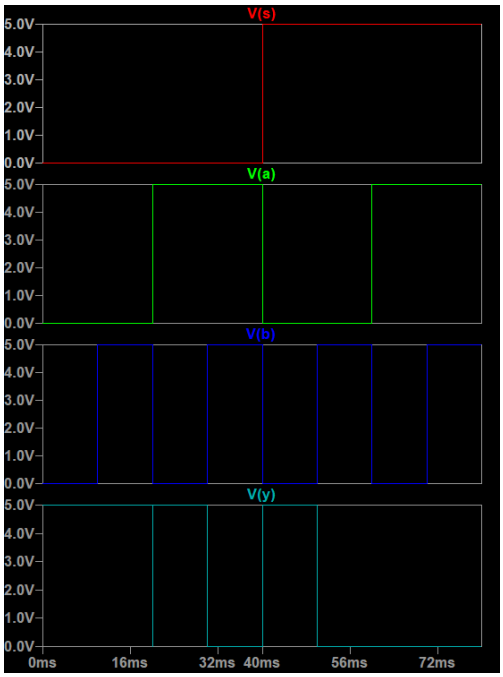

Fig. 14 Graphical Representation of the Truth table

Part 2: Design a single switch matrix using six pass transistors.

FPGA architectures are dominated by programmable interconnects which gives more flexibility to obtain more complex designs with fixed I/O pin assignment and predictable delays. Interconnects are programmed by switch matrices where paths

can be connected or disconnected using transistors.

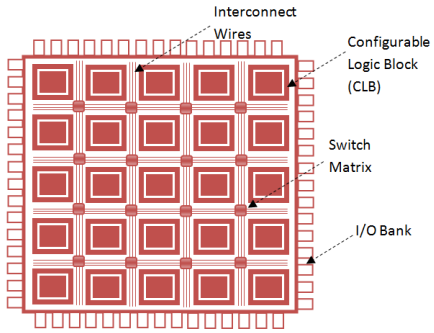

Fig. 15 FPGA Architecture

Routes created by Transistors inside the switch matrix should be bi-directional. But a bi-directional path could not be achieved using a normal NMOS, as the body (substrate) terminal is connected internally to the Source terminal. So, to ground the body, Source need to be grounded which disables the chance of conducting from Source to Drain. So, we used NMOS4 transistor in LTspice instead of the normal NMOS. NMOS4 is a Monolithic MOSFET which is a 4-terminal device. It has a separate body (substrate) terminal which can be used to ground the body independent of the Source. When the body terminal is grounded, by giving a HIGH voltage to the Gate, a bi-directional channel is created which can conduct either from Source to Drain or from Drain to Source.

To simulate the operation of a switch matrix, I designed a 6-transistor switch matrix which is located in a junction of 4 routes. I gave an Input signal to one side and observed the output from other 3 sides. I connected some selected paths by switching on their respective transistors. Then I could observe a similar output signal as the input from routes which were connected but other outputs were floating. This happened because when the transistor is off, output terminal is not connected to anywhere. So, I used Pull-Down resistor at each output terminal to ground them when they are disconnected.

Example 01:

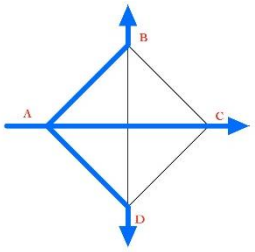

Fig. 15 A-B, A-C, A-D Paths Connected.

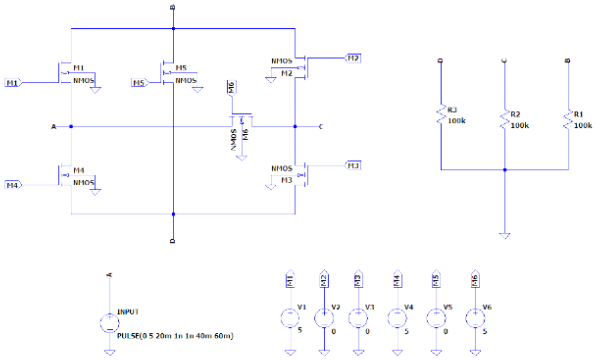

Fig. 17 Circuit Example 01

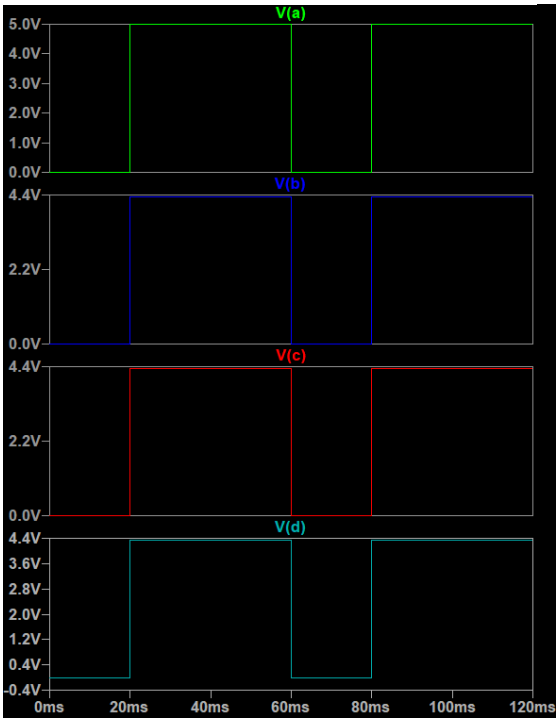

Fig. 18 Input(A) and Output (B, C, D) variation with time.

Example 02:

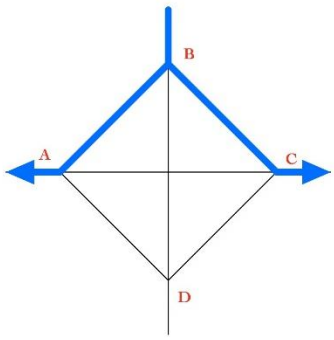

Fig. 19 B-A, B-C Paths Connected.

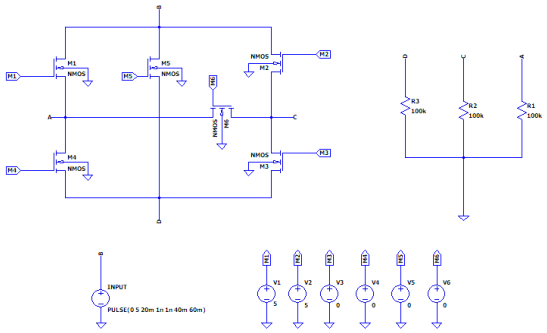

Fig. 20 Circuit Example 02

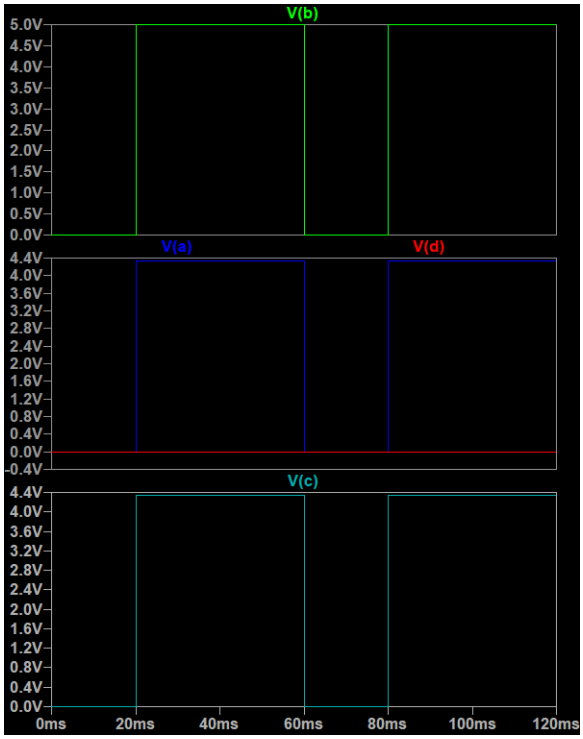

Fig. 21 Input (B) and Output (A, C) variation with time.

Example 03:

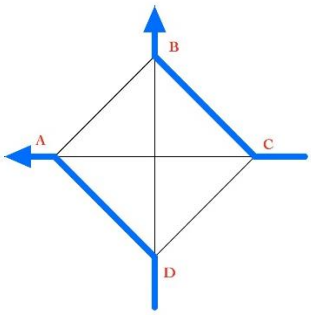

Fig. 22 D-A, C-B Paths Connected.

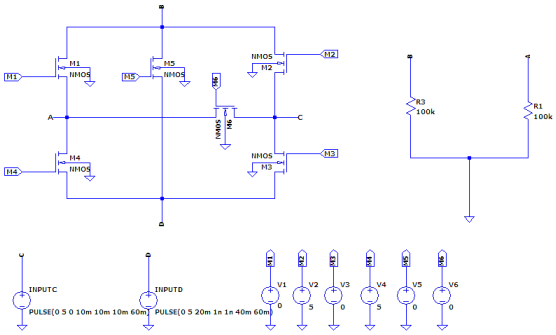

Fig. 23 Circuit Example 03

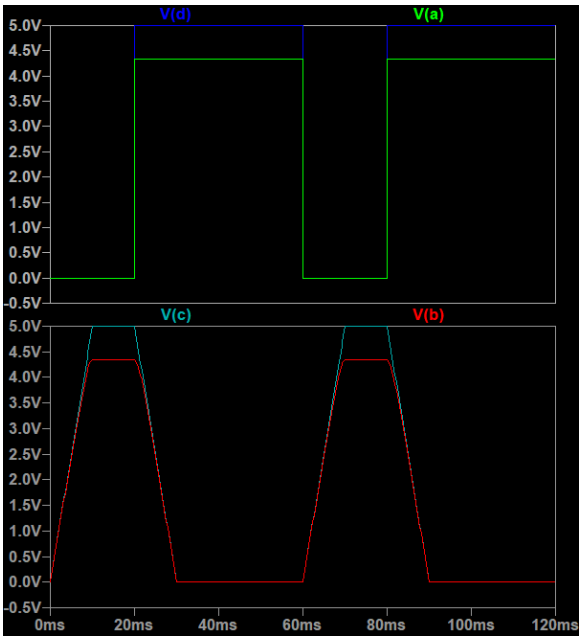

Fig. 24 Input (C, D) and Output (A, B) variation with time.

Part 3: Design a PLD that can be used to design any 3-input combinational circuit.

A programmable logic device (PLD) has an implemented logic design that can be reconfigured in the field by the end-user. A PLD must be programmed before it is used for a specific task. Under SPLD(simple PLD), there are three types of PLDs such as PROM, PAL and PLA which differ from each other relative to the programmable and fixed layers of it. Any sum of products can be represented by AND-OR layers and in PROM, AND layer is fixed while the OR layer is programmable. PAL has a programmable AND and Fixed OR. Both AND and OR layers are programmable in PLA.

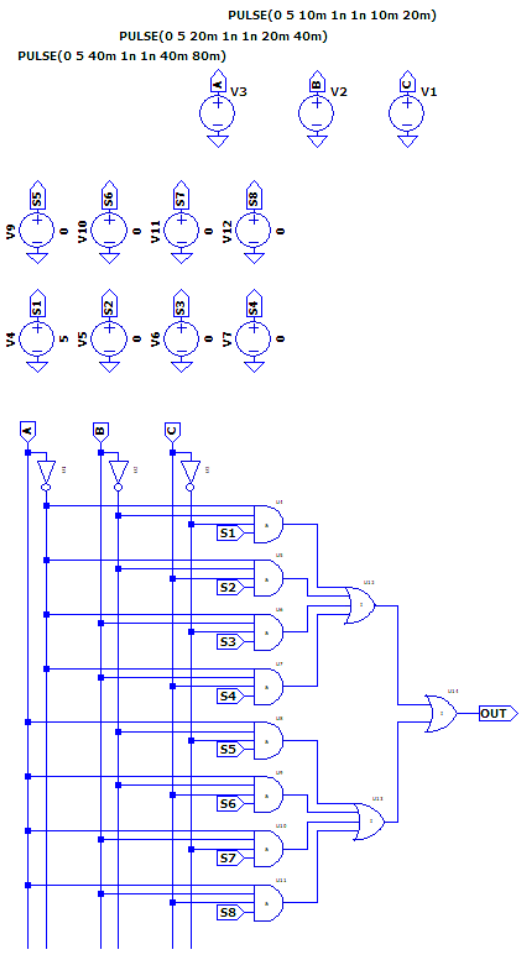

Fig. 25 Configurable 3 -Input Combinational Logic Circuit

Any combinational logic circuit can be implemented as a sum of minterms. Since, this is a 3-Input PLD, there are only 8 minterms as included in this table. So, any 3-Input combinational logic circuit can be implemented as a sum of these minterms.

As shown in Fig. 25 circuit diagram, 8 combinations are made and each of them are fed into AND gates with a selection bit. Then minterm can feed into the OR gate by making the selection bit into logic gate 1 (5V). Therefore, this PLD circuit can be used to design any 3-input combinational circuit.

Table 5: Selection Pins with Respective Minterms

Selection Pin	Combination
S1	$\bar{A}\bar{B}\bar{C}$
S2	$\bar{A}\bar{B}C$
S3	$\bar{A}B\bar{C}$
S4	$\bar{A}BC$
S5	$A\bar{B}\bar{C}$
S6	$A\bar{B}C$
S7	$AB\bar{C}$
S8	ABC

In this Design, all 8 minterms are generated using 8 AND gates and the appropriate minterms are selected using the Selection bits which are then added using OR gates. So, this becomes a PROM as the AND plane is fixed, and the OR plane is programmable.

The combination of A, B, C inputs act as an address and the Selection bits represent the memory which needed to be written appropriately prior to using this PROM.

Example 1: 3 Input XOR gate

Output waveform is similar to the 3 input XOR output as mentioned in the truth table. There exist voltage spikes at 20ms and 60ms in the output waveform because the inputs are switching from high to low or low to high.

Table 6: Truth Table for 3-Input XOR Gate

Inputs			Output
A	B	C	$A \oplus B \oplus C$
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

.

Example 2: 3 Input NOR gate

NOR gate also can be implemented by setting the S1 selection bit into logic state high.

Table 7: Truth Table for 3-Input NOR Gate

Inputs			Output
A	B	C	$\overline{A+B+C}$
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	0

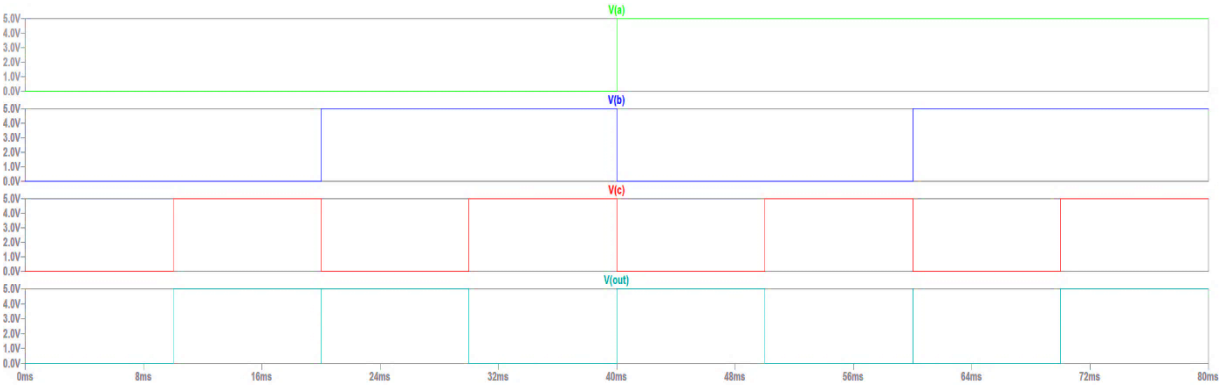

Fig. 26 Wave Diagram for Example 1

Fig. 27 Wave Diagram for Example 2

5. References

1. Design of Analog CMOS Integrated Circuits – Behzad Razvi
2. https://techweb.rohm.com/knowledge/si/s-si/03-s-si/4873
3. Design and Analysis of 3 Stage Ring Oscillator Based on MOS Capacitance for Wireless Applications - Rafiul Islam, Ahmad Nafis Khan Suprotik, S. M. Zia Uddin & Md. Tawfiq Amin
4. https://www.researchgate.net/publication/316908267
5. https://en.wikipedia.org/wiki/Barkhausen_stability_criterion
6. E.R. Patchett et al. / Organic Electronics 15 (2014) 1493–1502
7. University „Politehnica“ Bucharest - Simulation of a ring oscillator with CMOS Inverters
8. CMOS Design and Performance Analysis of Ring Oscillator for Different Stages - Saikee Chauhan, Rajesh Mehra
9. https://www.reddit.com/r/AskElectronics/comments/eoayaa/why_am_i_getting_different_behavior_between_my/
10. Electronic Devices (CONVENTIONAL CURRENT VERSION), Ninth Edition - by Thomas L. Floyd
11. https://www.eetimes.com/all-about-fpgas/#
12. https://allaboutfpga.com/fpga-architecture/
13. https://www.electronics-tutorials.ws/transistor/tran_6.html
14. https://ininet.org/chapter-3-combinational-logic-design-with-plds.html