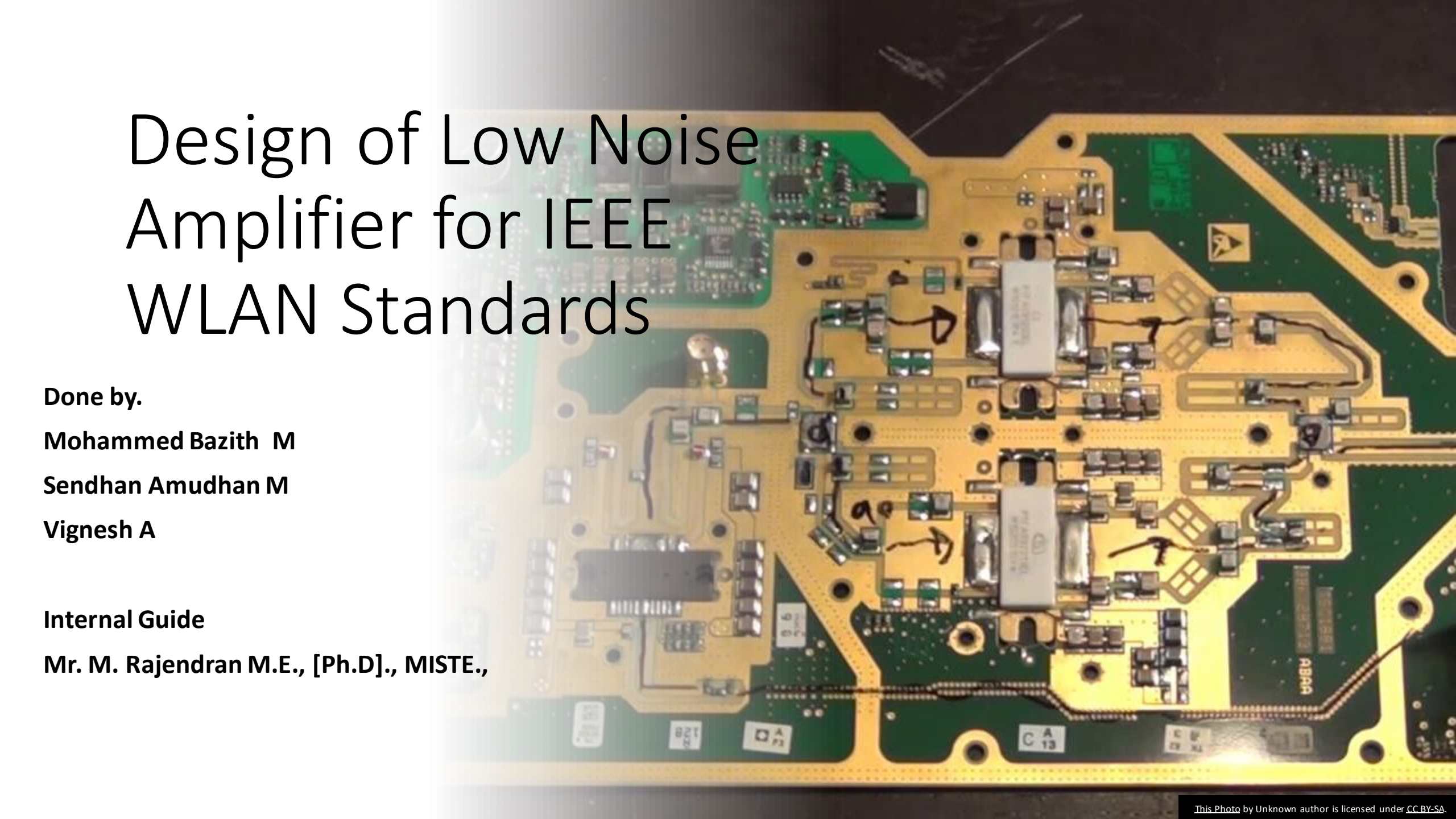
Design of Low Noise Amplifier for IEEE WLAN Standards



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Internal Guide

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Introduction

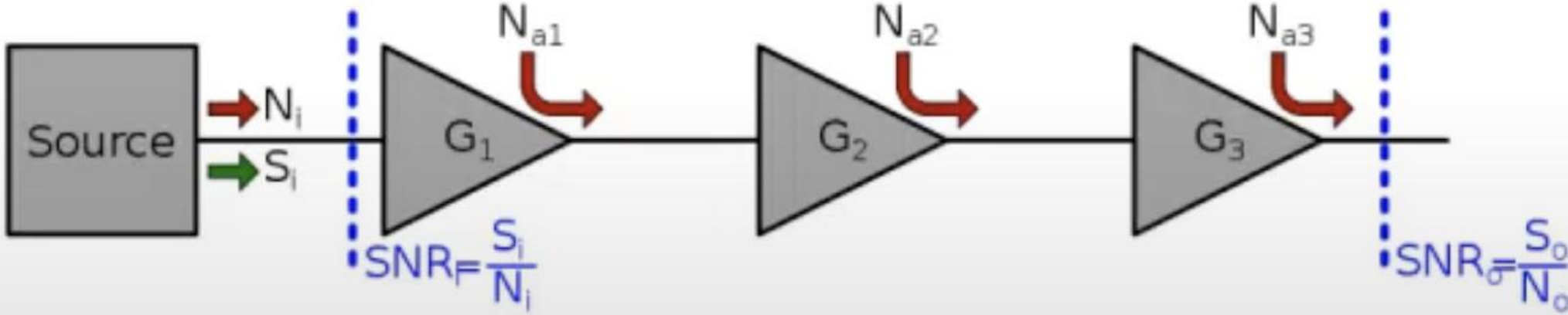
- This project presents the design of low noise amplifier (LNA) targeted for WLAN IEEE standards. The amplifier is designed to of frequency bands: 6 GHz (5.925–7.125 GHz), which is the frequency band of Wi-Fi 6E. The LNA is designed using a combination of active and passive components to achieve a high gain, low noise figure, and good linearity.
- The final design is realized using ADS Software and is tested for its performance in terms of gain, noise figure, and input/output impedance matching.
- Expected simulation results of the LNA will have gain of about 25-28 dB and a NF < 1.5 dB across the mentioned frequency band and will have reflection losses < -15 dB.
- The design methodology presented in this paper can also be used as a reference for the design of other LNAs for wireless communication applications.

What is a LNA?

- A low noise amplifier (LNA) is an electronic amplifier designed to amplify weak signals while adding as little noise as possible.
- The goal of an LNA is to amplify the signal with minimal distortion or noise so that it can be further processed or transmitted.
- LNAs are commonly used in radio frequency (RF) systems, such as in wireless communication devices, radar systems, and satellite receivers.
- In addition to amplifying the signal, an LNA also typically includes a number of features to reduce noise, such as using low-noise components and shielding the circuit from electromagnetic interference.
- Overall, the purpose of an LNA is to improve the sensitivity and overall performance of an RF system by amplifying weak signals while minimizing the introduction of noise.

$$F_{\text{total}} = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 G_2} + \frac{F_4 - 1}{G_1 G_2 G_3} + \cdots + \frac{F_n - 1}{G_1 G_2 \cdots G_{n-1}}$$

where F_i and G_i are the noise factor and available power gain, respectively, of the *i*-th stage, and *n* is the number of stages. Both magnitudes are expressed as ratios, not in decibels.



Noise Figure $$\mathrm{NF} = 10 \log_{10}(F) = 10 \log_{10}\left(\frac{\mathrm{SNR_i}}{\mathrm{SNR_o}}\right) = \mathrm{SNR_{i,\,dB}} - \mathrm{SNR_{o,\,dB}}$$

Literature Review

S.No	TITLE	AUTHOR	YEAR	MAJOR FINDINGS
1.	Switched Low-Noise Amplifier Using Gyrator-Based Matching Network for TD-LTE/LTE-U/Mid-Band 5G and WLAN Applications	Tsai, C.-H.; Lin, C.-Y.; Liang, C.-P.; Chung, S.-J.; Tarng, J.-H.	6 February 2021	This paper presents a low-noise amplifier (LNA) fabricated using a 0.18 µm Complementary Metal-Oxide Semiconductor (CMOS) process. The LNA uses a double-peak load network. The target frequencies of the triple-band LNA are 2.3–2.7 GHz, 3.4–3.8 GHz, and 5.1–5.9 GHz, covering the operating frequency bands of time-division long-term evolution (TD-LTE), mid-band Fifth generation (5G), LTE-unlicensed (LTE-U) band, and Wireless LAN (WLAN) technology. The measured power gains and noise figures at 2.5, 3.5, and 5.2 GHz are 12.3, 15.3, and 13.1 dB and 2.3, 2.2, and 2.6 dB, respectively.
2.	Design of an Ultra Low Power Low Noise Amplifier for 5-GHz band	Nishant Kumar, Rajini Bisht	2020	This paper is presented an ultra-low power Low Noise Amplifier (LNA) for 5-GHz frequency band. The operating voltage of this Low Noise Amplifier is 0.63 V. By using these techniques forward-body-bias and Current-reuse DC power dissipation is reduced. Capacitive Coupling is used for gain boosting. Simulation result shows the Noise Figure (NF) of 4.1 dB and 21.4 dB of gain at 5-GHz with 0.63 V operating voltage & power dissipation is 0.48 mW. This LNA is implemented using 180 nm TSMC library.

3.	Design at 2.4GHz Low Noise Amplifier for Wi-Fi-Application	M. EL BAKKALI, N.AMAR TOUMI, T. ELHAMADI	2020	This This paper presents a low noise amplifier (LNA) for WLAN applications. The target frequency band 802.11b/g 2.4GHz. The amplifier is characterized by input and output reflection coefficients less than -15dB, a forward gain (S21) of 15.112dB, a noise figure of 0.37dB and the third input intercept point of 14.8dB .
4	Practical Considerations for Low Noise Amplifier Design	By Tim Das Freescale Semiconductor	2013	This paper reviews the various parameters which is needed to be considered like topology, NF, Gain, Linearity, etc.
5	CMOS Low-Noise Amplifier Design Optimization Techniques	Kein Nguyen, Sang-Gug Lee		This paper presents reviews and analyses the different noise optimization techniques used **classical noise matching, simultaneous noise and input matching (SNIM), power-constrained noise optimization, and power-constrained simultaneous noise and input matching (PCSNIM) techniques.**

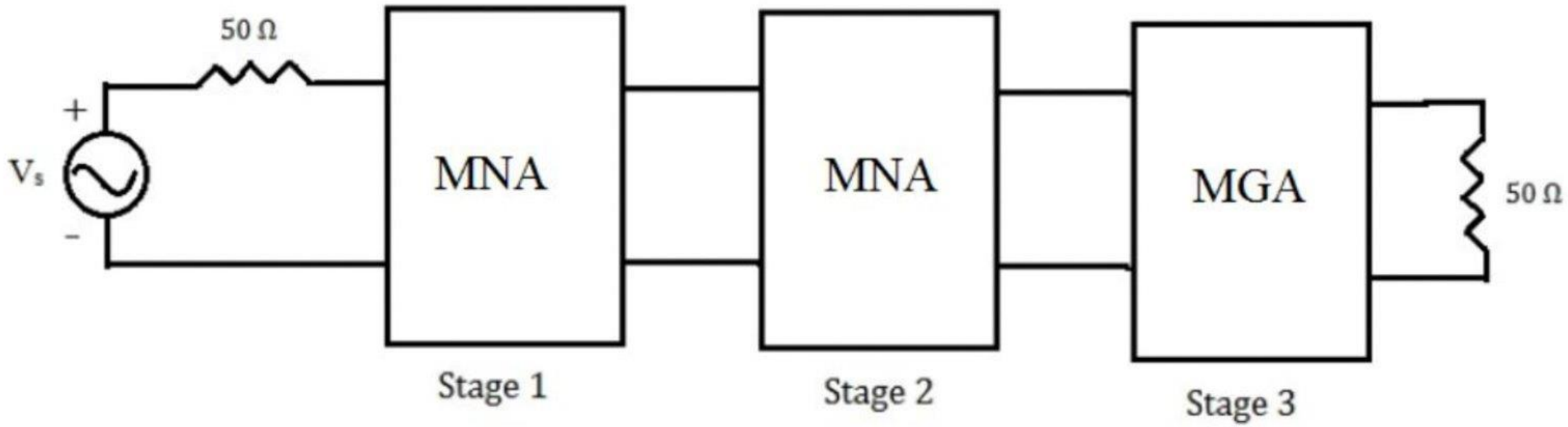
Problem Statement

- The objective of this research project is to design and develop a low noise amplifier (LNA) circuit capable of meeting the performance requirements for IEEE WLAN IEEE 802.11ax standards.
- Specifically, this project aims to design a LNA with predicted gains around 25-28 dB and a NF < 1.5 dB, which can be operated at 6 GHz (5.9–7.1 GHz) frequency range.
- The LNA will be optimized for high linearity and low noise figure, and will be implemented using GaAs FET technology.
- The goal of this project is to provide high-performance solution for wireless communication systems operating in the 6 GHz frequency range.

Proposed Solution

- Design a LNA for WLAN IEEE 802.11ax standard (Wi-Fi 6E) using three stages of amplifiers.
- Where the first two stages are dedicated for minimum noise amplifications.
- The final stage is used for maximum gain amplification.
- The individual amplifiers of each stage are designed using common source topology.
- Common source topology provides high power gain with low noise figure.

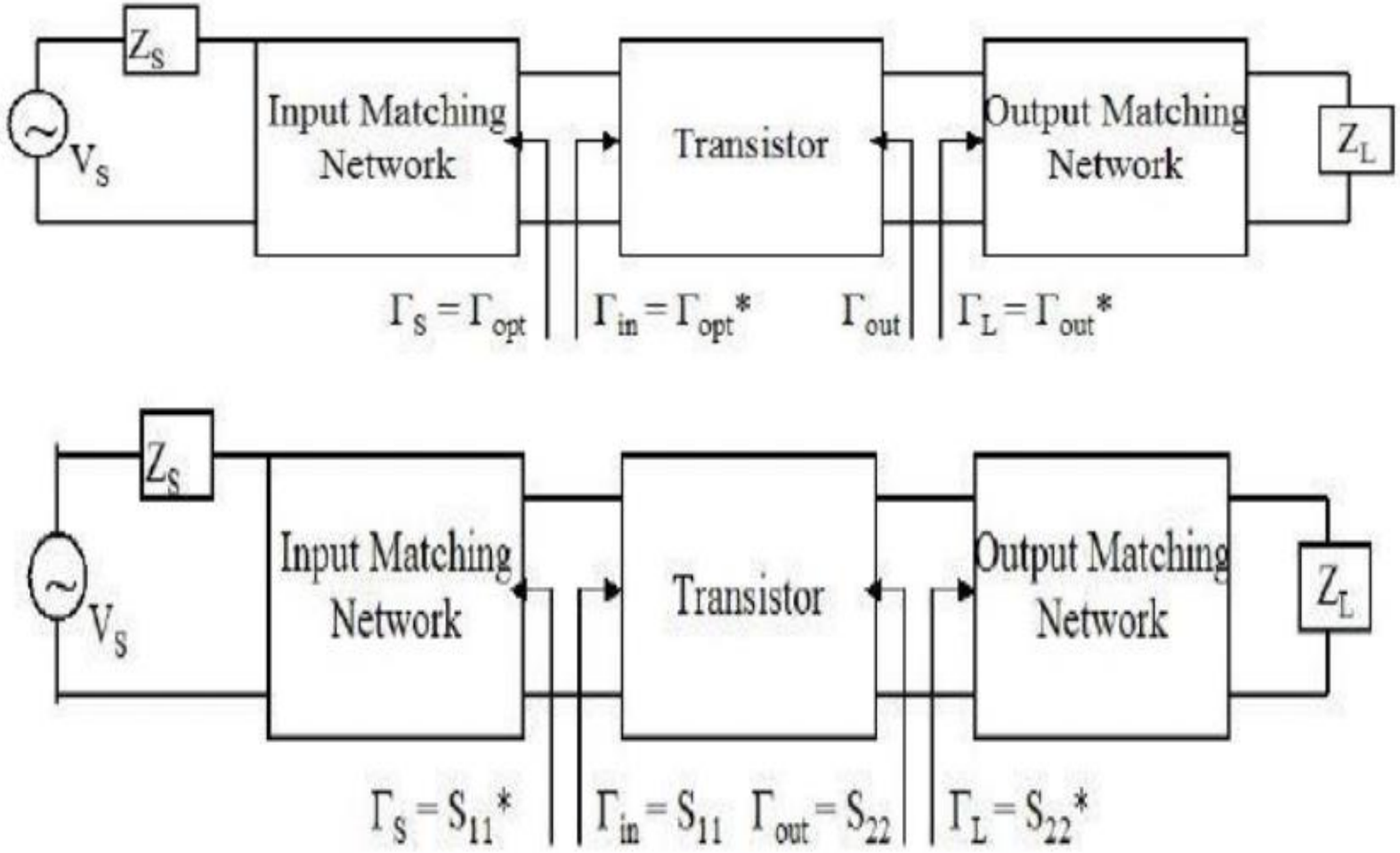
Block Diagram of the Three Stages



Design of Matching Network

- The key to design a low noise amplifier is to keep the noise to the minimum as possible and obtain maximum gain from the design.
- In order to deliver maximum power at an output as well as an input of the design, it is necessary to design the matching networks precisely.
- Matching network can be designed with lumped elements such as resistors, capacitors or else with distributed elements such as transmission line, stubs.
- In this project, distributed elements are used for designing matching networks as the frequency is quite high.

Matching Network Design Methodology



Comparison between existing model and proposed model

Model	Transistor type	Operating Frequency	Characteristics	Gain and Noise Figure
Existing System	CMOS	5 GHz	Low Power Consumption and High Integration	Gain: 21.4 dB Noise Figure: 4.1 dB
Proposed System	GaAs FET	6 GHz	Low Noise Figure and High Gain (More Suitable for Higher Frequency)	Gain: 25-28 dB Noise Figure: < 1.5 dB

Types of Transistors

Process Technologies

The most popular active devices used in LNAs are based on GaAs pHEMTs and SiGe BiCMOS process technologies. Performance differences between the two technologies are shown in Table 3.

Table 3. Comparison of Device Technologies for L− and S−Band LNAs

Typical Performance	GaAs pHEMT	SiGe BiCMOS
Noise Figure (dB)	≥ 0.4	≥ 0.9
Gain (dB	12 to 21	10 to 17
OIP3 (dBm)	≥ 41	≥ 31
Breakdown Voltage (Vdc)	15	much less than 15 V
Inductor Q−factor	15	5 to 10
Strengths	High P1dB and OIP3, very low noise figure	Higher integration, lower cost, ESD immunity
f_T/f_{MAX}	Similar	

HEWLETT PACKARD

ATF-13136
2-16 GHz Low Noise Gallium Arsenide FET

Features

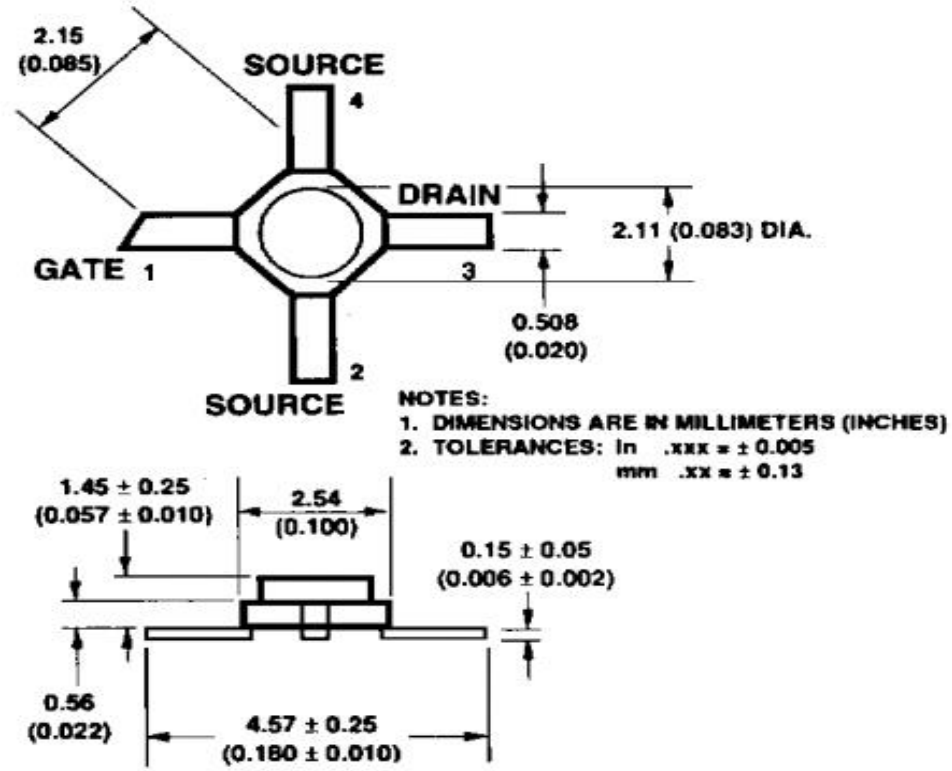
- **Low Noise Figure: 1.2 dB typical at 12 GHz**
- **High Associated Gain: 9.5 dB typical at 12 GHz**
- **High Output Power: 17.5 dBm typical $P_{1\,dB}$ at 12 GHz**
- **Cost Effective Ceramic Microstrip Package**
- **Tape-and-Reel Packaging Option Available[2]**

Description

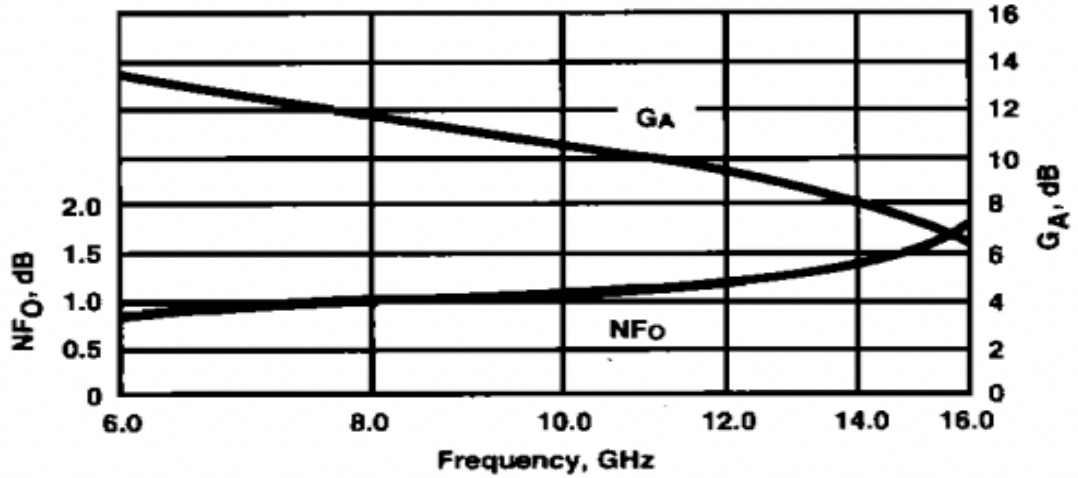
The ATF-13136 is a high performance gallium arsenide Schottky-barrier-gate field effect transistor housed in a cost effective microstrip package. Its premium noise figure makes this device appropriate for use in the first stage of low noise amplifiers operating in the 2-16 GHz frequency range.

This GaAs FET device has a nominal 0.3 micron gate length with a total gate periphery of 250 microns. Proven gold based metallization systems and nitride passivation assure a rugged, reliable device.

36 micro-X Package[1]



OPTIMUM NOISE FIGURE AND ASSOCIATED GAIN vs. FREQUENCY
V_{DS} = 2.5 V, I_{DS} = 20 mA, T_A = 25°C



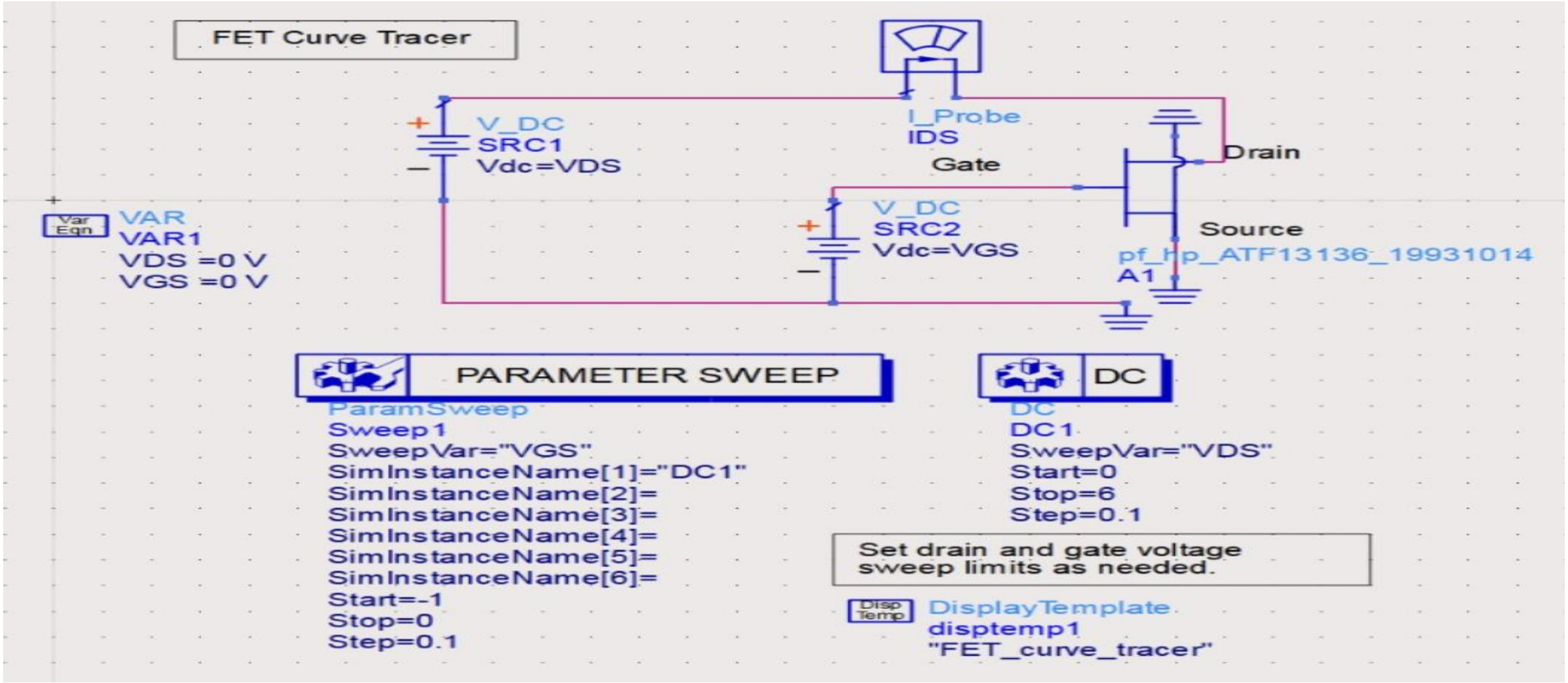
Noise Parameters: V_{DS} = 3 V, I_{DS} = 20 mA

Freq. GHz	NF_O dB	Gamma Opt Mag	Gamma Opt Ang	$R_N/50$
4.0	0.5	.58	87	.22
6.0	0.8	.47	130	.18
8.0	1.0	.37	–163	.17
12.0	1.2	.47	–65	.80
14.0	1.4	.52	–15	1.20

Electrical Specifications, T_A = 25°C

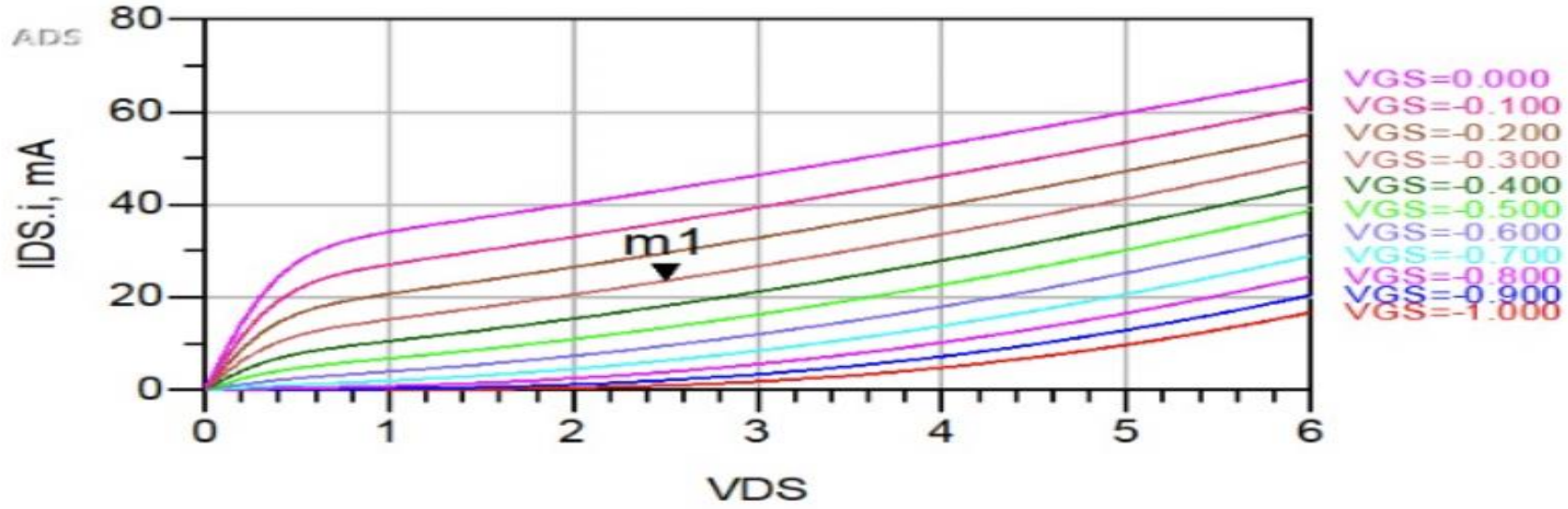
Symbol	Parameters and Test Conditions		Units	Min.	Typ.	Max.
NF_O	Optimum Noise Figure: V_{DS} = 2.5 V, I_{DS} = 15 - 30 mA	f = 8.0 GHz f = 12.0 GHz f = 14.0 GHz	dB dB dB		1.0 1.2 1.4	1.4
G_A	Gain @ NF_O: V_{DS} = 2.5 V, I_{DS} = 15 - 30 mA	f = 8.0 GHz f = 12.0 GHz f = 14.0 GHz	dB dB dB	8.5	11.5 9.5 8.0	
$P_{1\,dB}$	Output Power @ 1 dB Gain Compression: V_{DS} = 4 V, I_{DS} = 40 mA	f = 12.0 GHz	dBm		17.5	
$G_{1\,dB}$	1dB Compressed Gain: V_{DS} = 4 V, I_{DS} = 40 mA	f = 12.0 GHz	dB		8.5	
g_m	Transconductance: V_{DS} = 2.5 V, V_{GS} = 0 V		mmho	25	55	
I_{DSS}	Saturated Drain Current: V_{DS} = 2.5 V, V_{GS} = 0 V		mA	40	50	90
V_P	Pinchoff Voltage: V_{DS} = 2.5 V, I_{DS} = 1 mA		V	–4.0	–1.5	–0.5

DC Bias of the Transistor (FET Tracer Curve)



FET Bias Characteristics

Use with FET_curve_tracer Schematic Template

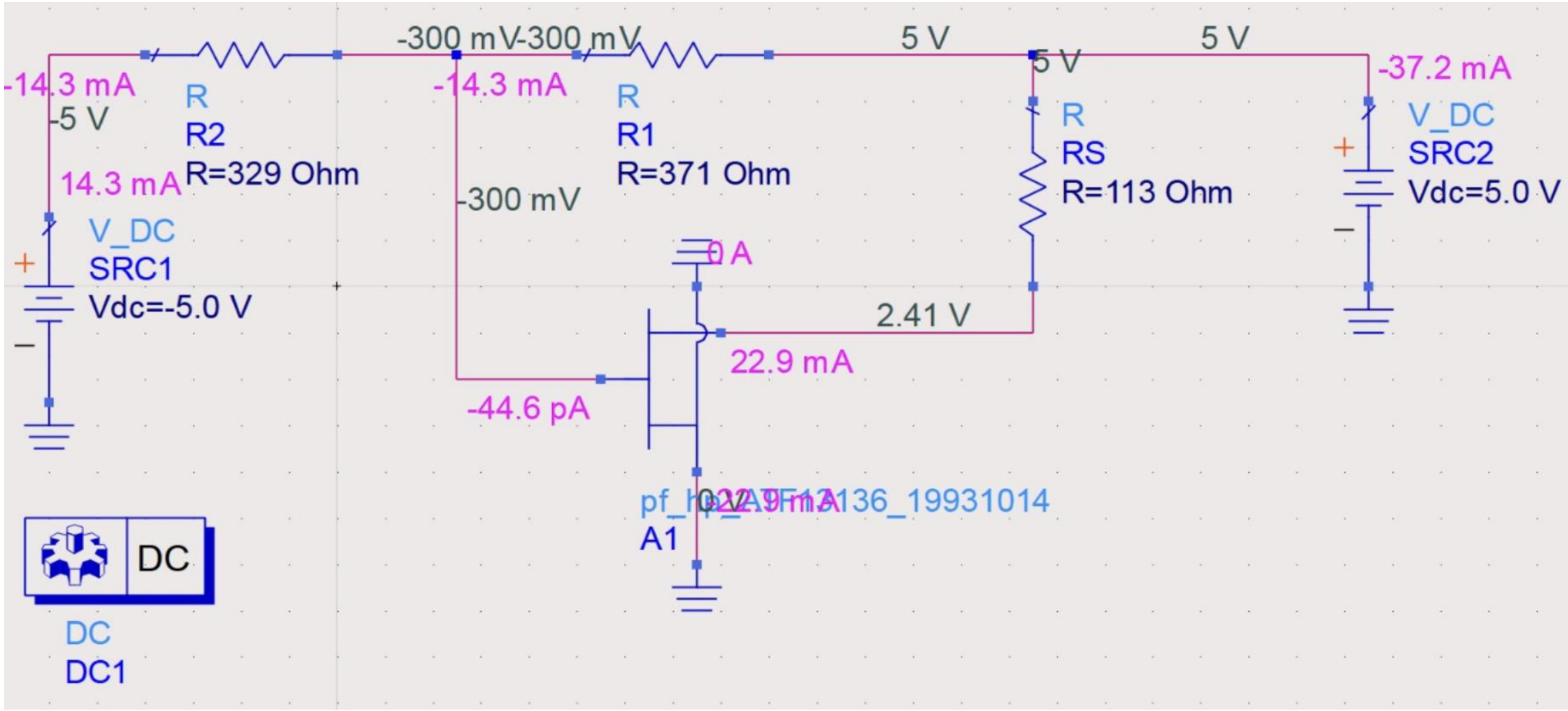


Values at bias point indicated by marker m1.
Move marker to update.

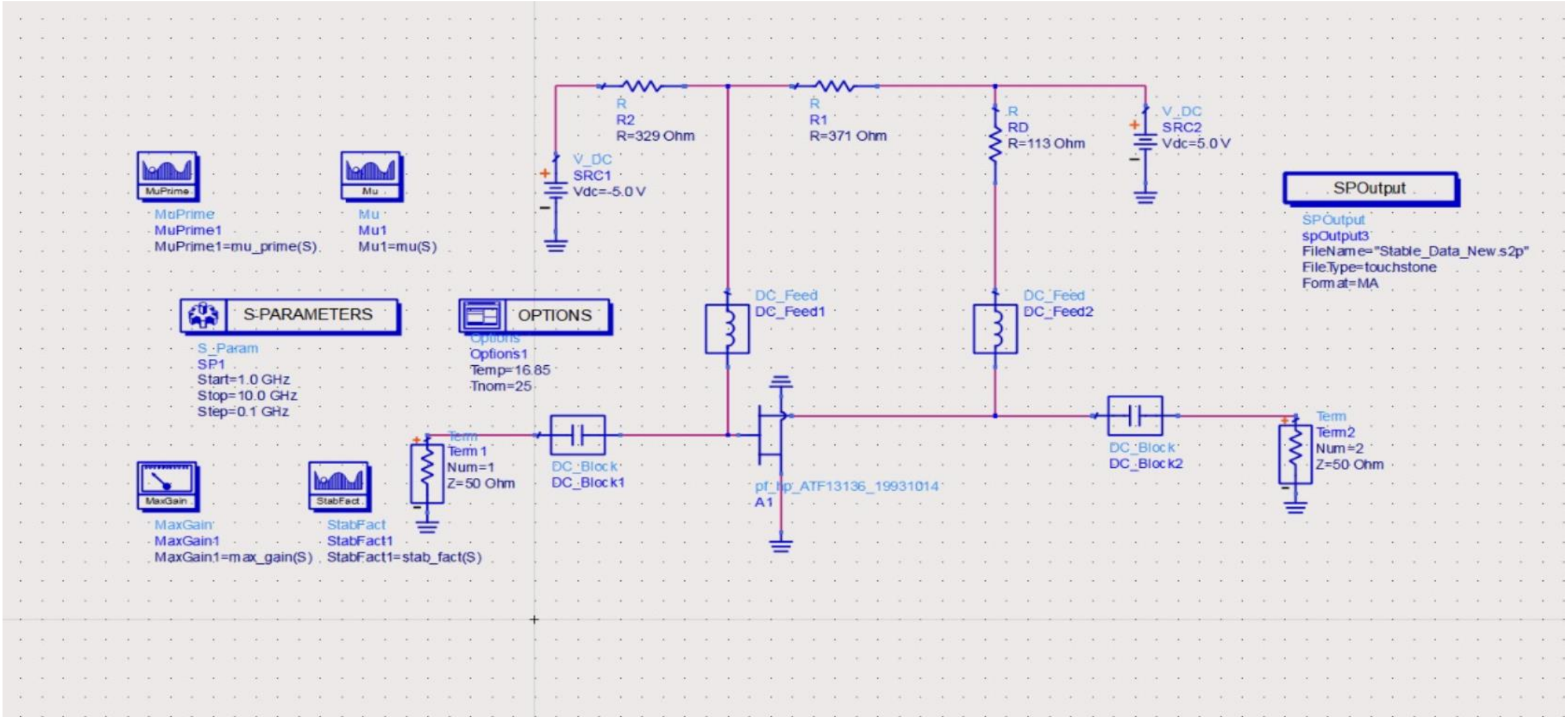
VDS	Device Power Consumption, Watts
2.500	0.059

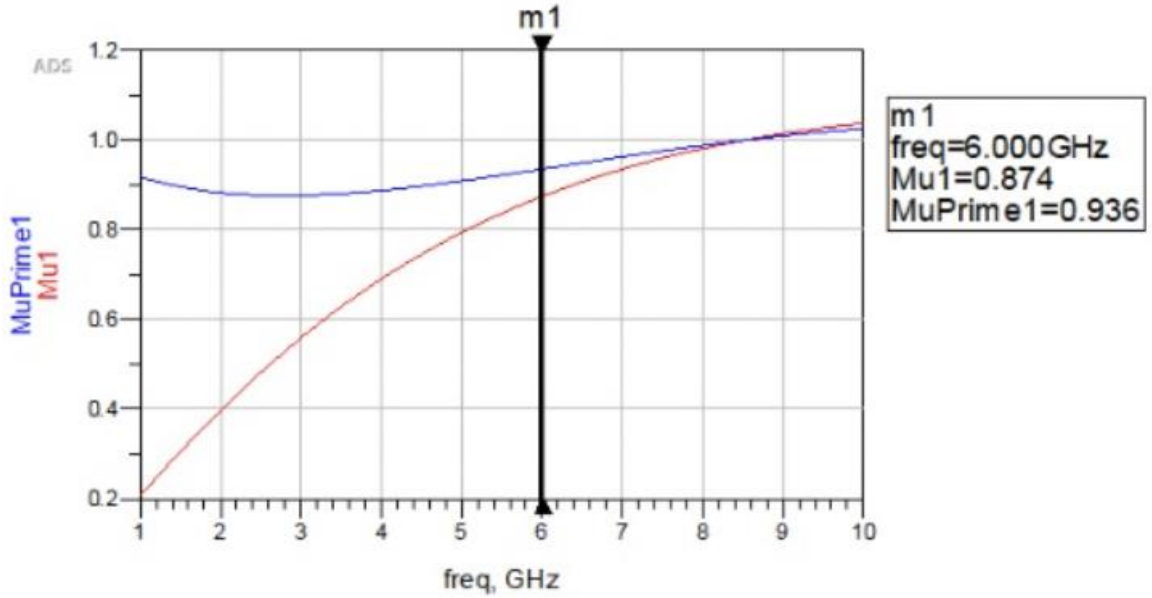
m1
VDS=2.500
IDS.i=0.024
VGS=-0.300

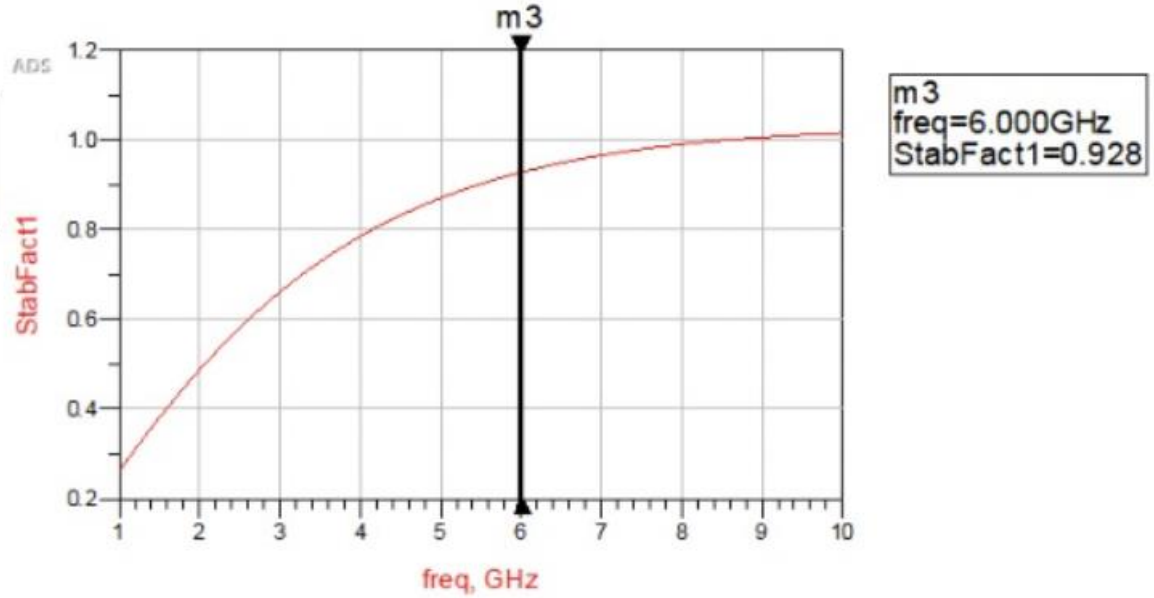
DC Biasing

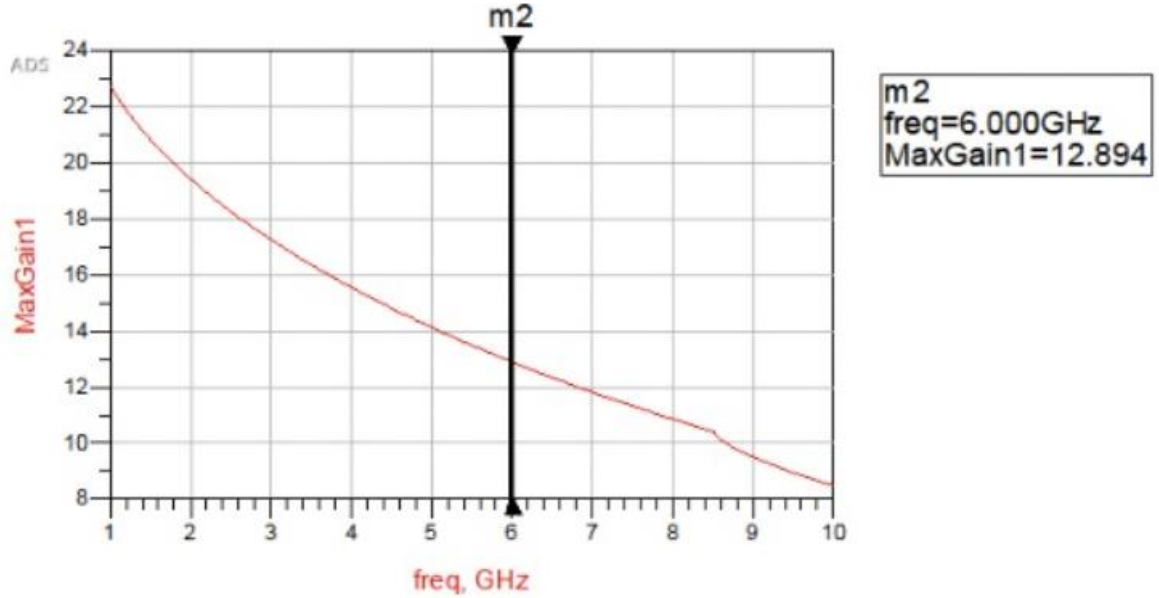

-14.3 mA
-5 V
R
R2
R=329 Ohm
14.3 mA
V_DC
SRC1
Vdc=-5.0 V
-300 mV
-300 mV
-14.3 mA
R
R1
R=371 Ohm
-300 mV
0 A
-44.6 pA
5 V
5 V
5 V
R
RS
R=113 Ohm
2.41 V
22.9 mA
-37.2 mA
V_DC
SRC2
Vdc=5.0 V
0 V
22.9 mA
A1
DC
DC
DC1

Determining the S parameters and Stability

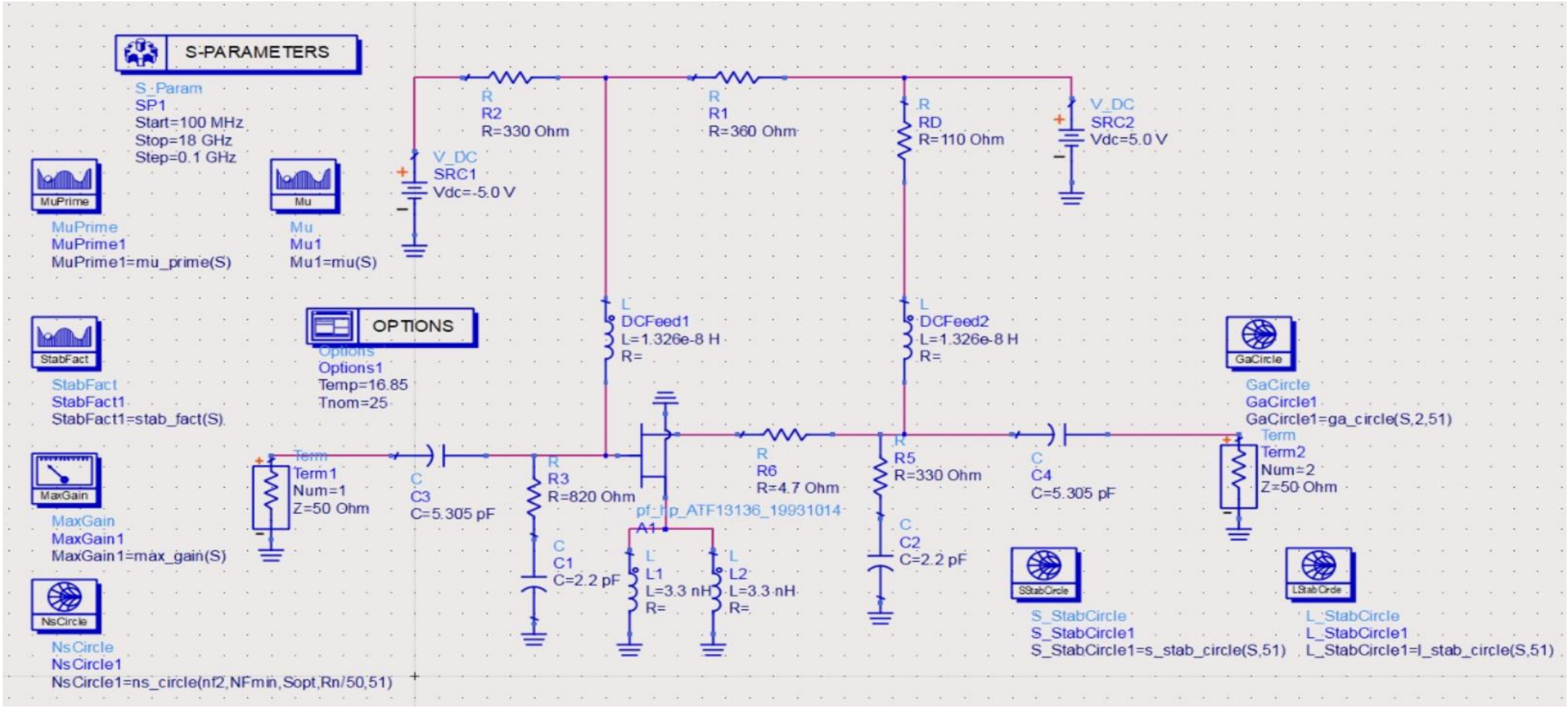


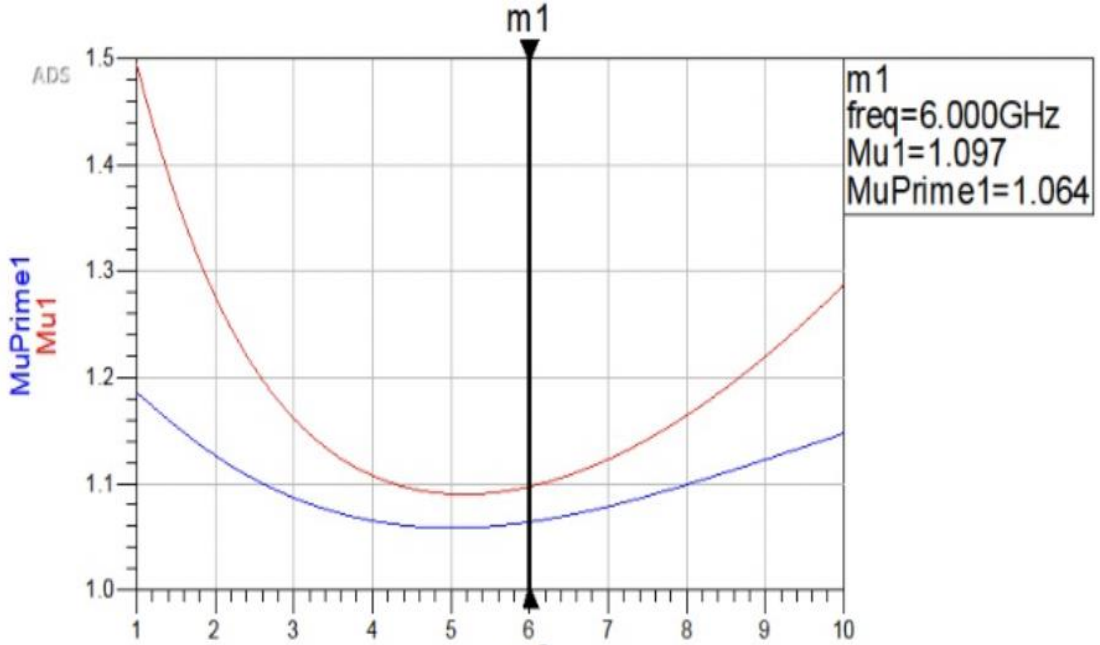

m1
ADS
MuPrime1
Mu1
freq, GHz
m1
freq=6.000GHz
Mu1=0.874
MuPrime1=0.936

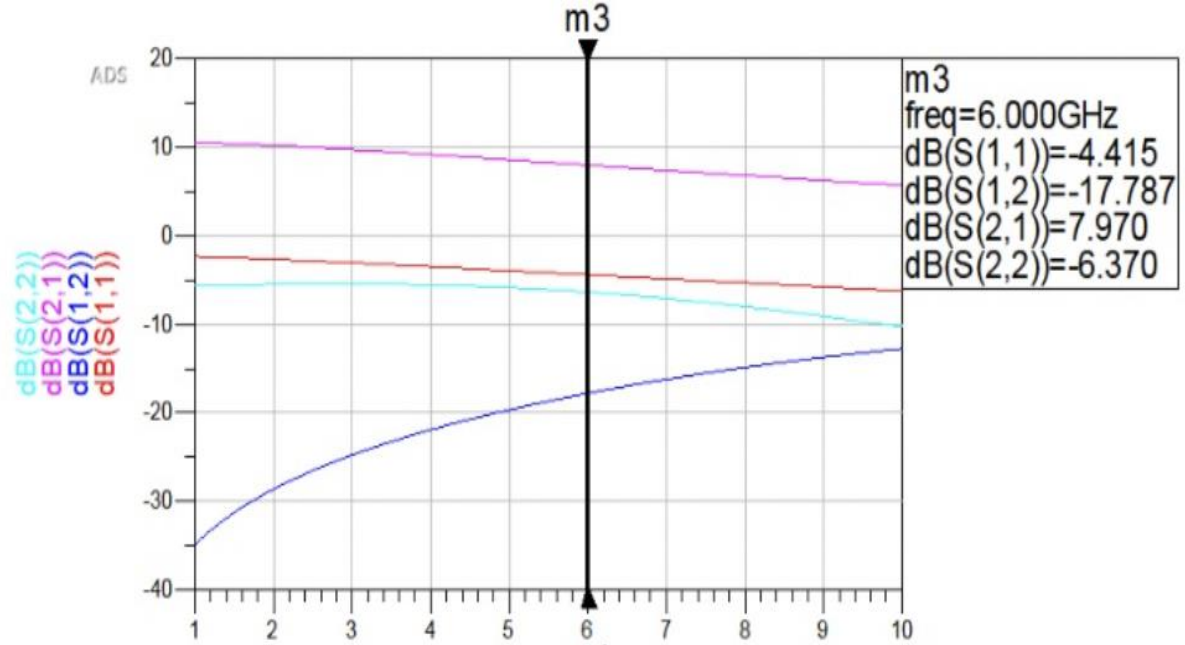

m3
ADS
StabFact1
freq, GHz
m3
freq=6.000GHz
StabFact1=0.928

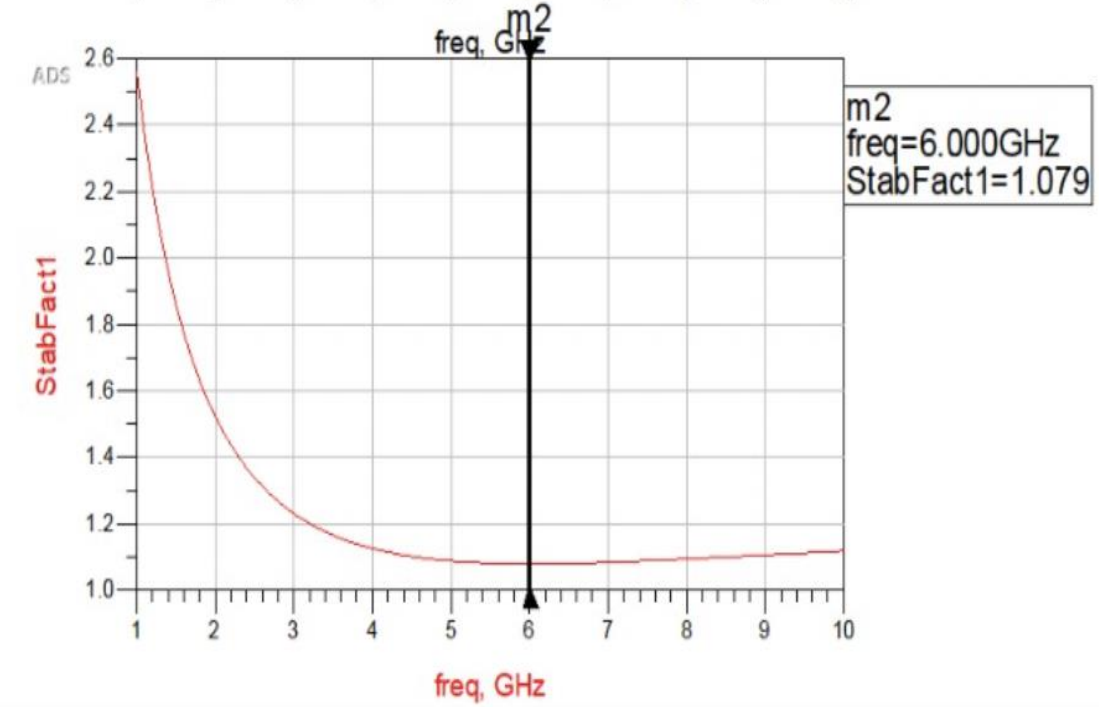

m2
ADS
MaxGain1
freq, GHz
m2
freq=6.000GHz
MaxGain1=12.894

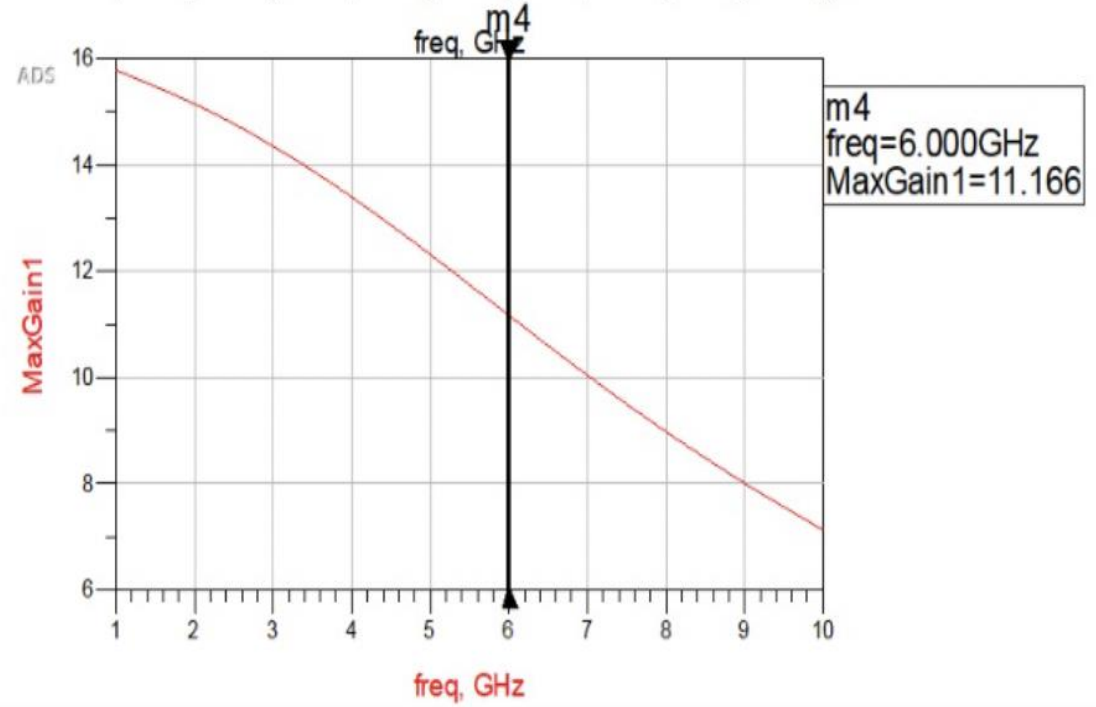
Source Inductive Degeneration



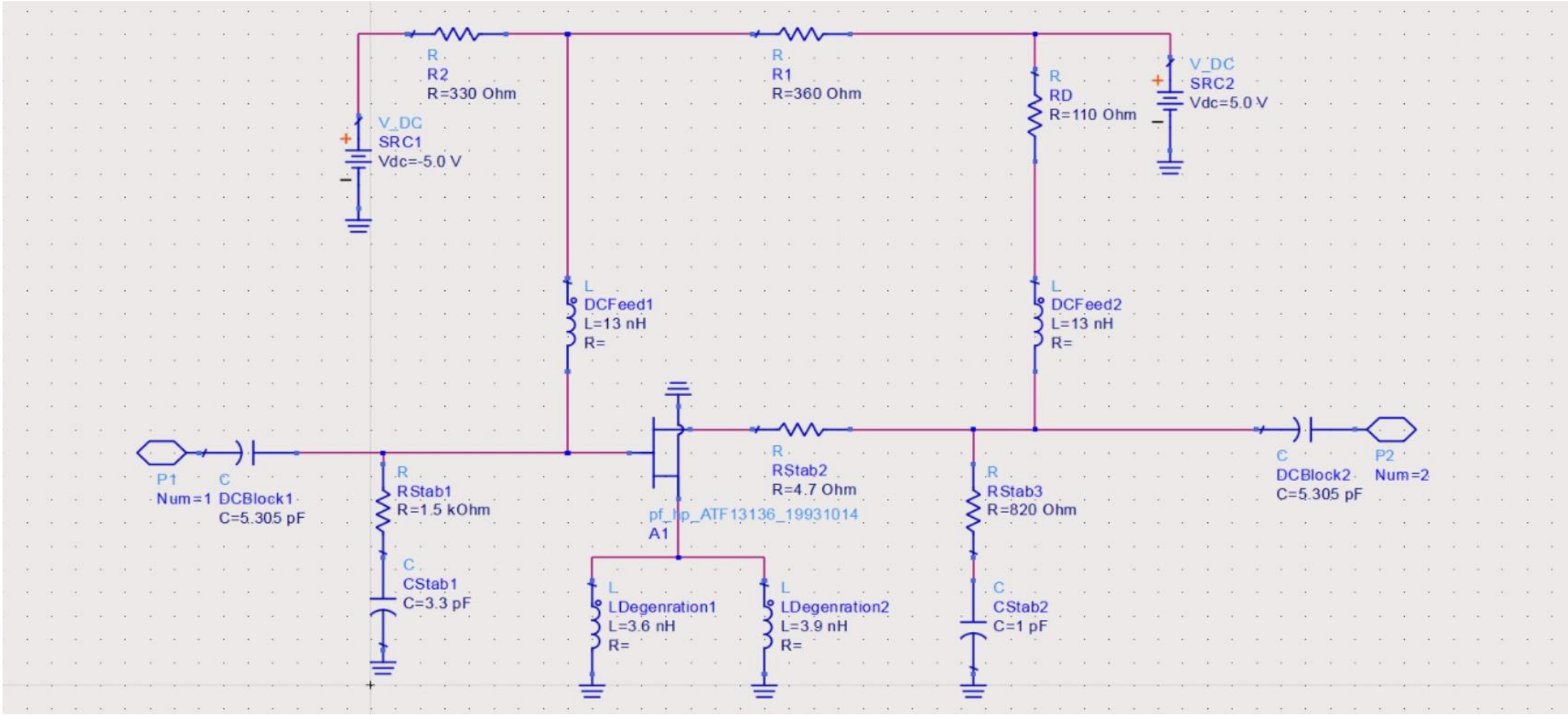

m1
ADS
m1
freq=6.000GHz
Mu1=1.097
MuPrime1=1.064
MuPrime1
Mu1


m3
ADS
m3
freq=6.000GHz
dB(S(1,1))=-4.415
dB(S(1,2))=-17.787
dB(S(2,1))=7.970
dB(S(2,2))=-6.370
dB(S(2,2))
dB(S(2,1))
dB(S(1,2))
dB(S(1,1))


m2
ADS
m2
freq=6.000GHz
StabFact1=1.079
StabFact1
freq, GHz


m4
ADS
m4
freq=6.000GHz
MaxGain1=11.166
MaxGain1
freq, GHz

Basic Amplifier



Low Noise Matching

Eqn GammaS = Sopt

Eqn Z0 = 50

Eqn Var1 = S(1,2) * S(2,1) * GammaS

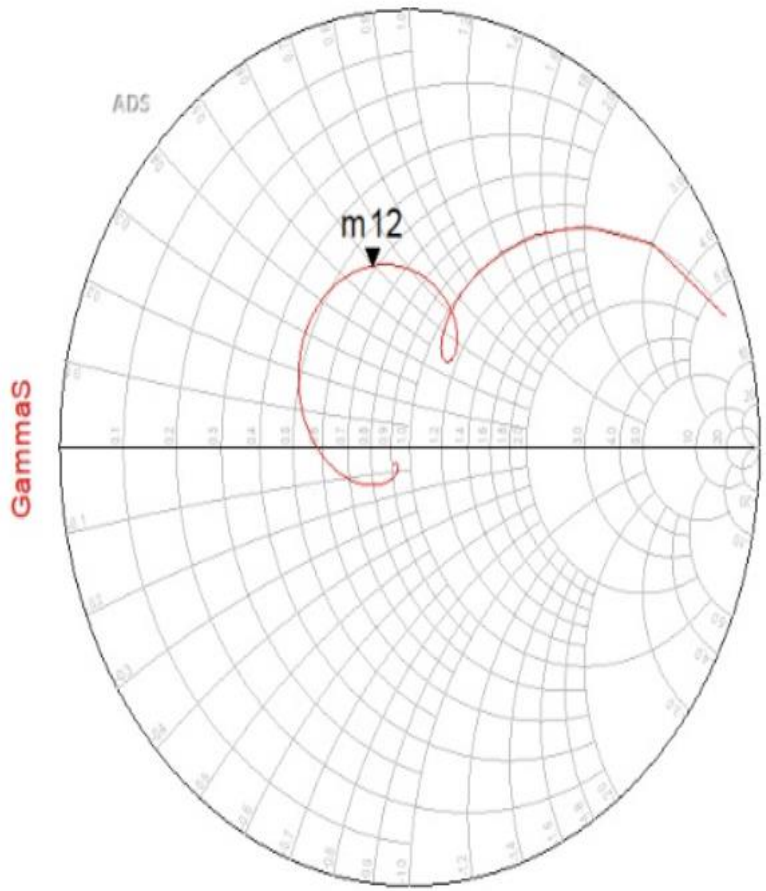
Eqn Var2 = 1 - (S(1,1) * GammaS)

Eqn Var = Var1 / Var2

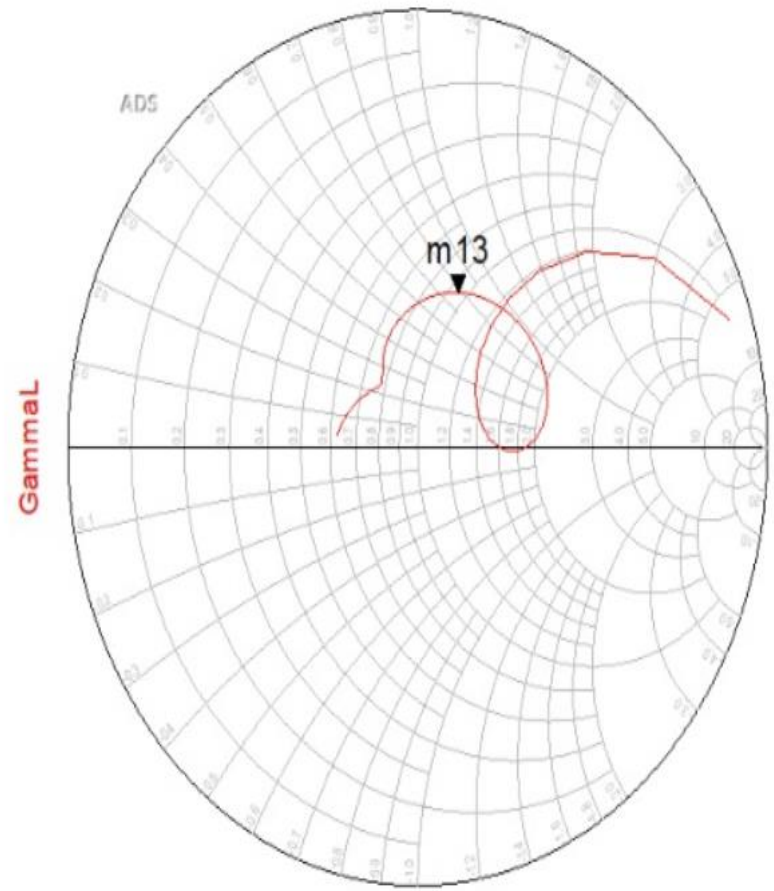
Eqn GammaOut = S(2,2) + Var

Eqn GammaL = conj(GammaOut)

m12
freq=6.000GHz
GammaS=0.428 / 104.294
impedance = Z0 * (0.585 + j0.595)



m13
freq=6.000GHz
GammaL=0.372 / 71.756
impedance = Z0 * (0.951 + j0.781)



Maximum Gain Matching

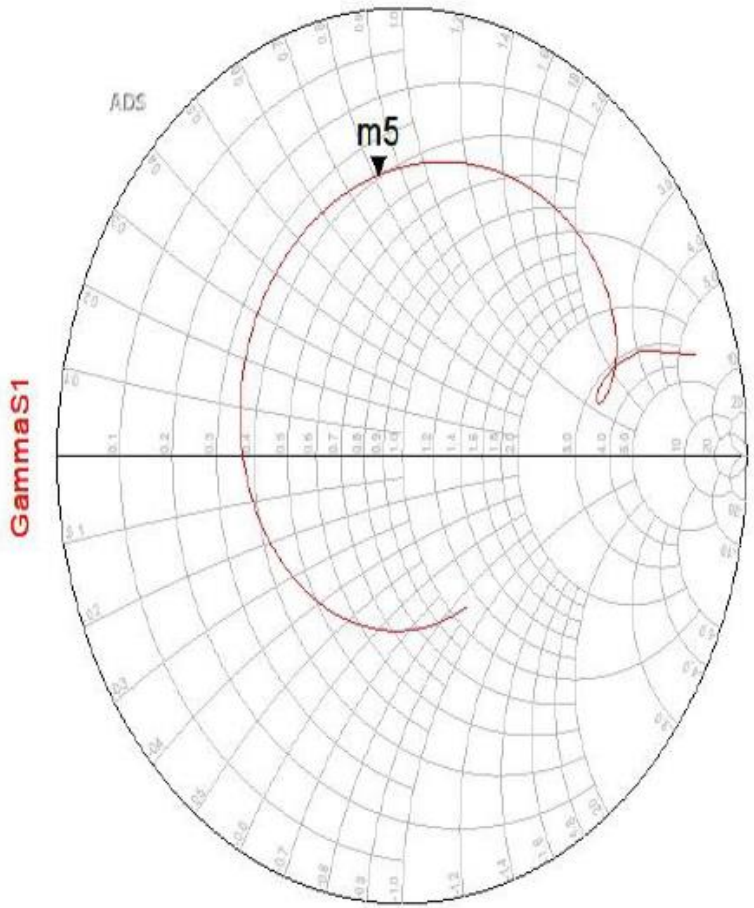
Eqn GammaS1=conj(S11)

Eqn Z1=50

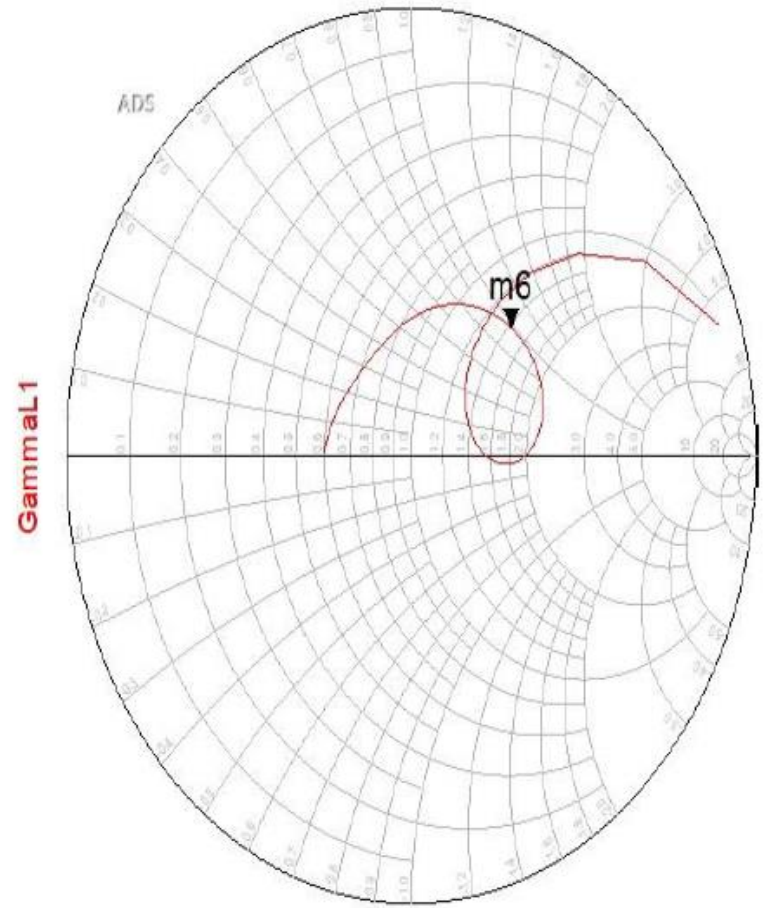
Eqn GammaOut1=S(2,2)

Eqn GammaL1=conj(GammaOut1)

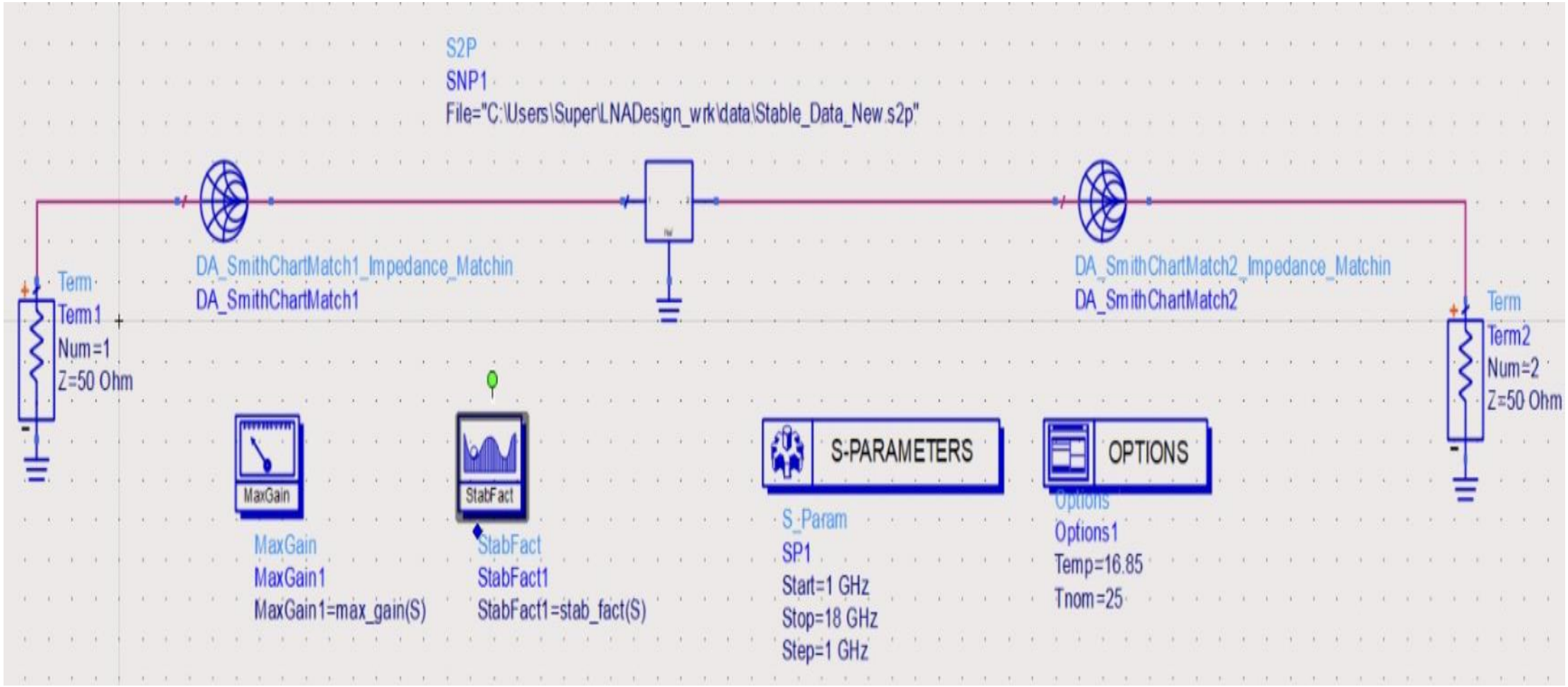
m5
freq=6.000GHz
GammaS1=0.630 / 96.218
impedance = Z0 * (0.393 + j0.817)



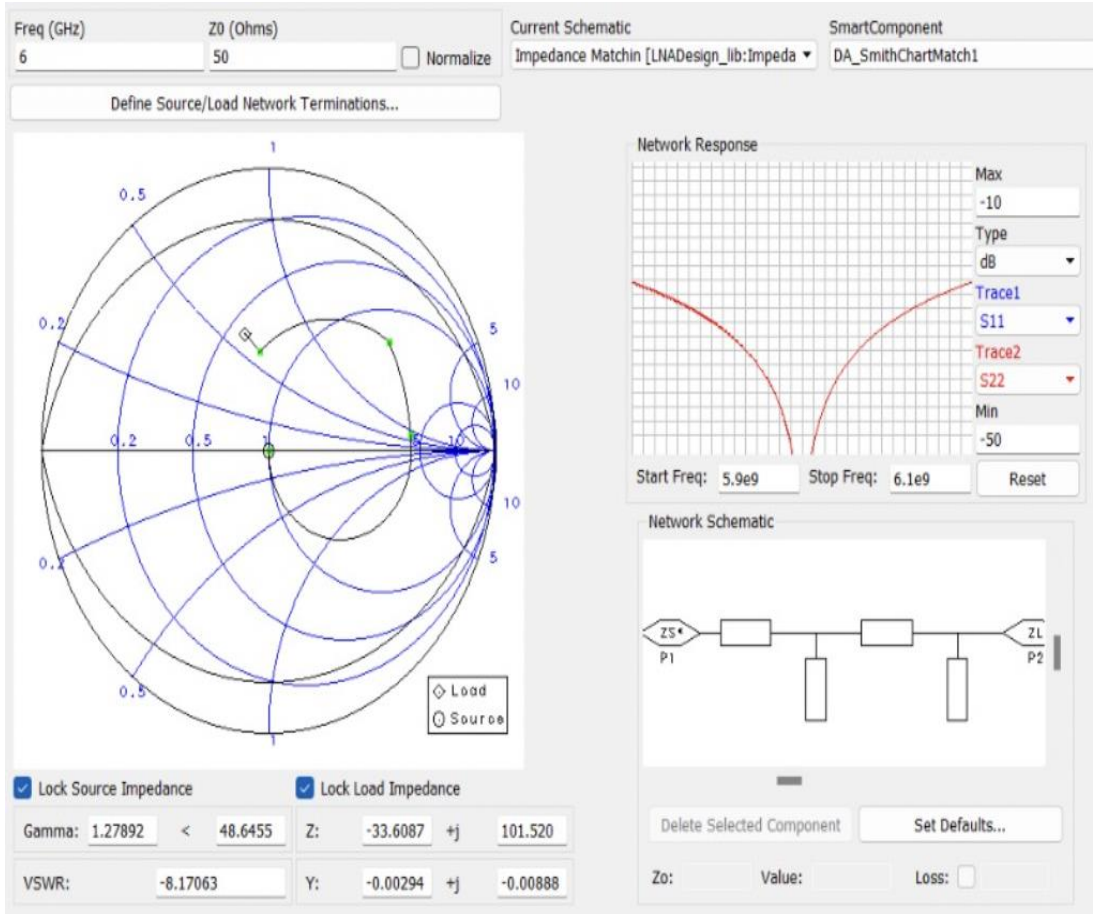
m6
freq=6.000GHz
GammaL1=0.407 / 44.554
impedance = Z0 * (1.425 + j0.977)

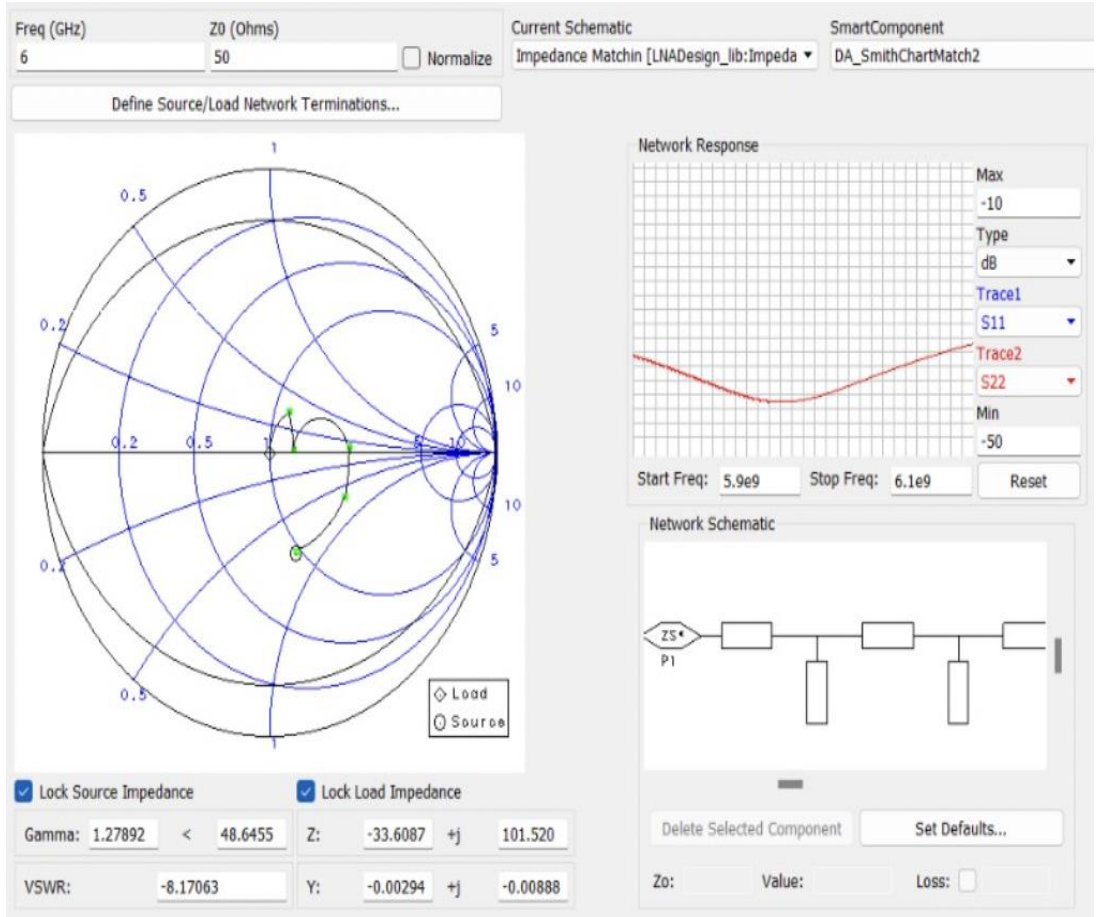


Design of Impedance Matching for Minimum Noise Amplifier

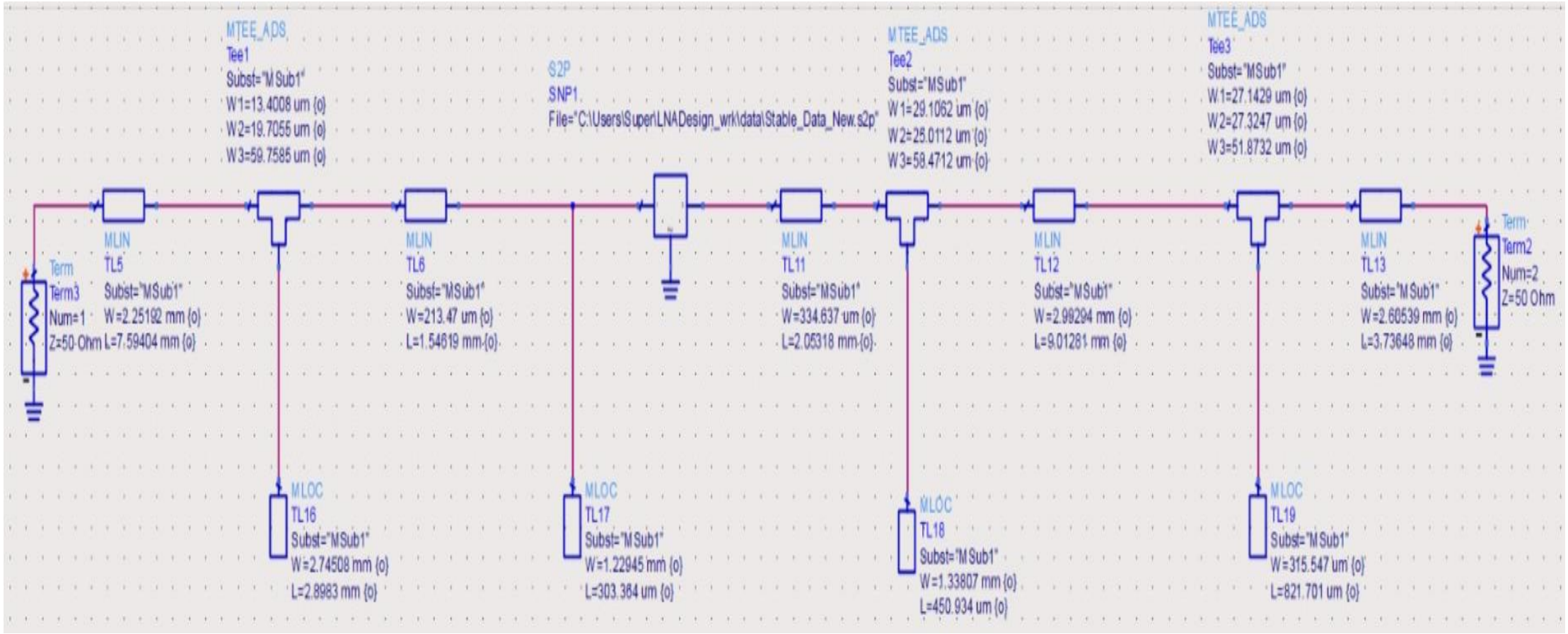


Impedance Matching Using Smith Chart

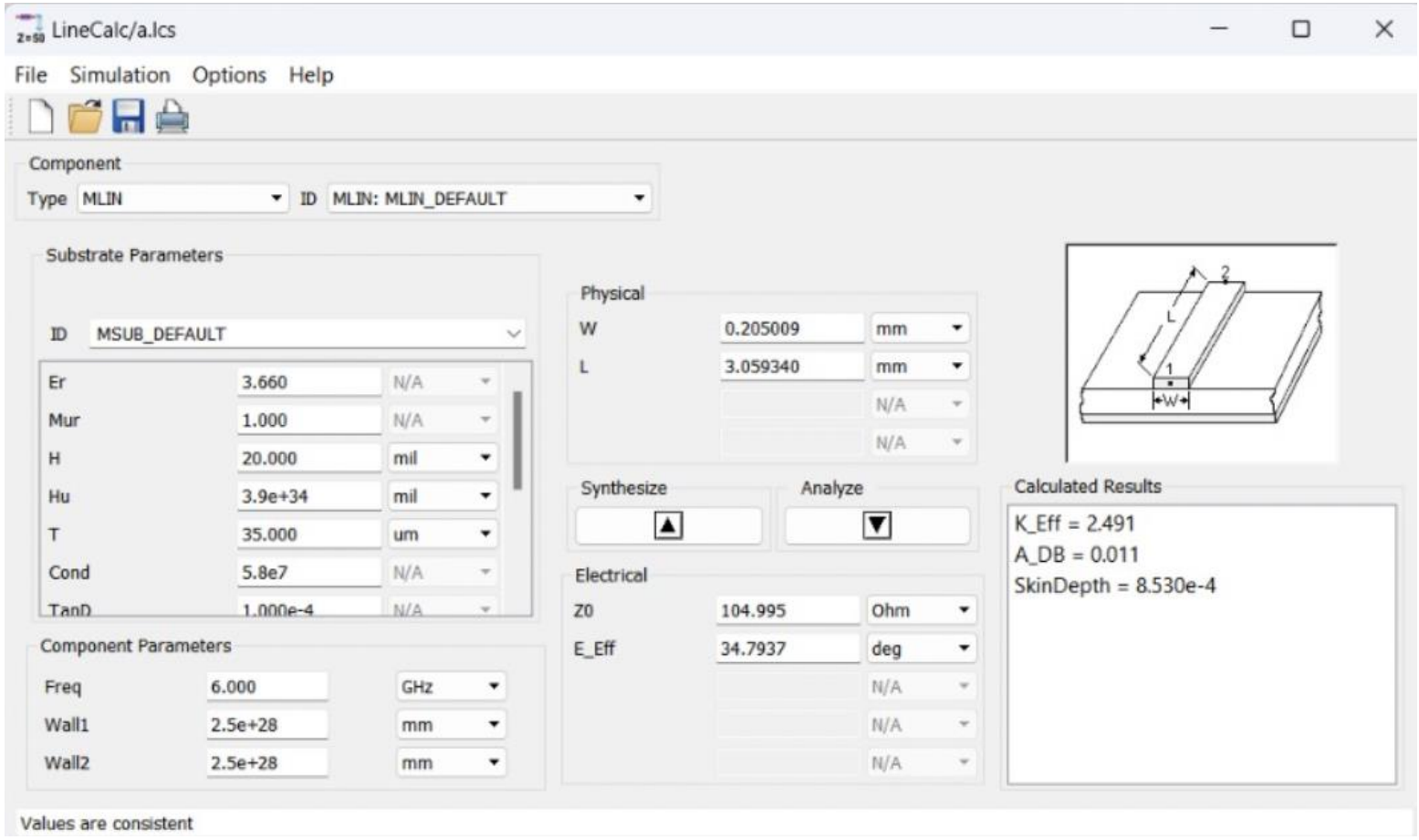




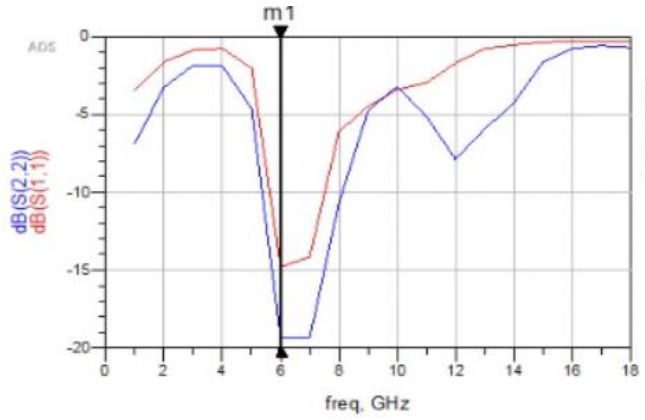
Replacing Ideal Transmission Lines using Microstrip Lines



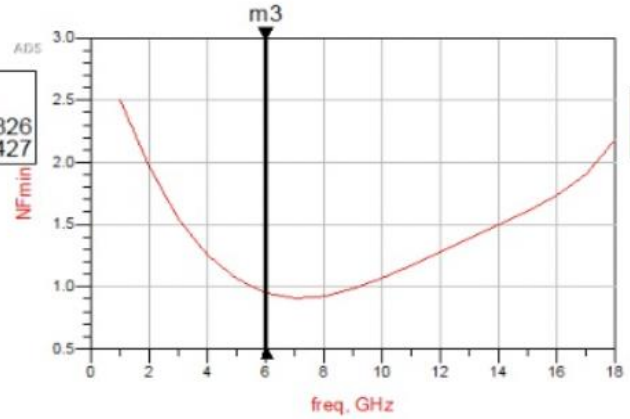
LineCalc is used to Calculate the Width and Length of the Microstrip Lines



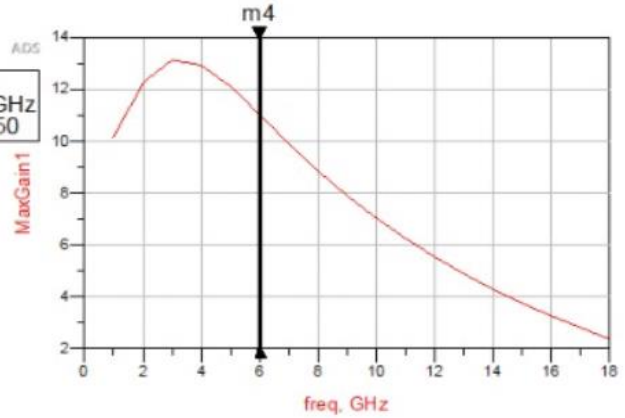
NF, Gain, Reflection Loss performance of the MNA



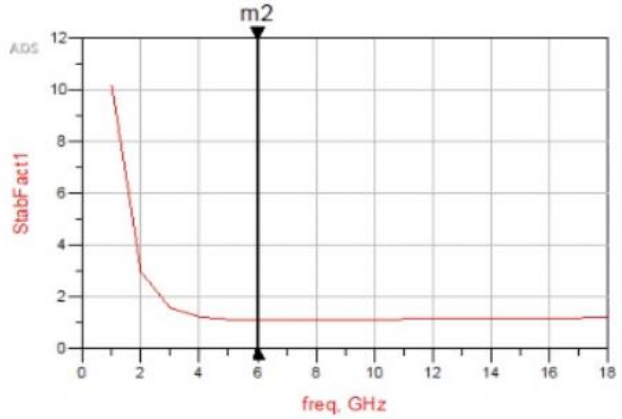
m1
freq=6.000GHz
dB(S(1,1))=-14.826
dB(S(2,2))=-19.427



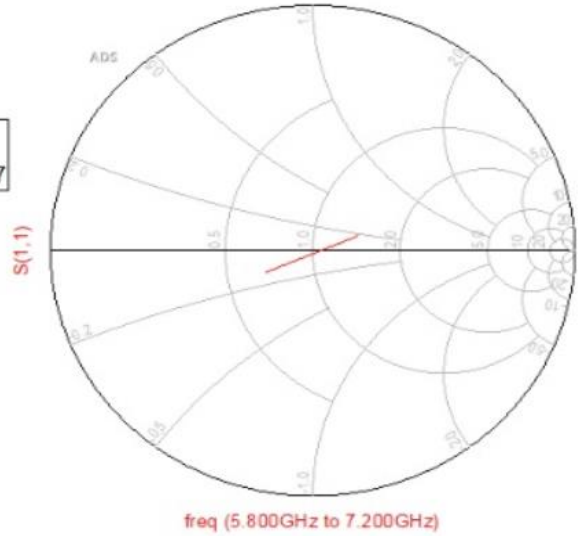
m3
freq=6.000GHz
NFmin=0.950

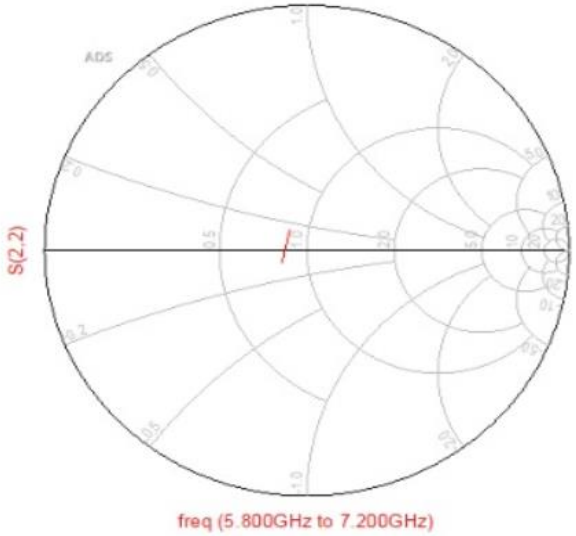


m4
freq=6.000GHz
MaxGain1=11.022

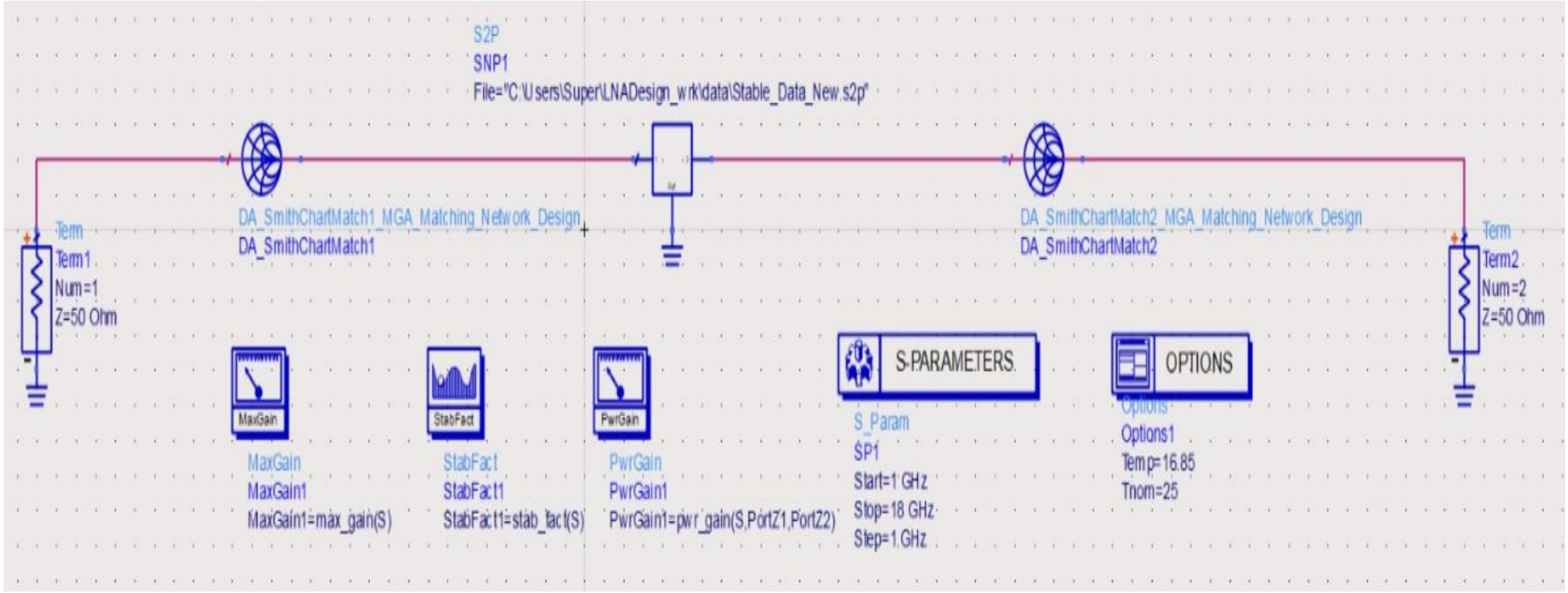


m2
freq=6.000GHz
StabFact1=1.107

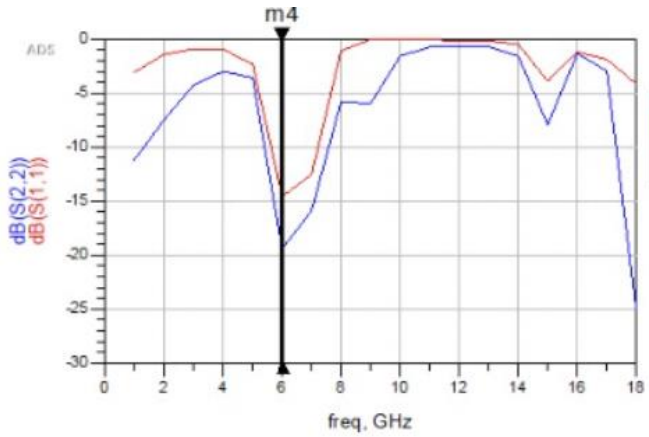




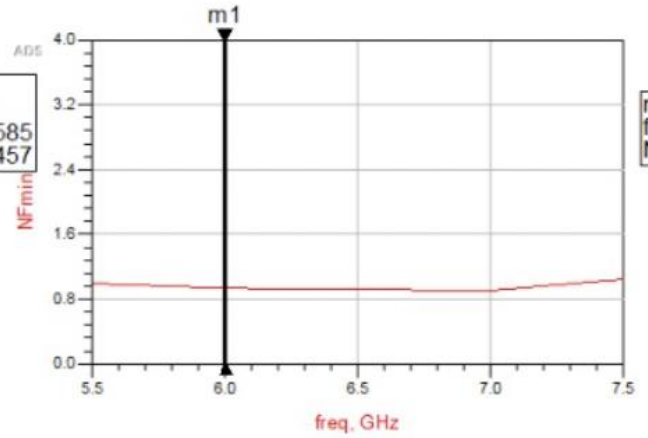
Matching Network Design of Maximum Gain Amplifier



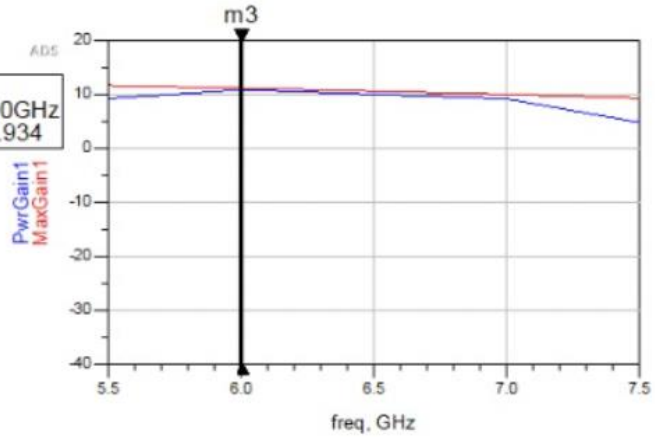
NF, Gain, Reflection Loss performance of the MGA



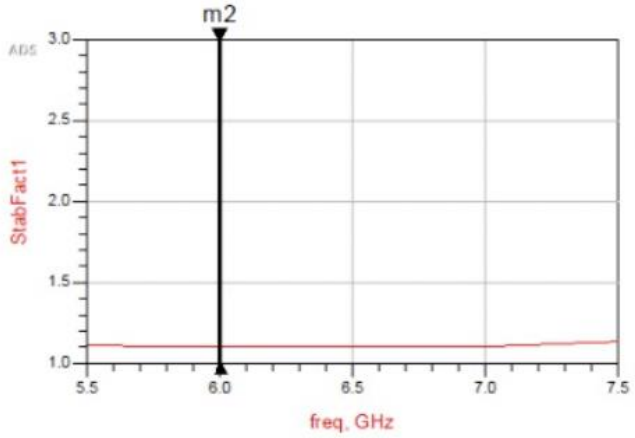
m4
freq=6.000GHz
dB(S(1,1))=-14.585
dB(S(2,2))=-19.457



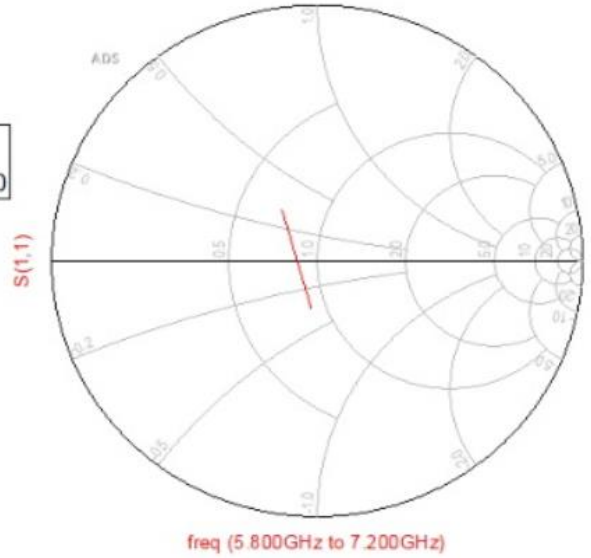
m1
freq=6.000GHz
NFmin=0.934

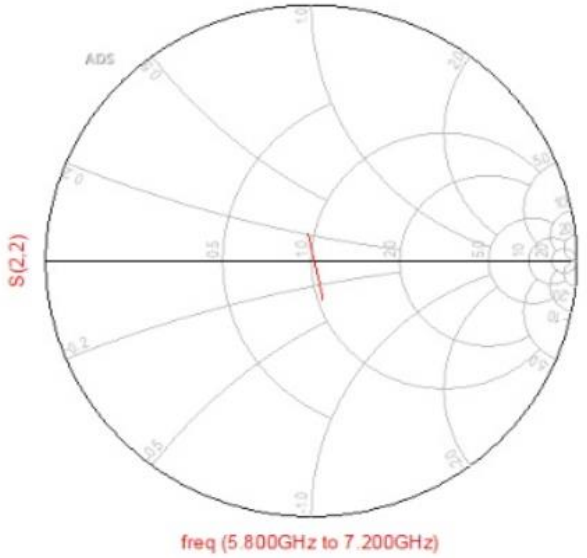


m3
freq=6.000GHz
MaxGain1=11.088
PwrGain1=10.786

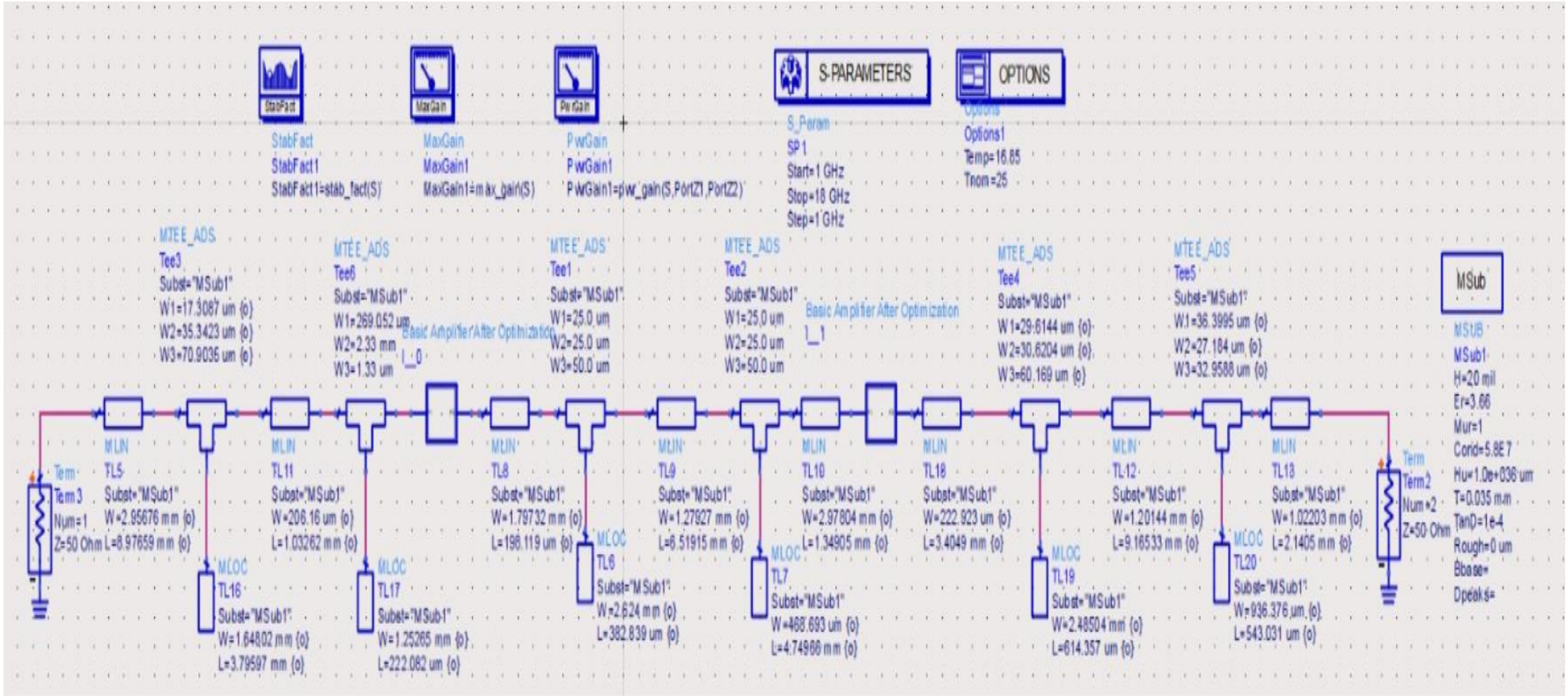


m2
freq=6.000GHz
StabFact1=1.100

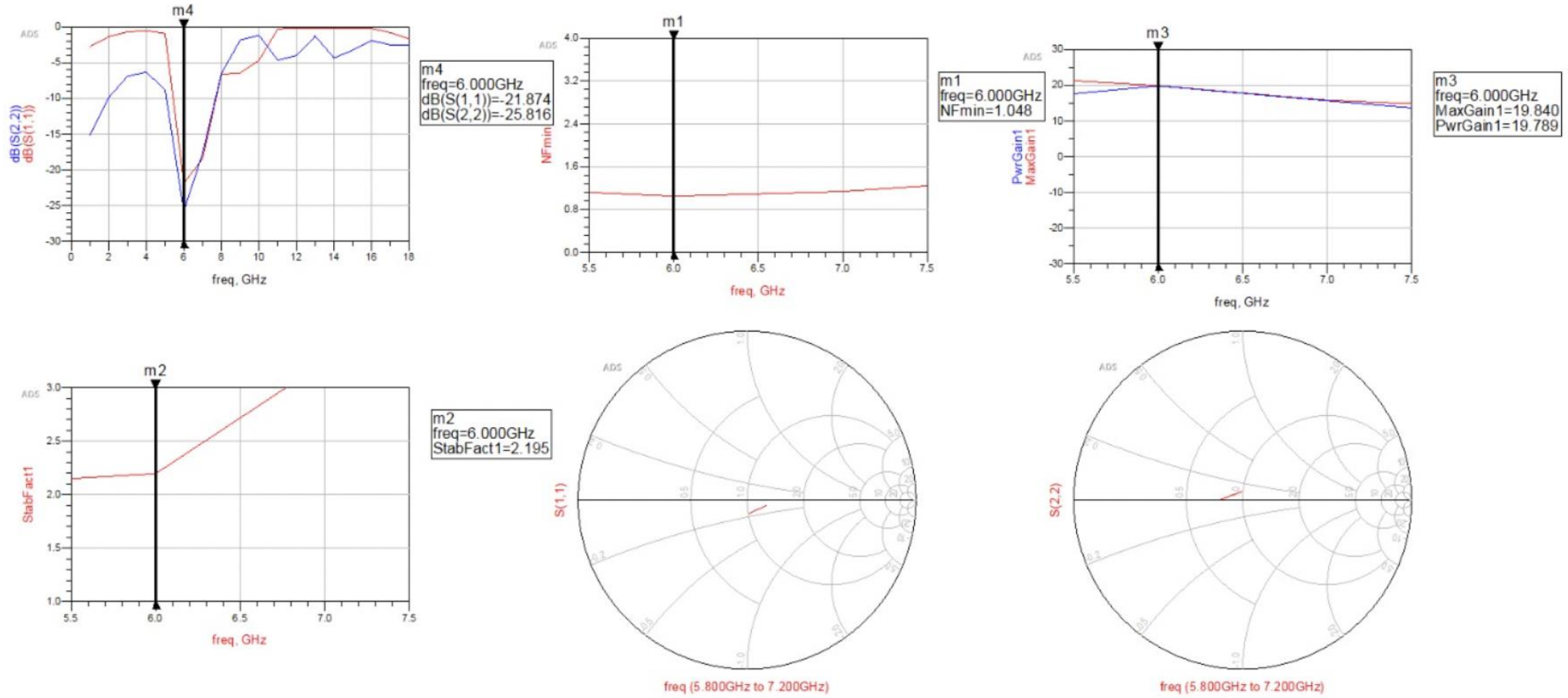




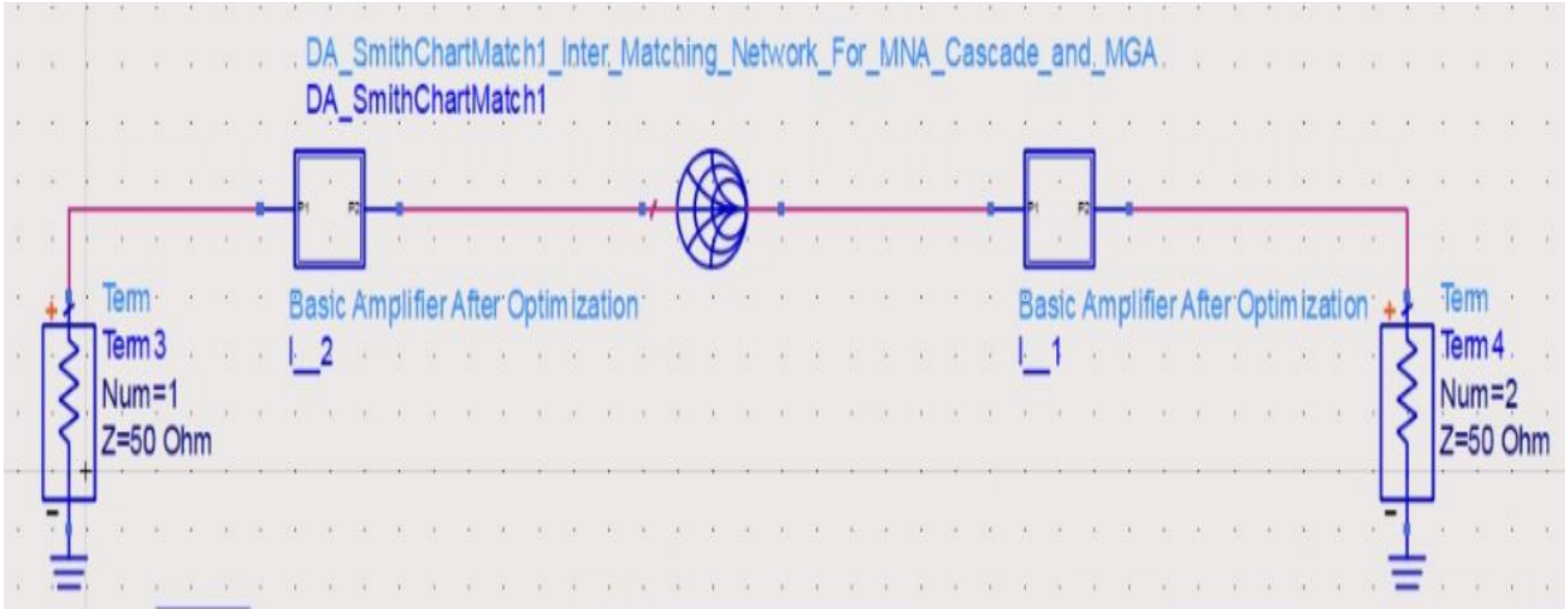
Cascaded Two Stage Minimum Noise Amplifier



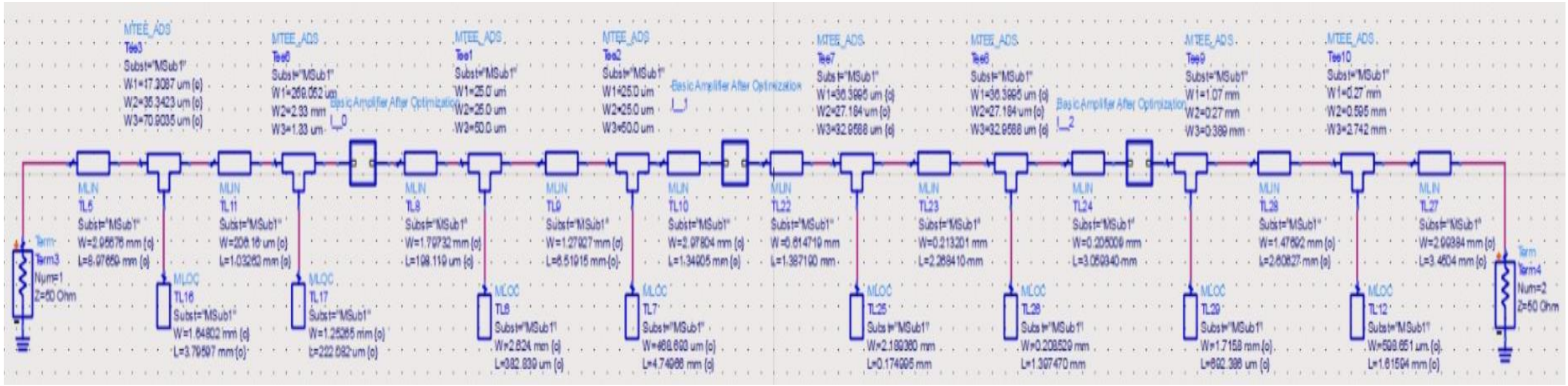
NF, Gain, Reflection Loss performance of the Cascaded MNA



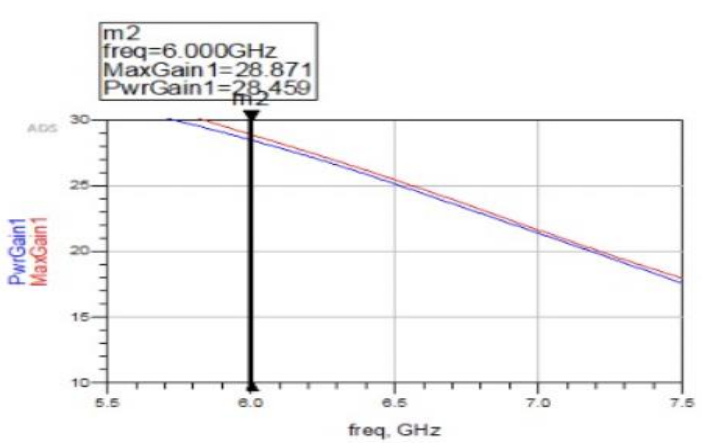
Interstage matching Network Design (Between Cascaded MNA and Final Stage MGA)

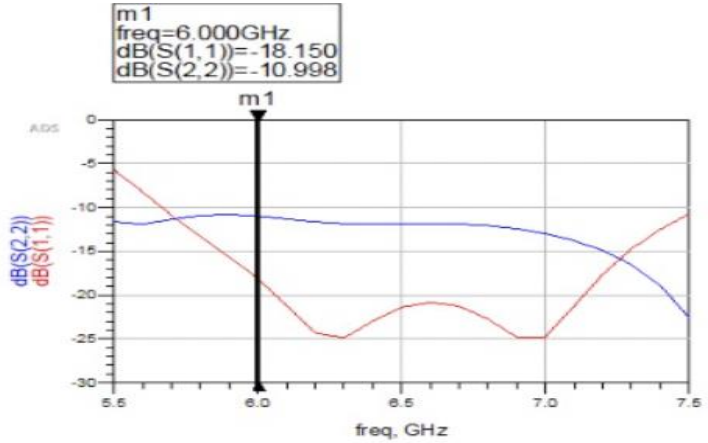


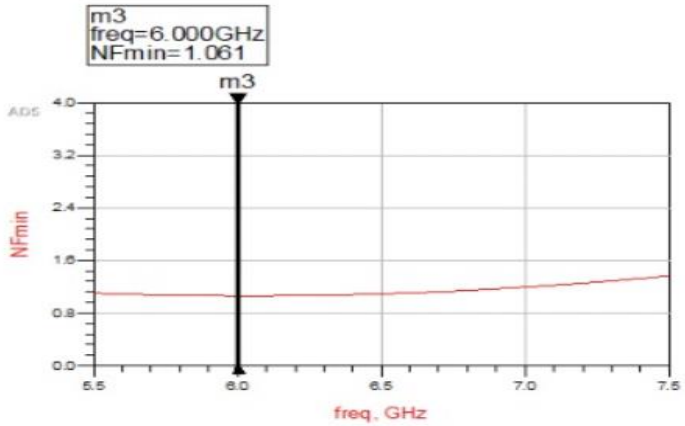
Final Low Noise Amplifier Design

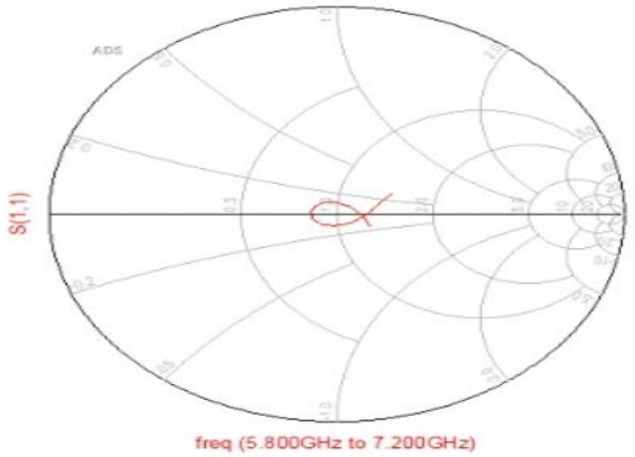


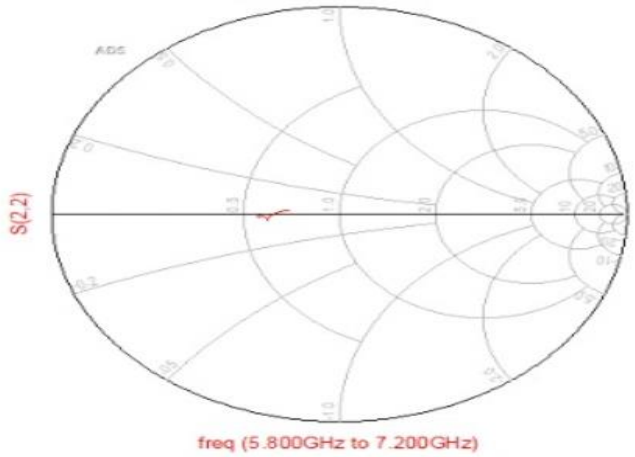
NF, Gain, Reflection Loss performance of the Overall LNA











Final Result

Parameter	Specified	Result Achieved
NF(min)	< 1.5 dB	1.061 dB
Maximum Gain (Max Gain)	25-28 dB	31.454 dB
Output Return Loss (S22)	< -15 dB	-18.150 dB

Conclusion

- A low noise amplifier is successfully designed by using a transistor model number ATF-13136.
- The initial two stages used Minimum Noise Amplifier design technique whereas the third stage used Maximum Gain Amplifier design technique.
- The ADS simulation outcomes as displayed in a Table (previous slide) shows that the Low Noise Amplifier at the frequency of 6 GHz met the design goals with a gain around 25-28 dB, a noise figure less than 1.5 dB, return loss (S22) less than -15dB.
- Distributed elements were the key elements in designing matching networks.
- The results are very close and comparable to each other.


ANY
QUESTIONS
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