

LOW NOISE AMPLIFIER DESIGN FOR WLAN

IEEE 802.11ax STANDARDS

A PROJECT REPORT

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INTERNAL EXAMINAR

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ABSTRACT

Low-noise amplifiers (LNAs) are critically important in microwave/WLAN receiver systems. LNAs are essential for boosting weak signals with minimal noise contribution, critical in various communication and measurement systems. In this project, a microwave three-stage LNA has been developed. Our design goal is to design an LNA whose transducer gain is between 18-20 dB, noise figure is less than 1.5 dB, and return loss is greater than 15 dB across 5.8-7.2 GHz frequency band. LNAs are critical components in high-sensitivity wireless communication systems. In this project, a transistor, with code ATF-13136 at the operating point ($V_{ds} = 2.5$ V, $I_d = 24$ mA), is selected as an active device for the key amplification device. A bias circuit is designed and added to the transistor. With the help of Smith Chart, the ideal input matching network, output matching network, and the inter-stage network are developed based on the S parameters of the transistor together with the bias circuit at the central frequency of 6GHz. Then the ideal three-stage LNA is implemented by synthesizing them together. Based on the ideal design, the practical three-stage LNA is developed in 5.8-7.2 GHz. The details of the dimensions for components, as micro-strip lines, are presented. Our entire design is analyzed, developed and optimized in the environment of Advanced Design System.

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LIST OF ABBREVIATIONS

ABBREVIATIONS EXPANSIONS

AC	Alternating Current
BJT	Bipolar Junction Transistor
C	Capacitor
CG Topology	Common Gate Topology
CS Topology	Common Source Topology
DC	Direct Current
ESC	Electronic Smith Chart
FET	Field Effect Transistor
GaAs	Gallium Arsenide
HBT	Heterojunction Bipolar Transistor
IDS	Drain to Source Current
K	Stability Factor
L	Inductor
LNA	Low Noise Amplifiers
MGA	Maximum Gain Amplifiers
MNA	Minimum Noise Amplifiers

MMIC	Monolithic Microwave Integrated Circuits
NF	Noise Factor
Q-point	Quiescent-Point
R	Resistor
RF	Radio Frequency
SiGe	Silicon Germanium
S Parameters	Scattering Parameters
S2p file	Touchstone File
VDS	Drain to Source Voltage
VGS	Gate to Source Voltage
WLAN	Wireless Local Area Network
Δ	Delta
μ	Mu-Factor

Chapter 1

INTRODUCTION

In this chapter, we firstly introduce the importance and role of LNA, in other words, where and why the LNA is used. Secondly, we describe the concepts of the key parameters for design LNA, like Gain, Noise Figure, Stability, Central Frequency and Bandwidth, which are important in theory for design.

1.1 THE ROLE OF LNA

Low Noise Amplifiers (LNAs) are critically important in microwave receiver systems. LNAs play a crucial role in microwave receiver systems as they help to enhance the sensitivity of the receiver by minimizing the amount of noise generated during signal amplification. Microwave signals received from antennas are typically too weak to undergo further operations, such as demodulation, without amplification. However, if the amplifier produces noise at a level similar to or higher than the signal being amplified, it becomes challenging to differentiate between the signal and noise. Therefore, the use of LNAs with low noise is necessary to reduce the impact of noise in the receiver system.

LNAs are placed at the beginning of the receiver system, where they amplify the expected signal, producing a more significant difference between the signal and noise compared to conventional amplifiers. Even when additional noise is introduced in the following components, such as mixers, the amplified signal will remain unaffected. LNA amplifiers are extensively used in various microwave communication applications, including GPS receivers, cellular phones, wireless LANs, and satellite communication systems.

1.2 LNA TOPOLOGY

A basic LNA topology consists of blocks as an amplifier device (transistor), biased device, input matching network, output matching network as in Figure 1:

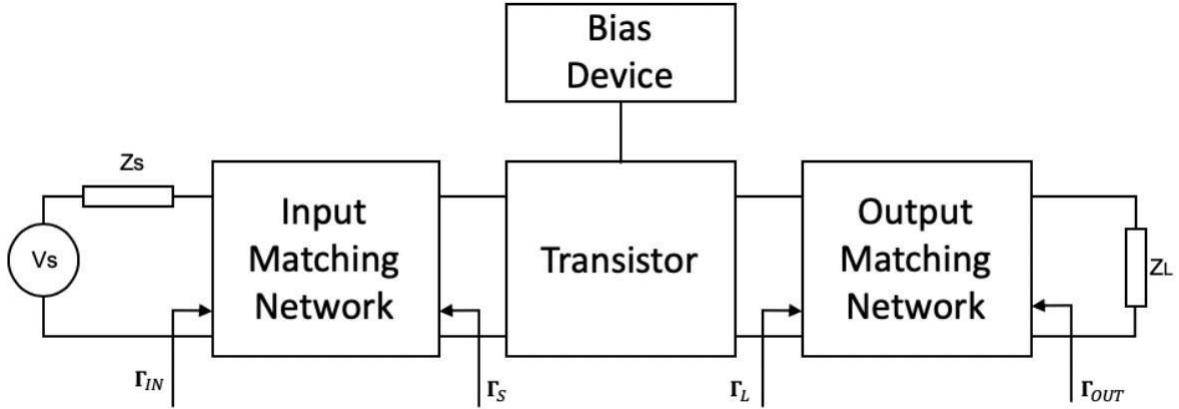


Figure 1 - LNA System Topology

1.3 LNA PARAMETERS

The critical parameters to consider when designing a LNA are gain, noise figure, and input/output impedance. These factors determine the level of amplification, noise added to the signal, and matching between the LNA and the preceding/following circuits, respectively, impacting overall LNA performance.

1.3.1 Transducer Gain

Transducer Gain is an index to quantitatively describe the amplification level of one LNA. Transducer Gain (GT) is defined as the ratio between the power delivered to the load by the amplifier (PL) and the power available from the source (PA):

$$G_T = \frac{P_L}{P_A} \quad (1)$$

For a practical LNA, the gain is measured with the source and load impedance both of 50 Ohm as customary. Considering an amplifier as a two-port network

as in Figure 2, the expression for the GT can be derived as:

$$G_T = |S_{21}|^2 \frac{(1 - |\Gamma_S|^2)(1 - |\Gamma_L|^2)}{|(1 - \Gamma_S S_{11})(1 - \Gamma_L S_{22}) - \Gamma_S \Gamma_L S_{12} S_{21}|^2} \quad (2)$$

Also, the reflection coefficients at input and output can be evaluated:

$$\Gamma_{IN} = S_{11} + \frac{S_{12} S_{21} \Gamma_L}{1 - S_{22} \Gamma_L} \quad \Gamma_{OUT} = S_{22} + \frac{S_{12} S_{21} \Gamma_S}{1 - S_{11} \Gamma_S} \quad (3)$$

where:

- $S_{11}, S_{12}, S_{21}, S_{22}$ are the device S-parameters;
- Γ_S and Γ_L are the reflection coefficients at source and load respectively

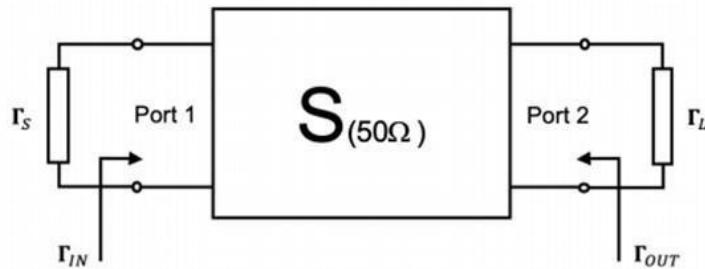


Figure 2 - Amplifier as Two-Port Network

1.3.2 Noise Figure

Thermal noise, shot noise, and flicker noise are the main sources of Electronic Noise. Thermal noise is always associated with dissipation phenomena produced by currents and voltages. It is represented by a voltage or current source randomly variable in time. Shot noise arises typically in PN junctions forwardly biased; it is due to the discrete nature of current through the junction, which results randomly variant around the imposed bias value.

Flicker noise arises in semiconductor devices, due to impurities and defects in the crystal structure. In microwave devices, the noise is characterized as Noise

Figure (NF). The expression of noise in a two-port network as Figure 3, the Noise Figure is defined as the ratio between PN out and Ga PN in, namely

$$NF = \frac{P_{Nout}}{G_a \cdot P_{Nin}} \quad (4)$$

Where:

- PN out is the actual noise power at the output;
- Ga is the available power;
- GaPN in is the noise power at output if the 2-port would not add noise power

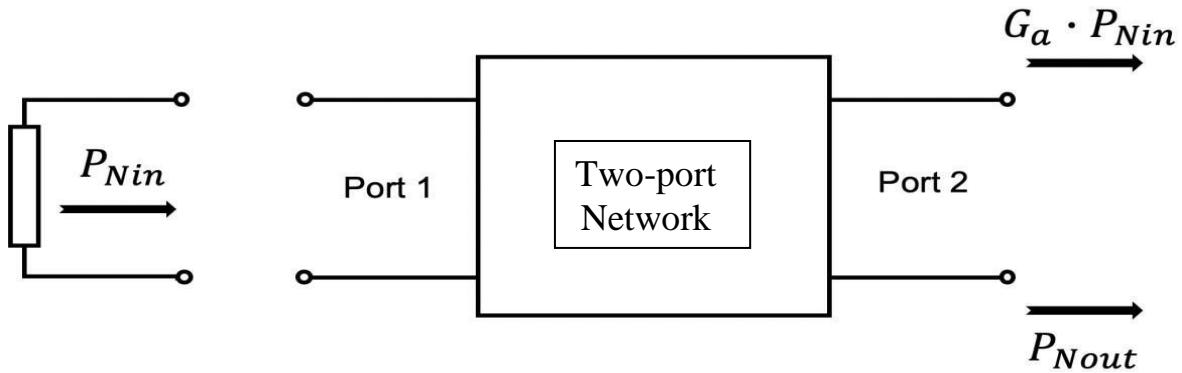


Figure 3 - Noise Power in a Two-Port Network

In practice, NF is a function of frequency, so the above powers must be assumed per unit band, such as the power densities. Moreover, NF also depends on the source impedance. More often, the noise figure is expressed in decibels (in dB) NFdb as,

$$NF_{db} = 10 \log NF \quad (5)$$

We can get the noise figure as the expression of Γ_S , reflection coefficient of the source, given by

$$NF = (NF)_{min} + 4r_n \frac{|\Gamma_S - \Gamma_{min}|^2}{|1 + \Gamma_{min}|^2 \cdot (1 + |\Gamma_S|^2)} \quad (6)$$

where:

- (NF)_{min} is the minimum value of NF;

- Γ_{min} is the value of Γ_S which determines $NF = NF_{min}$;
- r_n is the normalized noise resistance.

All these parameters are frequency-dependent. Typically, they are made directly into .s2p data files. The data files are provided available as references for commercial devices by manufacturers or devices vendors.

If we plot the equation expressing NF as a function of Γ_S on the Smith Chart, an NF circle with a certain center and radius will be obtained. Together with the circle of the gain, the proper value of Γ_S can be selected within the common area of two circles.

For cascade stages as in Figure 4, the overall noise figure of the cascade stages network is expressed as

$$(NF)_{TOT} = NF_1 + \frac{NF_2 - 1}{G_{a1}} + \frac{NF_3 - 1}{G_{a1}G_{a2}} + \dots \quad (7)$$

where:

- G_{an} is the available power in the n stage, for $n=1,2,3\dots n$;
- NF_n is the noise figure in the n stages, for $n=1,2,3\dots n$.

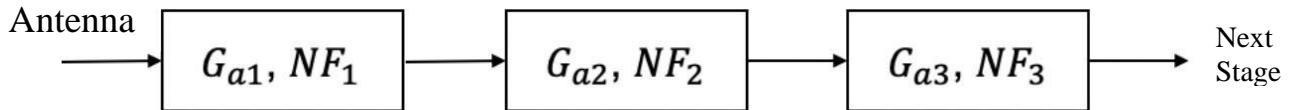


Figure 4 - Two-Port Network with Cascading Stages

It is important to point out that the noise figure is mainly determined by the first stage. So, for designing multiple-stage LNA, setting the LNA in the first stage

with the lowest NF is a wise design decision. The noise figure NF can be represented on the ΓS complex plane. The noise points with the same value, which is $NF = \text{constant}$, are on the same circle called the equal noise figure circle.

1.3.3 Stability

In certain radio frequency bands and certain impedance environments, amplifier is intending to oscillate. Stability shows how much is this tendency. For example, if we say an LNA is stable, it means the output signal remains a finite amplitude for an input exciting signal with finite amplitude. There are generally three types of stability, as unstable, potentially unstable and unconditionally stable. The oscillators make use of the property of being unstable. For amplifiers, they always work under the other two types of stability, potentially unstable and unconditionally stable. Unconditionally stable means that the amplifier is stable in whatever impedance environment. Potentially unstable means that the amplifier is stable only in certain impedance environments.

It is important that LNA maintains stable in required bandwidth with impedance through our design, which means the designed LNA will not behave like an oscillator. This can be achieved if we use stable techniques to impose the LNA to be unconditionally stable. Or even the LNA is potentially unstable, the input and output reflection coefficients fall in their stable admission regions respectively. To determine the stability of our amplifier, here we can use the stability factor K. Given the S parameters, the conditions $\Gamma_{in} < 1$, $\Gamma_{out} < 1$ whatever value of ΓS , ΓL if:

$$K = \frac{1 - |s_{11}|^2 - |s_{22}|^2 + |s_{11} \cdot s_{22} - s_{12} \cdot s_{21}|^2}{2|s_{12} \cdot s_{21}|^2} > 1, \det S < 1 \quad (8)$$

If these equations are verified, the two-port is unconditionally stable. When $K < 1$, the admissible values of ΓS , ΓL must, however, satisfy the conditions

$$|\Gamma_{in}| = |s_{11} + \frac{s_{21}s_{12}\Gamma_L}{1 - s_{22}\Gamma_L}| < 1 \quad |\Gamma_{out}| = |s_{22} + \frac{s_{21}s_{12}\Gamma_S}{1 - s_{11}\Gamma_S}| < 1 \quad (9)$$

These constraints, which can be represented graphically on the Smith Chart, allow to identify the admissible values of Γ_S , Γ_L .

By setting the ‘less than’ symbol to ‘equal’ symbol in Equation 12, we can obtain the circles which define the boundary between the admissible and not admissible regions. To identify which of the two is the stable region the values Γ_{in} (Γ_{out}) for $(\Gamma L(\Gamma S) = 0)$ must be observed. Taking into account that $\Gamma_{in}(\Gamma_{out})$ coincides in this case with $s_{11}(s_{22})$, it has:

The stable region for $\Gamma L(\Gamma S)$ is outside the instability circle if:

- $|s_{11}|(|s_{22}|) < 1$ and the circle does not enclose the centre of the chart
- $|s_{11}|(|s_{22}|) > 1$ and the circle encloses the centre of the chart

The stable region for $\Gamma L(\Gamma S)$ is inside the instability circle if:

- $|s_{11}|(|s_{22}|) > 1$ and the circle does not enclose the centre of the chart
- $|s_{11}|(|s_{22}|) < 1$ and the circle encloses the centre of the chart

1.3.4 Central Frequency and passband

The central frequency is the frequency in which the LNA works. With different devices and for different purposes, it can be set to hundreds of 106 Hz, or even higher in the microwave band. Central frequency is one of the main indicators of the low-noise amplifier. It is one of the basic references for selecting the proper active device and is on x-axis for displaying graphically some specifications of the circuit components during the design process. For the passband, to ensure that the signal passes through the amplifying circuit without

distortion, the value of the gain must be limited in a range around the central frequency. The passband is the bandwidth of this range.

1.4 Background about LNA Design

For LNA designs, the available gain design approach is typically utilized to facilitate a gain versus noise “trade-off”. Most applications do not allow or necessarily require a minimum noise design since gain is reduced to allow for the lower noise performance. Thus, a gain versus noise “trade-off” is appropriate. Knowledge about the system in which the amplifier is to be used is required to make the appropriate gain versus noise trade-off. If subsequent stages following the RF amplifier have a high cumulative noise figure, more gain is required to “take-over” the noise figure of those stages, thus providing the lowest possible system noise. An example system is shown in Figure 5. System Noise Figure is calculated using the Friis formula as follows:

$$F_T = F_1 + \frac{F_2 - 1}{g_1} + \frac{F_3 - 1}{g_1 g_2} + \dots + \frac{F_n - 1}{g_1 g_2 \dots g_{n-1}} \quad (10)$$

where: FT is the total system Noise Figure,

F1 is the Noise Figure of stage one,

F2 is the Noise Figure of stage two,

Fn is the Noise Figure of stage number n.

g1 is the numeric gain factor of stage one,

g2 is the numeric gain factor of stage two,

gn-1 is the numeric gain factor of the second to the last stage.

LNAs are critical components in modern communication systems, providing amplification with minimal added noise. LNA design involves optimizing transistor selection, biasing, and matching networks to achieve high

gain and low noise figure. Factors such as stability, linearity, and power consumption must also be considered.

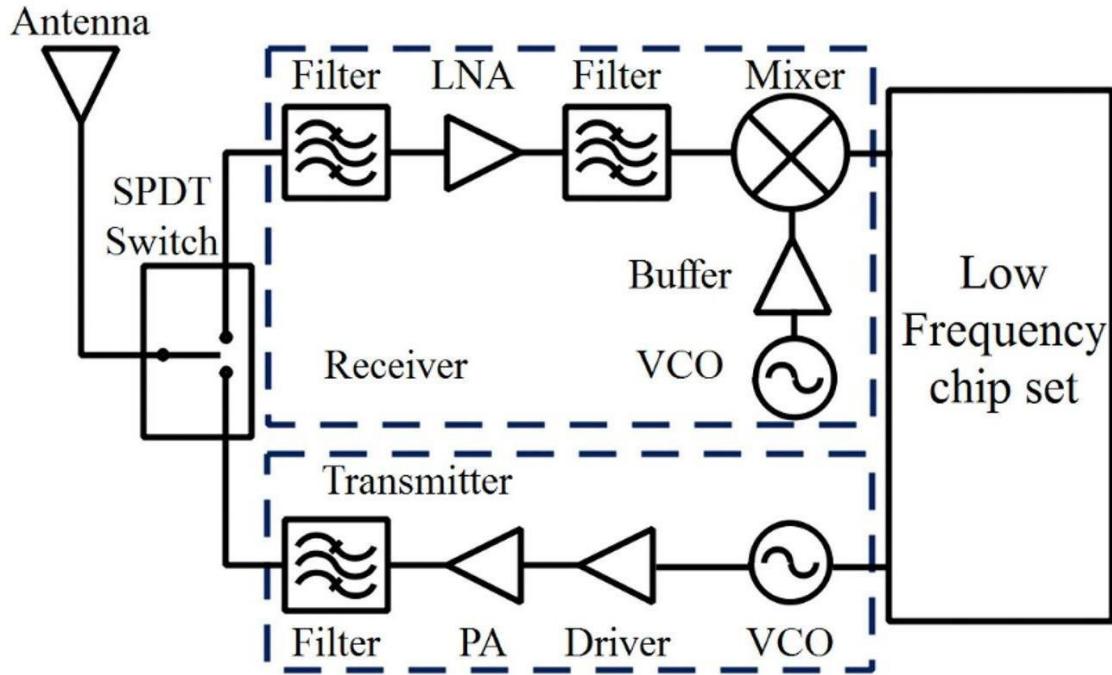


Figure 5 - LNA Blocks

Based on Equation 10, earlier gain stages diminish the effect of cumulative noise added by stages farther back in the system. Thus, trading away too much gain for lower noise figure in the early stages of the system may degrade the overall system noise due to less noise “take-over” of the following stages.

Equations 11 and 12, respectively, convert noise figure, NF in dB, to numeric Noise Figure, F and gain, G in dB to gain factor, g:

$$F = 10^{\frac{NF}{10}} \quad (11)$$

$$g = 10^{\frac{G}{10}} \quad (12)$$

Equations 13 and 14 respectively, convert Noise Figure, F to noise figure, NF in dB, and gain factor, g to gain, G in dB:

$$NF = 10 \log F \quad (13)$$

$$G = 10 \log(g) \quad (14)$$

1.4.1 Available Gain Procedure

For LNA design, the available gain design approach is typically performed. When performing the available gain design procedure, the source termination is constrained to some arbitrary impedance (usually for better noise performance), and the resulting output reflection coefficient of the device is conjugately matched. Thus, a mismatch may exist at the input whereas the output is perfectly matched. If a mismatch exists at the device input, the amount of gain is less than the maximum possible gain as is the case when both input and output are conjugately matched. To determine the amount of available gain with the input mismatched, Equation 2 is modified. Since the output is conjugately matched for a given source termination, Γ_{OUT} is expressed in terms of Γ_S and the two-port s-parameters. By substitution and rearrangement, this also allows Equation 2 to be expressed in terms of Γ_S and the two-port s-parameters. The available gain design procedure is applicable to both the conditionally stable and unconditionally stable cases. This amplifier design procedure examines the unconditionally stable case only.

The transducer gain equation g_T of Equation 2, is rearranged as shown in Equations 15 and 16:

$$g_T = \frac{1 - |\Gamma_s|^2}{|1 - S_{11}\Gamma_s|^2} |S_{21}|^2 \frac{1 - |\Gamma_L|^2}{|1 - \Gamma_{OUT}\Gamma_L|^2} \quad (15)$$

Where:

$$\Gamma_{OUT} = S_{22} + \frac{S_{21}S_{12}\Gamma_s}{1 - S_{11}\Gamma_s} \quad (16)$$

When the device output is conjugately matched for a given source termination Γ_S , then transducer gain, g_T , is simplified in terms of the s-parameters and Γ_S .

Conjugately matching the output mathematically yields $\Gamma_L = \Gamma_{OUT}^*$ and Equation 17 yields available gain, g_A :

$$g_A = \frac{1 - |\Gamma_s|^2}{|1 - S_{11}\Gamma_s|^2} |S_{21}|^2 \frac{1}{1 - |\Gamma_{OUT}|^2} \quad (17)$$

Substituting Equation 16 into Equation 17 yields the available gain equation, g_A , as shown in Equation 18, which is a function of Γ_S and the two-port s-parameters.

$$g_A = \frac{|S_{21}|^2(1 - |\Gamma_s|^2)}{\left(1 - \left|\frac{S_{22} - \Delta\Gamma_s}{1 - S_{11}\Gamma_s}\right|^2\right) |1 - S_{11}\Gamma_s|^2} \quad (18)$$

A family of circles known as available gain circles are constructed that provide a specific amount of mismatch at the device input. An infinite number of source terminations forming the circle allow selection of mismatch at the device input. To construct an available gain circle, locate the center of the circle on a Smith chart and draw the circumference from a calculated radius. Locate the center for a particular gain circle using Equation 22, which yields a magnitude and angle.

The desired available gain in dB is converted to numeric gain factor g_A for Equation 19. Equation 19 is then used in Equations 21 and 22.

$$g_a = \frac{g_A}{|S_{21}|^2} \quad (19)$$

$$C_1 = S_{11} - \Delta S_{22}^* \quad (20)$$

The radius of an available gain circle is calculated by equation 21:

$$R_a = \frac{[1 - 2K|S_{12}S_{21}|g_a + |S_{12}S_{21}|^2g_a^2]^{1/2}}{1 + g_a(|S_{11}|^2 - |\Delta|^2)} \quad (21)$$

$$C_a = \frac{g_a C_1^*}{1 + g_a(|S_{11}|^2 - |\Delta|^2)} \quad (22)$$

Plotting available gain circles in conjunction with noise contours allows an easy selection of gain versus noise figure for the amplifier.

1.4.2 Noise Figure Design Procedure

Equation 23 describes transistor Noise Figure performance. As shown in this equation, transistor noise performance is independent of load termination and is determined solely by its source termination and noise parameters. The noise parameters fully describe the noise performance of a device for a specific set of conditions such as frequency, bias, and temperature.

$$F = F_{Min} + \frac{4r_n|\Gamma_s - \Gamma_{opt}|^2}{(1 - |\Gamma_s|^2)(1 + |\Gamma_{opt}|^2)} \quad (23)$$

Transistor Noise Figure F is a function of Γ_S , FMin, r_n , and Γ_{opt} , where FMin, r_n , and Γ_{opt} are known as the transistor noise parameters. Γ_S terminates the two-port input of Figure 2. As Γ_S approaches Γ_{opt} , the transistor Noise Figure approaches its minimum. As Γ_S departs from Γ_{opt} , the Noise Figure increases from its minimum value. The rate at which the Noise Figure increases depends on the noise resistance r_n . Conversion of transistor Noise Figure to noise figure in dB is obtained from Equation 13. Equation 24 obtains the noise resistancern if FMin, Γ_{opt} , and the Noise Figure with the input terminated in 50Ω is known.
($\Gamma_S = 0$)

$$r_n = (F_{\Gamma_s=0} - F_{min}) \frac{|1 + \Gamma_{opt}|^2}{4|\Gamma_{opt}|^2} \quad (24)$$

Since Noise Figure degrades as the source termination departs from Γ_{opt} , contours may be constructed which yield a given noise performance for a particular source termination called noise circles. An infinite number of source terminations forming a circle provide a given noise figure. The noise circles are plotted by first locating the center of a particular circle using Equation 26.

$$N_i = \frac{F_i - F_{min}}{4r_n} |1 + \Gamma_{opt}|^2 \quad (25)$$

$$C_{F_i} = \frac{\Gamma_{opt}}{1 + N_i} \quad (26)$$

Equation 27 calculates the radius of each noise circle.

For LNA design, a gain versus noise trade-off is typically made. Available gain circles are plotted with constant noise figure circles for a trade-off between gain and noise figure. The optimum noise performance seldom coincides with the maximum gain of the device. Since each gain or noise circle describes the device performance under a given set of conditions, a prediction of gain and noise figure is determined by a known source termination. Enhanced noise performance is obtained with a source termination closer to the optimum noise termination Γ_{opt} , at the expense of gain. More gain results when the source termination is conjugately matched to the device input, Γ_{MS} , at the expense of noise figure. A trade-off is made between noise and gain by selecting an intermediate source termination. Thus, neither optimum noise nor maximum gain is obtained.

1.5 SMITH CHART

The Smith Chart is a graphical tool commonly used in radio frequency (RF) engineering for impedance matching and transmission line analysis. It allows for easy visualization of complex impedance values and simplifies calculations

of reflection coefficients, standing wave ratios, and other RF parameters.

1.5.1 Introduction:

Smith Chart (shown in Figure 6) is a powerful tool for solving a variety of problems related to radio frequency (RF) circuit design and analysis. Developed by Phillip H. Smith in the early 20th century, this graphical representation of complex impedance has become an indispensable tool for RF engineers. The Smith Chart is a polar graph in which the impedance is represented as a function of frequency. It is used to plot the impedance of a transmission line, such as coaxial cable, and to visualize the effect of impedance matching. By using the Smith Chart, engineers can easily see how impedance matching affects the reflection coefficient and voltage standing wave ratio (VSWR) of a transmission line.

The Smith Chart is based on the concept of normalized impedance. Impedance is normalized by dividing it by the characteristic impedance of the transmission line. The characteristic impedance is the ratio of the voltage to the current in a transmission line. By normalizing the impedance, it is possible to plot a single curve on the Smith Chart that represents all possible impedances. This curve is called the normalized impedance curve, or the unity circle. The Smith Chart is also used to visualize the transformation of impedance caused by transmission lines or other RF devices. By plotting the impedance before and after the device on the Smith Chart, engineers can easily see the transformation of the impedance. In addition to impedance, the Smith Chart can also be used to plot other parameters, such as admittance and reflection coefficient. The reflection coefficient is the ratio of the reflected voltage to the incident voltage in a transmission line. By plotting the reflection coefficient on the Smith Chart, engineers can easily see the relationship between reflection coefficient and impedance. There are several advantages to using the Smith Chart. First, it

provides a graphical representation of complex impedance that is easy to use and interpret. Second, it allows engineers to quickly and easily see the effects of impedance matching and transmission line transformations. Finally, the Smith Chart can be used to design and optimize RF circuits, such as filters and matching networks. In summary, the Smith Chart is an essential tool for RF engineers, providing a powerful graphical representation of complex impedance and allowing engineers to visualize the effects of impedance matching and transmission line transformations. By understanding and using the Smith Chart, engineers can design and optimize high-performance RF circuits. The Smith chart is a graphical tool used in radio frequency (RF) engineering to simplify the analysis and design of transmission lines and matching networks. It was developed by Phillip H. Smith in the early 1930s and has become an essential tool for RF engineers and designers. The Smith chart is a polar plot of complex impedance, where the real part is represented along the horizontal axis and the imaginary part is represented along the vertical axis. The chart is a unit circle centered at the origin, with a radius of 1.0. The chart is logarithmic in scale, which makes it useful for analyzing a wide range of frequencies.

One of the primary uses of the Smith chart is for impedance matching. Impedance matching is the process of adjusting the impedance of a circuit to maximize the transfer of power between the source and the load. The Smith chart simplifies this process by providing a graphical representation of the impedance of a transmission line or matching network. This allows the engineer to easily visualize the impedance transformations required to achieve a desired impedance match. Another important use of the Smith chart is for the analysis of transmission lines. A transmission line is a type of cable used to transmit electrical signals from one point to another. The Smith chart can be used to analyze the behavior of transmission lines, such as the reflection coefficient and standing wave ratio. The reflection coefficient is a measure of the reflection of

energy at the boundary of a transmission line. It is defined as the ratio of the reflected voltage to the incident voltage. The reflection coefficient can be plotted on the Smith chart, where it is represented as a point on the chart. The distance of the point from the center of the chart represents the magnitude of the reflection coefficient, while the angle from the horizontal axis represents the phase of the reflection coefficient. The standing wave ratio (SWR) is a measure of the amount of energy reflected by a transmission line. It is defined as the ratio of the maximum voltage to the minimum voltage on the transmission line. The SWR can be plotted on the Smith chart, where it is represented as a circle on the chart. The diameter of the circle represents the magnitude of the SWR, while the angle from the horizontal axis represents the phase of the SWR.

In summary, the Smith Chart is a graphical tool used in the analysis and design of transmission lines and matching networks. It provides a polar plot of the complex reflection coefficient and simplifies the visualization of impedance and admittance values. The Smith Chart is widely used in RF and microwave circuit design, and it can help optimize the impedance matching of antennas, filters, and amplifiers. The chart simplifies complex calculations, making it easy to analyze and design transmission lines and matching networks. It also provides an intuitive graphical representation of the behavior of transmission lines and matching networks, enabling engineers to visualize the interaction between various components. The Smith Chart is a versatile and useful tool in RF and microwave engineering, and its application is essential to design high-performance and efficient circuits. Its usefulness lies in its ability to simplify complex calculations, and its intuitive graphical representation can help engineers to visualize the behavior of transmission lines and matching networks.

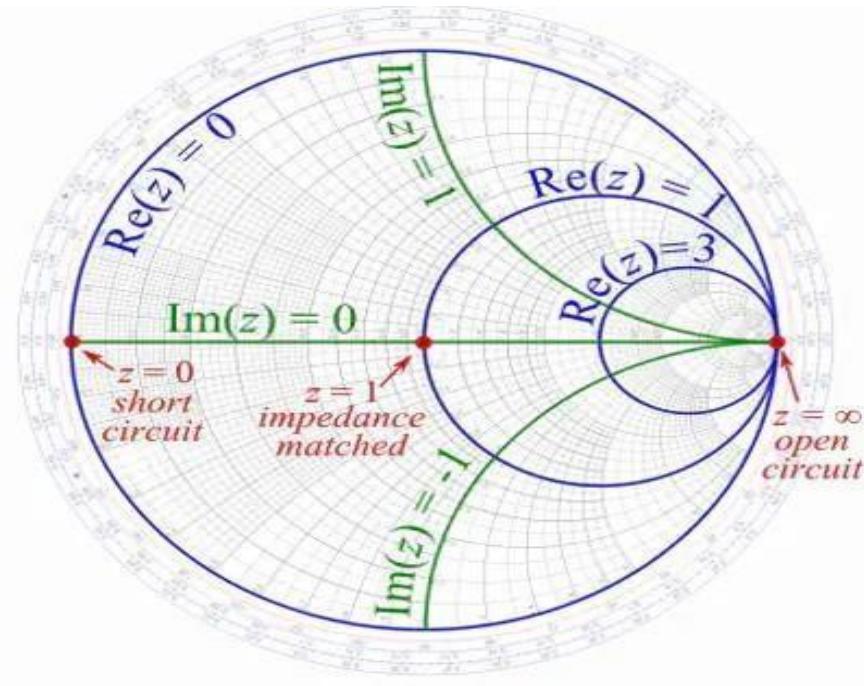


Figure 6 - Smith Chart

1.5.2 Smith Chart Applications

The Smith chart is a powerful tool in microwave engineering for designing and analyzing circuits. It can be used for a variety of applications, including impedance matching, filter design, and transmission line analysis. In this section, we will discuss some of the most common applications of the Smith chart.

- 1. Impedance matching:** Impedance matching is a critical aspect of microwave circuit design, and the Smith chart is an essential tool for achieving it. The chart enables the designer to visualize and optimize impedance transformations between different circuits and components. By plotting the load impedance on the chart and then finding the corresponding reflection coefficient, it is possible to calculate the required impedance transformation to achieve maximum power transfer. The designer can then select the appropriate transmission line or matching network to achieve the desired impedance transformation.

- 2. Filter design:** The Smith chart can also be used for designing microwave filters. By plotting the filter response on the chart, it is possible to identify the required component values to achieve the desired filter characteristics. For example, by plotting the impedance of a filter on the chart, it is possible to identify the frequency response of the filter and select the appropriate values for the capacitors and inductors.
- 3. Transmission line analysis:** The Smith chart is also a powerful tool for analyzing transmission lines. By plotting the impedance of a transmission line on the chart, it is possible to identify the characteristics of the line, such as its characteristic impedance, propagation constant, and reflection coefficient. This information is essential for designing and optimizing transmission line circuits, such as power dividers, couplers, and filters.
- 4. Antenna design:** The Smith chart is also useful in antenna design, particularly for designing matching networks. By plotting the impedance of the antenna on the chart, it is possible to identify the required matching network to achieve the desired impedance transformation. This is critical for maximizing the power transfer between the antenna and the transmission line and optimizing the radiation pattern of the antenna.
- 5. Amplifier design:** The Smith chart is also useful in designing microwave amplifiers. By plotting the input and output impedances of the amplifier on the chart, it is possible to identify the required matching network to achieve maximum power transfer and minimize the reflection coefficient.

1.5.3 Electronic Smith Chart (ESC) Tool

Electronic Smith Chart (ESC) tools are computer software programs designed to simulate and analyze microwave circuits using the Smith chart. These tools

provide a graphical representation of complex impedances and the corresponding reflection coefficients on a Smith chart, making it easier for engineers to design and optimize microwave circuits. In this article, we will discuss the features and applications of ESC tools and their benefits in microwave circuit design. ESC tools are based on the Smith chart, which is a graphical representation of complex impedances and the corresponding reflection coefficients on a normalized impedance plane. The Smith chart is widely used in microwave engineering to analyze transmission lines, antennas, and other microwave circuits. It is particularly useful in impedance matching and tuning circuits for maximum power transfer.

ESC tools provide a graphical interface for designing and analyzing microwave circuits using the Smith chart. These tools typically allow users to enter circuit parameters such as frequency, characteristic impedance, and component values, and then simulate the circuit's behavior on the Smith chart. The software calculates and displays the reflection coefficient, standing wave ratio, impedance, and other parameters on the Smith chart, allowing the user to analyze the circuit's performance and make design changes as necessary. One of the key advantages of ESC tools is their ability to simplify complex calculations and provide a visual representation of circuit behavior. With ESC tools, engineers can quickly and easily analyze circuit performance, identify potential problems, and optimize their designs for maximum efficiency. This saves time and reduces the risk of errors compared to manual calculations and simulations.

ESC tools are used in a wide range of applications in microwave circuit design, including transmission line design, antenna design, filter design, amplifier design, and impedance matching. For example, in transmission line design, engineers use ESC tools to analyze the behavior of different types of transmission lines, such as coaxial cables and waveguides, and to optimize their

impedance matching for maximum signal transfer. ESC (ESC) tools are software-based applications that allow users to create, manipulate and analyze Smith charts electronically. They have become increasingly popular among engineers and students in the field of electrical engineering due to their versatility, ease of use, and ability to simplify complex calculations. One of the significant advantages of using ESC tools is their ability to provide real-time analysis of circuits. The tools allow users to modify the circuit's parameters and observe the changes on the Smith chart, allowing for faster and more efficient circuit optimization.

1.6 MICROSTRIP LINES

Microstrip lines are a popular type of transmission line used in radio frequency (RF) and microwave circuits. They consist of a thin conductor placed on a dielectric substrate, allowing for easy integration with other components. Microstrip lines are widely used in RF engineering due to their low cost and ease of fabrication.

1.6.1 Introduction to Microstrip Lines

Microstrip lines (Shown in Figure 7) are a type of transmission line used in microwave and radio frequency (RF) applications. They are composed of a conductor strip separated from a ground plane by a dielectric substrate. Microstrip lines are widely used in various RF and microwave components such as antennas, filters, amplifiers, couplers, and mixers. They offer several advantages over other transmission lines, including low cost, low weight, and easy integration with other components on a printed circuit board (PCB). In a microstrip line, the conductor strip is usually made of copper or other highly conductive material and is typically very thin, with a width ranging from a few microns to several millimeters. The ground plane is typically a larger area of copper on the opposite side of the dielectric substrate. The dielectric substrate is

usually made of a low-loss material with a high dielectric constant, such as alumina, glass-reinforced Teflon (PTFE), or Rogers Duroid. The thickness of the substrate is typically in the range of a few tenths of a millimeter to a few millimeters.

They consist of a thin strip of conducting material, typically copper, on a substrate layer, which is usually a low-loss dielectric material. The top surface of the substrate is usually covered by a thin layer of metal, forming a ground plane. Microstrip lines have several advantages over other types of transmission lines, including low cost, ease of fabrication, and compatibility with integrated circuit technology. The basic structure of a microstrip line consists of a conducting strip, a dielectric substrate, and a ground plane. The conducting strip and the ground plane are usually made of copper or other highly conductive metals. The dielectric substrate can be made of a variety of materials, such as alumina, teflon, or quartz, depending on the specific application. The dielectric constant and thickness of the substrate determine the characteristic impedance and the velocity of propagation of the signal in the microstrip line.

The signal in a microstrip line is guided along the conducting strip and the dielectric substrate, with the ground plane providing a return path for the current. The electric and magnetic fields associated with the signal are mostly confined to the dielectric substrate, with some leakage into the air above the strip and the ground plane. The amount of leakage depends on the thickness of the substrate and the width of the strip. The characteristic impedance of a microstrip line is determined by the width of the strip, the thickness and dielectric constant of the substrate, and the distance between the strip and the ground plane. The impedance is typically in the range of 25 to 100 ohms, although higher and lower values can be obtained by varying the dimensions and materials of the line. The characteristic impedance of the line is important

because it determines the amount of power that can be transmitted without reflection or loss.

Microstrip lines have several advantages over other types of transmission lines, such as coaxial cables and waveguides. They are easier and cheaper to fabricate, and can be integrated with other components on a single substrate. The geometry of a microstrip line is defined by its width (W), thickness of the substrate (h), and the dielectric constant of the substrate (ϵ_r). The characteristic impedance (Z_0) of a microstrip line is determined by these parameters and can be calculated using several analytical and numerical methods. The most commonly used method is based on the quasi-TEM mode approximation, which assumes that the electric and magnetic fields are predominantly transverse electromagnetic (TEM) waves, and that the fields are uniform along the width of the conductor and the thickness of the substrate.

The propagation velocity of a microstrip line depends on the dielectric constant of the substrate and the width of the conductor. The phase velocity of the signal is lower than the velocity of light in free space due to the presence of the dielectric substrate. The characteristic impedance of a microstrip line can be made to match the input impedance of other components such as amplifiers and filters by adjusting the width of the conductor or the thickness of the substrate.

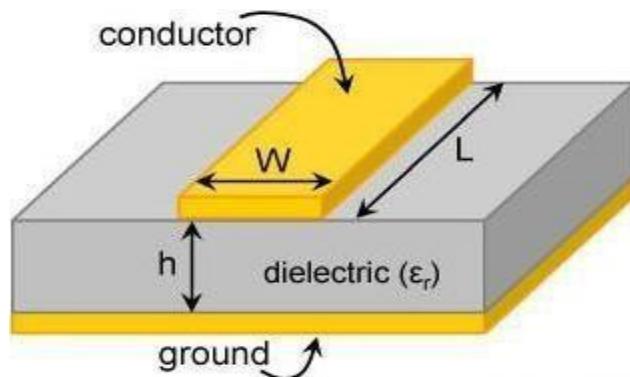


Figure 7 - Microstrip Line

1.6.2 - Applications of Microstrip Lines

Microstrip lines are widely used in high-frequency electronic circuits, particularly in microwave applications. Some of the common applications of microstrip lines include:

- 1. Antennas:** Microstrip lines are used as feed lines in microstrip antennas, which are widely used in radar and wireless communication systems.
- 2. Filters:** Microstrip lines can be used to create various types of filters, such as low-pass, high-pass, bandpass, and notch filters.
- 3. Amplifiers:** Microstrip lines can be used as interconnects between amplifiers and other components in RF and microwave systems.
- 4. Couplers:** Microstrip lines can be used to create couplers, which are used to divide or combine power in microwave circuits.
- 5. Delay lines:** Microstrip lines can be used to create delay lines, which are used to introduce a time delay in a signal.

Overall, Microstrip Lines are widely used in microwave and RF circuits as transmission lines. They consist of a thin strip of conductive material (typically copper) on top of a dielectric substrate, with a ground plane on the bottom. Microstrip Lines offer several advantages over other transmission line types, including low cost, easy fabrication, and compatibility with integrated circuits. They also exhibit predictable and controllable impedance characteristics, which allows for efficient signal transfer with minimal reflection and loss. However, microstrip lines are also prone to radiation and coupling with nearby components, which can lead to unwanted signal distortion and interference. Proper design and layout techniques can mitigate these effects and ensure optimal performance of microstrip line-based circuits.

Chapter 2

LITERATURE REVIEW

1. Design of an Ultra Low Power LNA for 5-GHz band - Nishant Kumar, Rajini Bisht, IEEE 2020.

Wireless communication has undergone significant changes due to the revolution of the Internet of Things (IoT). With advancements in wireless communication technology, issues and barriers are eliminated, leading to the development of low-power and high-performance LNAs. LNAs are the noise selecting component that amplifies the desired signal and suppresses noise in the RF receiver. For optimal receiver performance, the goal is to achieve minimum noise and maximum gain. This paper focuses on the design of a low-power LNA operating at 5GHz using capacitive coupling topology to enhance gain performance while minimizing the noise figure (NF). Additionally, techniques like current reuse and forward-body-bias are used to minimize power dissipation. Wi-Fi standards now work on 5GHz bands, and this paper is designed to work at this frequency. There are many CMOS LNA circuits that have been demonstrated in the last few years, with a focus on minimizing power dissipation, enhancing gain performance, and minimizing NF. Capacitive coupling topology has been used to achieve these goals. The advancements in low-power LNA design are significant as they enable the development of next-generation wireless communication systems for the IoT era. The challenges associated with designing LNAs for high-performance wireless communication systems are many. The advancements in technology have led to the development of low-power LNAs that provide an effective solution for the design of high-performance wireless communication systems. The research in this field is essential for the development of RF receivers that can achieve optimal performance while consuming minimal power.

2. Switched Low-Noise Amplifier Using Gyrator-Based Matching

Network for TD-LTE/LTE-U/Mid-Band 5G and WLAN Applications - Tsai, C.-H.; Lin, C.-Y.; Liang, C.-P.; Chung, S.-J.; Tarng, J.-H, MDPI 2021

The advancements in mobile telecommunication systems, such as 4G systems like TD-LTE, have made significant progress. The major TD-LTE frequency bands currently in use are 2.3 GHz (Band 40), 2.6 GHz (Band 41), and 3.5 GHz (Bands 42 and 43). To improve the performance of LTE and provide faster and more secure mobile services, utilizing LTE-unlicensed (LTE-U) band in the unlicensed 5-GHz spectrum is considered a favorable solution for achieving a larger bandwidth. The IEEE 802.11ac, with an operating frequency of 5 GHz, has been developed and specified as a Wi-Fi standard that is three times faster than IEEE 802.11n. Therefore, several coexistence schemes have been developed for efficient and fair spectrum sharing between LTE-U and WLAN. Highly integrated radio-frequency integrated circuits with multiple bands are becoming critical for use in TD-LTE, LTE-U, 5G, and WLAN applications. However, compatibility with 2-, 3-, and 5-GHz bands operation has become challenging for low-noise amplifier designers. A dual-resonant transformer-based matching network was analyzed and capable of two different frequencies, but a dual-band operation is insufficient to cover the latest triple-band wireless standard. The lossy silicon substrate limits the reliability of the LNA, and several papers have proposed methods for ameliorating the noise of LNAs. In conclusion, this paper proposes a novel approach to address the challenges associated with the design of LNAs for multiple bands.

3. CMOS Low-Noise Amplifier Design Optimization Techniques - Kein Nguyen, Sang-Gug Lee, IEEE

CMOS technology has emerged as a popular choice for implementing radio transceivers in various wireless communication systems due to its scalability,

high level of integration, and low cost. The low-noise amplifier is a crucial component in a radio receiver, as it typically dominates the sensitivity. However, LNA design involves numerous tradeoffs, such as noise figure, gain, linearity, impedance matching, and power dissipation. The primary objective of LNA design is to achieve simultaneous noise and input matching (SNIM) at a given power dissipation. Several LNA design techniques have been proposed to achieve this goal, including classical noise matching (CNM), SNIM, power-constrained noise optimization (PCNO), and power-constrained simultaneous noise and input matching (PCSNIM). This paper aims to analyze the four LNA design techniques based on noise parameter expressions to provide a comprehensive and consistent understanding of CMOS-based LNA design techniques.

4. Practical Considerations for LNA Design - By Tim Das Freescale Semiconductor, NXP Semiconductors 2023

In the field of radio receiver design, the LNA is a critical component that significantly impacts receiver performance. The RF design engineer must focus on optimizing the front-end performance of the receiver, paying particular attention to the first active device. This paper examines the variables that affect LNA performance at both the device and board levels, and the challenges that arise when accommodating specific application requirements. The paper explores three popular LNA topologies and two process technology implementations, highlighting the performance trade-offs associated with each. The primary objective of LNA design is to achieve sufficient sensitivity to detect the signal of interest amidst the noise and interference. Five characteristics that impact receiver sensitivity include noise figure, gain, bandwidth, linearity, and dynamic range. However, controlling these variables requires a thorough understanding of the active device, impedance matching, and the intricacies of fabrication and assembly to produce an amplifier that

achieves optimal performance with the fewest trade-offs. The paper aims to provide a concise summary of the key considerations affecting LNA performance and implementation.

5. Design at 2.4GHz LNA for Wifi-Application - M. EL BAKKALI, N.AMAR TOUMI, T. ELHAMADI, IEEE 2019

LNAs are critical components in the reception chain of wireless networks and mobile devices, and must be continuously improved to meet new standards and performance requirements. The 802.11 family of standards, which includes the popular Wi-Fi (Wireless Fidelity) protocol, has seen significant growth and demands high data rates, necessitating the development of high-speed communication links with reliable quality. When designing LNAs for these applications, the choice of transistor is crucial and should exhibit minimal noise, such as GaAs or GaN field effect transistors. The selection of an appropriate topology is also essential, as it impacts factors such as bandwidth range, gain, noise levels, power dissipation, and chip size. In this paper, we present the design of a planar LNA using RF4 substrate for 2.4GHz wireless applications. The article discusses the transistor choice and bias point, LNA theory, and design methodology, followed by an explanation of the electromagnetic simulation results of the 2.4GHz layout and a comparison with existing works.

Chapter 3

DESIGN GOALS AND METHODOLOGY

In this chapter, the design goal for LNA is represented and discussed. Then, the general methodology to design LNA is described. At last, the AWR design environment is briefly introduced.

3.1 LNA DESIGN GOALS

In Table 1, specifications for LNA are clearly represented. As we can see, the required operation band for the LNA is a wide bandwidth range. And the central frequency is at 6 GHz, which lies in the so-called C-band according to the classification of the radio frequency range.

Table 1 - LNA Design Goals

Parameters	Goals
Frequency Range	5.8 - 7.2 GHz
Amplifier Maximum Gain	25 - 28 dB
Noise Figure	< 1.5 dB
Input Return Loss (S11)	< -15 dB
Output Return Loss (S22)	< -15 dB

The gain of an amplifier operating within the frequency range of 5.8 to 7.2 GHz should be restricted to a maximum range of 25 dB to 28 dB. This is due to the current state of the art development in transistor and amplifier technology.

For the noise figure, the largest acceptable value is 1.5 dB. To obtain the noise figure of an amplifier is the primary target, and we should always pay attention to the value of NF after adding new components during our design process. Maintaining a noise figure below 1.5 dB is crucial when designing an amplifier.

It is important to keep track of the noise figure value after adding new components to the design process, as achieving the desired noise figure is the primary objective. Verifying that the return loss is greater than 15 dB is essential to ensure that the amplifier exhibits good power efficiency characteristics. To determine the return loss, it is necessary to measure the S22 of the final LNA.

In the design process using Advance Design System (ADS), it is advantageous to use components that are already available in its library. This ensures continuity and convenience under the same design environment. The ADSlibrary includes a wide range of popular vendor parts that are directly embedded, making them easily accessible and simple to use, which enhances the effectiveness of the design process.

3.2 DESIGN METHODOLOGY

LNA design often involves the use of S-parameters, which are commonly employed to describe the behavior of two-port networks. By analyzing S-parameters, one can determine key characteristics such as maximum achievable gain, possible instability issues, and input/output impedance levels. S-parameters also provide a means of calculating the ideal source and load impedances for a given transducer gain, which is helpful in selecting appropriate components for the design.

Designing a LNA for microwave applications can be achieved through various approaches and in different sequences. However, our specific design process consists of the following steps:

- The initial step in our microwave LNA design involves selecting the appropriate active device. It is crucial to choose a transistor that aligns with our specifications outlined in Table 1, with regards to factors such as noise level, gain, and operating frequency.

- The second step in our LNA design process is to develop a biasing circuit that can provide the appropriate bias to the selected transistor. The biasing circuit must meet the noise and gain requirements of the transistor while also contributing to overall stability.
- The third step in our microwave LNA design involves using the Smith Chart to achieve an optimal design. By leveraging this tool, we can determine the ideal loads Γ_S and Γ_L for our selected transistor at the central frequency of 6 GHz. It is essential that these loads fall within the stability admission region of the Smith Chart. We then proceed to design both the Minimum Noise Amplifier (MNA) stage and the Maximum Gain Amplifier (MGA) stage independently, taking into account the desired specifications and requirements.
- The fourth step in our microwave LNA design process involves the cascading of the MNA and MGA stages into a three-stage amplifier configuration. This is achieved by implementing the MNA as the first two stages and the MGA as the final (third) stage. To achieve a reduction in the overall noise figure and an increase in gain, input and output matching networks are designed for each stage. Additionally, interstage matching networks are also incorporated into the design. In our approach, all of the matching networks are realized using ideal transmission lines generated with the aid of ESC tools available in ADS.

- In the fifth step of our microwave LNA design process, the ideal transmission lines used in our design are replaced with practical microstrip lines. To determine the appropriate length and width of the microstrip lines, we utilize the LineCalc tool available in ADS. This step is essential in ensuring the practical implementation of the LNA, and the optimization of the length and width of each microstrip line can lead to improved overall performance.
- The final step in our microwave LNA design process involves simulating the designed LNA to assess its performance. To accomplish this, we utilize Python programs to verify the output and ensure that the LNA meets our desired specifications and requirements. This step is critical in determining the practical effectiveness of the LNA and ensuring that it operates as intended.

3.3 ADVANCED DESIGN SYSTEM

Advanced Design System (ADS) is a powerful software suite that is widely used in the design and analysis of microwave and RF circuits. Developed by Keysight Technologies, ADS provides a comprehensive set of tools and capabilities for designing, simulating, and optimizing complex electronic systems. The software supports a range of applications, including high-frequency circuit design, signal integrity analysis, and electromagneticsimulation. One of the key strengths of ADS is its ability to integrate seamlesslywith other tools and technologies, such as MATLAB and Python, allowing for efficient and flexible workflow. Additionally, ADS includes a vast library of components and models, including active and passive devices, transmission lines, and substrate materials, that can be used to build and analyze complex circuits. ADS also includes advanced simulation capabilities, such as harmonic balance analysis and transient analysis, that can accurately model nonlinear

behavior and transient effects. Moreover, ADS provides a wide range of optimization and tuning tools, such as parameter sweeps and Monte Carlo simulations, that enable designers to quickly and efficiently optimize their designs.

In conclusion, Advanced Design System (ADS) is a powerful and versatile software tool that offers a wide range of capabilities for the design, analysis, and optimization of RF and microwave circuits. It has become a popular tool in the field of wireless communication due to its user-friendly interface, extensive component libraries, and advanced simulation features. ADS offers various simulation technologies such as circuit simulation, electromagnetic simulation, and system simulation, making it a comprehensive solution for RF and microwave circuit design. Additionally, ADS supports various design methodologies, including statistical design, yield optimization, and Monte Carlo analysis, enabling designers to make informed decisions about the performance, yield, and cost of their designs. Despite its numerous advantages, ADS has some limitations. It requires specialized training to use the software effectively, and it can be expensive for individual users or small companies. However, its value and efficiency for designing complex RF circuits far outweigh the costs. In summary, ADS has revolutionized the design process of RF and microwave circuits, providing designers with powerful tools to optimize circuit performance, reduce design time, and achieve higher levels of integration. Its continued development and innovation will undoubtedly shape the future of wireless communication technology.

Chapter 4

COMPONENT SELECTION

In any electronic circuit design, the proper selection of components is crucial for ensuring a successful outcome. Similarly, in our project, the choice of active device, substrate characteristics, and DC blocking capacitors is critical to the performance of our LNA. Therefore, in this chapter, we provide a detailed discussion on the selection criteria for these components. Through our discussion, we will identify the key specifications and parameters that must be considered when selecting the active device, substrate, and DC blocking capacitors. We will also examine the impact of each component's choice on the LNA's overall performance, such as its noise figure, gain, and stability. By providing a thorough understanding of the selection process, we can ensure that our LNA is designed to meet our desired specifications and requirements.

4.1 TRANSISTOR SELECTION

Numerous manufacturers offer a wide range of transistors, including Broadcom, Cree, Freescale, Fujitsu, Hewlett-Packard, MACON, Mimix, Mitsubishi, MwT, Philips, Polyfet, Rohm, SEDI, Semicoa, Raytheon, RFMD, Srenza, Sony, Toshiba, and Transcom. We thoroughly examine their product lists and datasheets to select the appropriate active device, which is typically a silicon transistor of the BJT, FET, or HEMT type.

When selecting the active device, we must take a global perspective and consider the transistor's specifications. Some transistors are unsuitable for our purposes due to their low working frequency, such as those produced by Freescale and Polyfet, which operate below 2GHz. Additionally, certain transistors have a high noise figure (NF) or lack an s-parameter file, such as those from Cree, Fujitsu, Raytheon, RFMD, Philips, Mitsubishi, Srenza, Sony,

Toshiba, Transcom, and others. Although some transistors, such as the MwT-LN180 by MwT and certain series by MACON, offer exceptional performance, their comparably higher prices make them impractical for our design. Therefore, it is crucial to carefully consider the specifications and price of the active device before selecting it for our design.

4.1.1 Process Technologies

The most popular active devices used in LNAs are based on GaAs pHEMTs and SiGe BiCMOS process technologies. Performance differences between the two technologies are shown in Table 2.

Table 2 . Comparison of Device Technologies for L– and S–Band LNAs

Typical Performance	GaAs pHEMT	SiGe BiCMOS
Noise Figure (dB)	≥ 0.4	≥ 0.9
Gain (dB)	12 to 21	10 to 17
OIP3 (dBm)	≥ 41	≥ 31
Breakdown Voltage (Vdc)	15	Much less than 15
Inductor Q-factor	15	5 to 10
Strengths	Hight P1dB and OIP3, Very Low Noise Figure	Higher Integration, Lower Cost, ESD Immunity
fT/ fMAX	Similar	

GaAs pHEMT devices generate very little noise due to the heterojunction between the doped AlGaAs layer and the extremely thin undoped GaAs layer, but the real advantage of GaAs is in gain linearity. Today's SiGe process technology is comparable to GaAs devices in terms of usable frequency range, but the relatively low breakdown voltage of SiGe devices limits dynamic range. GaAs pHEMT has clear advantages over SiGe implementations in terms of noise figure and linearity performance, whereas SiGe can operate much more

efficiently and has cost advantages due to higher levels of integration. As with any device technology, the relative advantages and disadvantages of each must be evaluated within the context of a specific application. To understand how process technologies differ in practice, consider the attributes of 30 commercially available LNAs MMICs produced by various manufacturers. All 30 devices operate within the 1400–2200 MHz frequency range, but each device does not share a common application. As a result, each design differs in performance optimization and trade-offs. That difference prevents direct comparisons between devices. Observations, however, limited to general characteristics of SiGe and GaAs designs are still relevant.

Figures 8 and 9 illustrate the performance trade-offs between OIP3 versus noise figure and OIP3 versus power consumption, respectively. Figure 8 illustrates that GaAs pHEMT devices generally have a higher OIP3 and lower noise figure than SiGe BiCMOS devices because they are designed to operate at higher power consumption levels. Figure 9 illustrates the clear distinction between how the technologies are used for mobile applications, where power budgets are very low, and other applications, where higher power consumption affords the opportunity to achieve LNAs with higher linearity.

GaAs pHEMT LNAs generally exhibit a much more optimal combination of high linearity and low noise when compared to SiGe implementations. GaAs pHEMT devices vary widely in power consumption compared to SiGe devices, which consume much less. GaAs pHEMT technology is best suited to applications in which optimization of receiver sensitivity is the foremost concern, such as in cellular base stations. SiGe LNAs, on the other hand, are best suited to applications in which sensitivities to power consumption and cost figure more prominently.

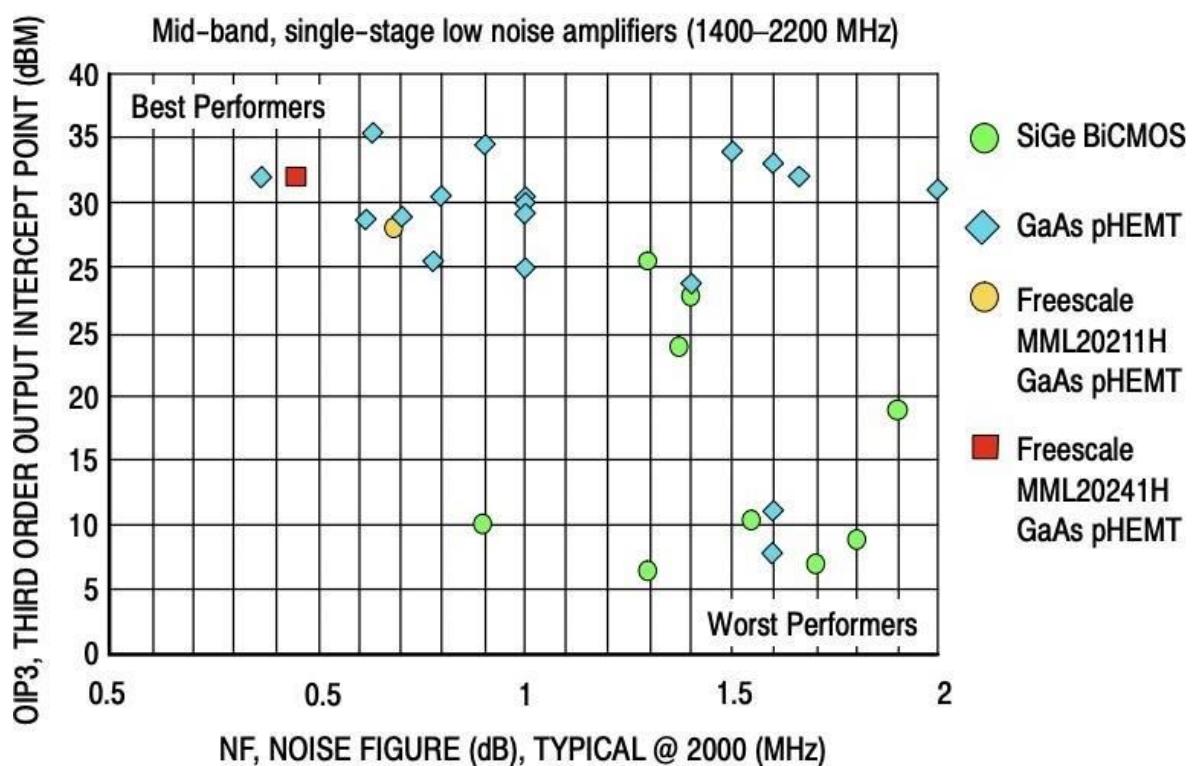


Figure 8 - Third Order Output Intercept Point versus Noise Figure

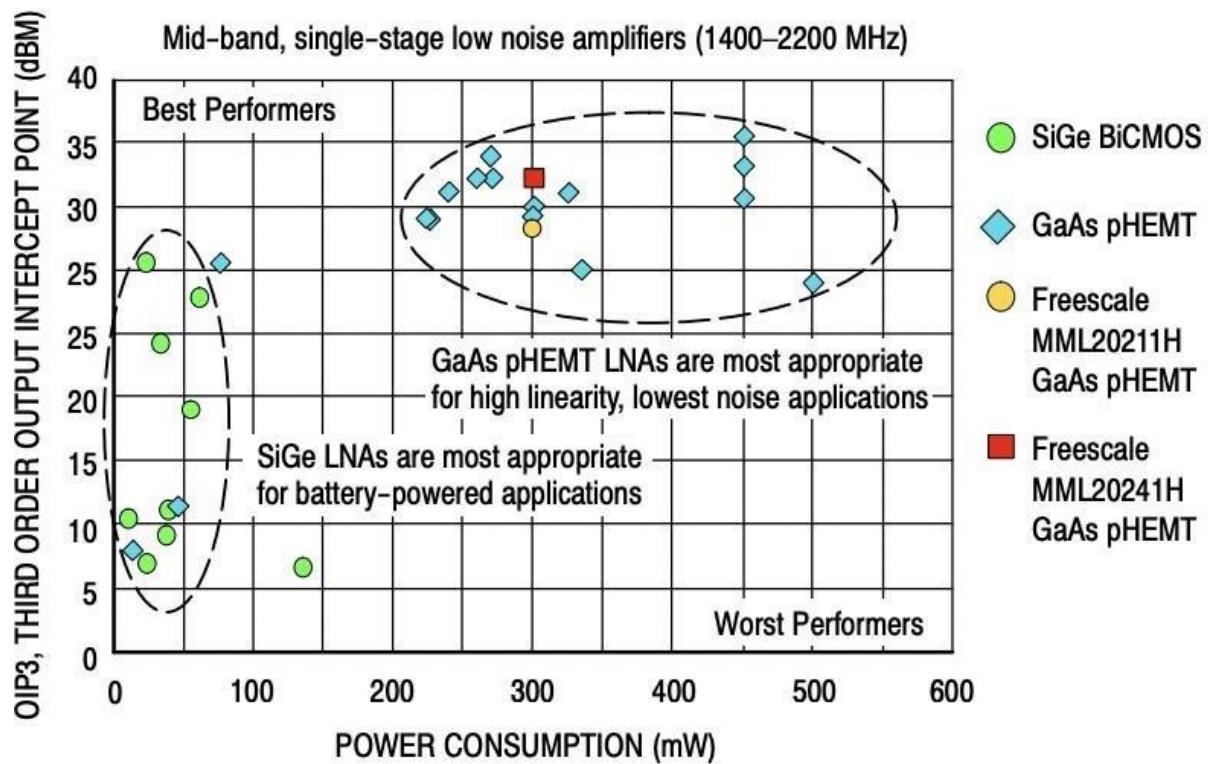


Figure 9 - Third Order Output Intercept Point versus Power Consumption

In conclusion, GaAs pHEMT and SiGe BiCMOS are both important technologies for the design of RF circuits in modern wireless communication systems. Each technology has its own advantages and limitations, and the choice of technology depends on the specific requirements of the application. Both technologies have made significant contributions to the development of wireless communication and will continue to play a crucial role in future advancements.

4.1.2 Transistor Geometry and Package Parasitics

Beyond the choice of process technology, LNA noise figure performance is significantly affected by transistor design and package parasitics. Although a transistor can be constructed for a perfect $50\ \Omega$ match, a specific transistor design also exists at which Y_{opt} is closer to Y_{in} while minimizing R_n . Shrinking transistor sizing improves power consumption, but often at the expense of degraded NF_{min} and IP_3 performance. Alternative dimensioning, such as narrower and shorter gate fingers on a field effect transistor (FET), can sometimes improve the noise figure by lowering gate resistance and high-frequency gain; stability also improves. Wider gate width or gate finger multiples increase transistor transconductance. As transistor aspect ratios take advantage of newer process technology nodes, however, these intrinsic relationships between electrical characteristics and transistor construction start to become muddled as device parasitics become more significant.

Package parasitics grow as frequency increases. Physical structures, such as bond-wires and bond-pads along with package capacitance, often dominate package parasitics and have a direct affect on the noise figure, input-impedance matching, and transistor transconductance. The designer must mitigate the effects of each of these elements; some tight process controls can even turn these structures into constructive design elements. Carefully controlled

bond-wire placement and length can be used as input-matching elements or to provide source degeneration.

4.1.3 ATF-13136 2-16 GHz LNA

The ATF-13136 is a LNA that operates in the frequency range of 2-16 GHz. It is a popular choice for applications in microwave and millimeter-wave systems due to its excellent noise figure and gain characteristics. The LNA is manufactured by Avago Technologies, now part of Broadcom Inc. The ATF-13136 is a monolithic microwave integrated circuit (MMIC) that uses a pseudomorphic high electron mobility transistor (pHEMT) technology. This technology provides high transconductance and low output conductance, which results in low noise and high gain characteristics.

From ATF-13136 Datasheet (see Appendix A) has a minimum noise figure of 1.0 dB at 8 GHz and a typical gain of 11.5 dB at 8 GHz. It can operate with a single positive supply voltage of 2.5 V and a bias current of 25 mA. The device is housed in a small, surface-mount package that makes it easy to integrate into various microwave circuits. The ATF-13136 LNA has been widely used in various applications, such as in radar systems, communication systems, and instrumentation. Its excellent noise figure and gain characteristics, combined with its small size and ease of integration, make it a popular choice for microwave and millimeter-wave circuit designers.

The ATF-13136, a GaAs FET, has been selected as the active device for the LNA in this project. The primary reason for this choice is its compatibility with the desired frequency range of operation, which is 5.8-7.2 GHz. Additionally, the ATF-13136 offers a remarkably low Noise Figure of 0.8 dB at 6 GHz, which is half the Noise Figure specified in the design goal. This low Noise Figure is crucial as the biasing and stability circuits add further Noise Figure that needs to

be compensated. Moreover, the ATF-13136 is readily available under the RF transistor library vendor in ADS, making it a convenient choice for the project.

4.2 SUBSTRATE SELECTION OF MICROSTRIP LINES

The choice of substrate material is a critical step in the design of microstrip lines. The substrate is the foundation of the microstrip circuit and provides support for the transmission line. It is also responsible for the dielectric properties of the circuit, which can have a significant impact on its performance. The selection of the appropriate substrate material depends on several factors such as the frequency of operation, the desired dielectric constant, and the physical size of the circuit.

There are numerous materials available for substrate selection such as FR-4, Rogers, Arlon, Teflon, and many others. Each of these materials has different properties that affect the performance of the microstrip circuit. The choice of substrate material can significantly affect the overall performance of the circuit, including the propagation delay, characteristic impedance, and insertion loss. Therefore, it is important to carefully evaluate the properties of each substrate material and select the one that best suits the specific design requirements. The selection of substrate material is a crucial step in ensuring the success of the microstrip circuit design.

4.2.1 Roger RO4350B Substrate

Rogers RO4350B is a high-frequency, high-performance laminated composite material used in microwave circuits, including power amplifiers, LNAs, and RF filters. It is a ceramic-filled PTFE composite that provides excellent electrical performance, dimensional stability, and ease of fabrication. The material's low dielectric constant and loss tangent, high thermal conductivity, and excellent adhesion characteristics make it a preferred choice for high-frequency

applications. RO4350B has a typical dielectric constant of 3.48 and a loss tangent of 0.0037 at 10 GHz. It can operate over a wide temperature range and is compatible with standard FR-4 processing methods. RO4350B is commonly used in microstrip and stripline circuits due to its superior electrical properties and mechanical stability. After considering various options for the microstrip substrate, the Rogers RO4350B (detailed in Appendix B) has been chosen for the microstrip design of the LNA, as well as for the replacement of ideal transmission lines with microstrip lines. The width and length of the microstrip lines have been optimized using the LineCalc tool available in ADS to ensure optimal performance of the LNA.

In conclusion, RO4350B is a high-performance ceramic-filled hydrocarbon laminate substrate material that offers excellent electrical and mechanical properties. It is suitable for high-frequency applications up to 40 GHz and is widely used in the design and fabrication of RF and microwave circuits. The material has a low dielectric constant and loss tangent, high thermal conductivity, and a low coefficient of thermal expansion. These properties make it an ideal substrate for high-speed digital and analog circuits, power amplifiers, filters, and other high-frequency applications. RO4350B also provides excellent dimensional stability, allowing for tight tolerances in the manufacture of high-precision circuits. Its performance and reliability make it a popular choice among designers and engineers in the RF and microwave industry.

Chapter 5

COMPONENT BIAS POINT SELECTION AND BIAS CIRCUIT DESIGN

Component bias point selection and the design of a biasing circuit are crucial aspects of LNA design. The biasing circuit is responsible for setting the operating point of the active device at the optimal bias point to ensure maximum gain and minimal noise figure. The goal is to set the bias point in such a way that it is in the center of the active device's operating region, where it can produce the highest possible gain with low noise figure.

5.1 DC BIAS POINT SELECTION

One of the crucial initial stages of LNA implementation is to set the bias. Although many LNA MMICs come with an active-bias circuit that can regulate the bias currents, it is still necessary to choose an appropriate bias point that balances the gain, noise figure (NF), and linearity based on the specific application requirements. The selection of a suitable bias point is important because it can affect the LNA's performance under different conditions such as variations in supply voltage, temperature, and FET threshold voltage.

The selection of the DC bias point is crucial for the proper operation of the LNA. In this project, the FET curve trace template (Figure 10) provided by the ADS software was utilized to select the operating point for the transistor, which was set to operate as a class A amplifier. To achieve this, the transistor was biased with a drain current value equal to half the saturation drain current. This approach ensures the proper operation of the LNA and provides the required gain and noise figure characteristics for the desired frequency range.

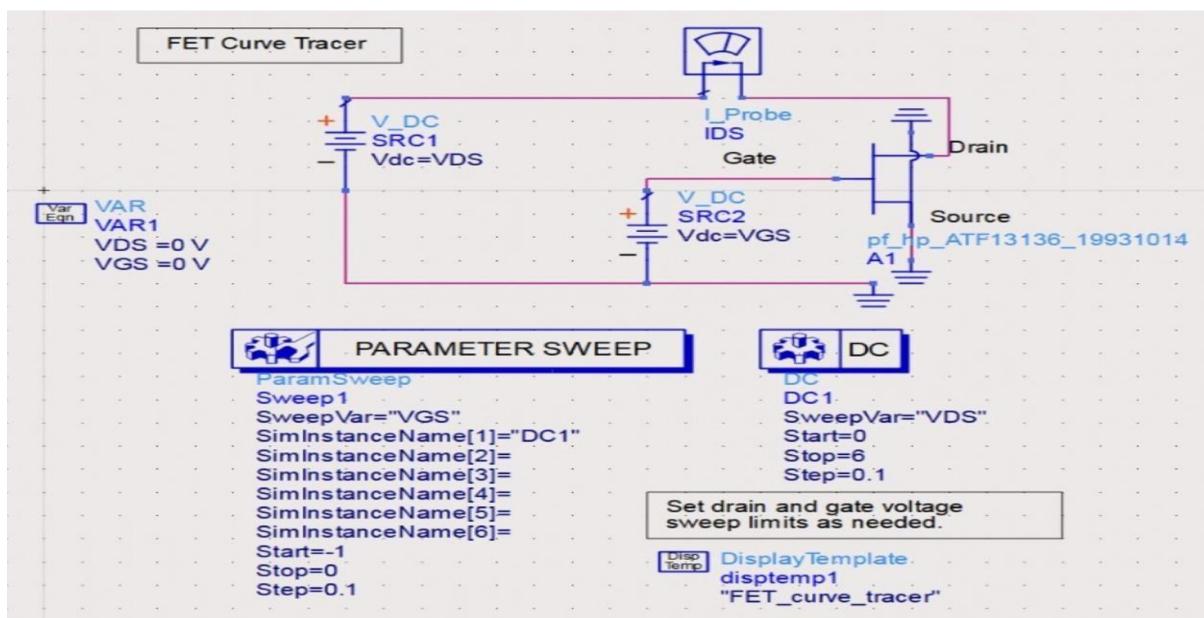


Figure 10 - FET Curve Tracer Setup

Figure 11 represents the FET Bias Characteristics (IDS Vs VDS) generated by the FET Curve Tracer Setup.

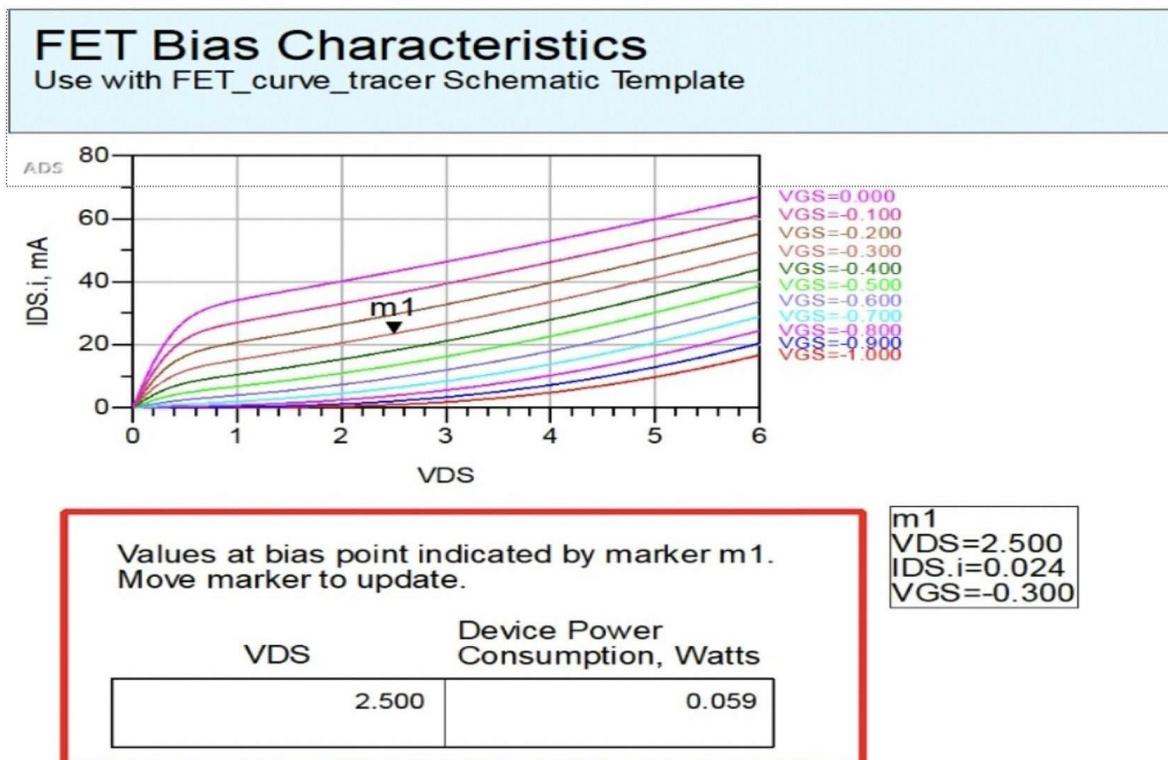


Figure 11 - FET Bias Characteristics

The operating point, or the DC bias point, for the FET was determined using the FET trace curve template provided in ADS software. The selected operating point was such that the transistor operated as a class A amplifier.

To achieve this, the FET was biased with a drain current value that was approximately half the saturation drain current. Based on Figure 5.2, the marker m1 was placed at the point (2.50 V, 24 mA), which was determined as the Q point. This Q point was selected to provide optimal values of gain and NF. Additionally, the typical value of IDSS, which is 50 mA, was considered in selecting the operating point. Hence, the FET was operated at 25 mA approximately to function as a class A amplifier.

The operation point is determined from ATF-13136 datasheet. At 6 GHz, the NFmin is about 0.9dB at $V_{ds} = 2.5V$ and $I_{ds} = 25mA$ and the gain is about 13 dB.

5.2 BIAS CIRCUIT DESIGN

Generally, amplifiers are categorized in different type based on the signal level, large signal amplifier or small signal amplifier. Each has its own particular method of analysis. In this project, a small signal amplifier is designed using small signal analysis method. This type of amplifier is only used when the signal is fluctuating from the steady bias level by a very small margin. Hence only small part of characteristics is covered in the analysis, so the operation is always in the linear region.

In this project, a small signal amplifier is designed which consists two portions of the circuitry, A DC biasing circuit and a RF/Microwave circuit. These blocks are designed with proper isolation to prevent leakage of RF signal to DC circuitry while travelling from input to output. For small signal analysis, as the

mode of operation as linear, Class A mode is used in this project to achieve proper biasing of the transistor with Q-point as $V_{DS} = 2.5V$ and $I_{DS} = 24mA$.

There are three schemes to achieve the isolation between RF circuitry and DC circuitry.

- Connecting quarter wave transformer between RF/MW circuitry and DC block.
- Connecting high-value capacitors as loads to short the residual RF/MW signals.
- Connecting RF chokes as an inductor, between RF/MW circuitry and DC block. RF choke blocks high-frequency signals such as RF signals and allows DC signal.

Connecting any two of above schemes guarantees great isolation between RF circuitry and DC circuitry.

5.2.1 DC Bias Circuit Design

To operate FET as an amplifier, it should be in a saturation region. Following steps involved in DC biasing:

- **Determine the required bias conditions:** The first step is to determine the required bias conditions for the FET based on the specifications and performance requirements of the circuit. This includes determining the desired drain current and voltage, as well as any specific biasing requirements for the FET.
- **Choose a biasing configuration:** There are several biasing configurations available, including fixed bias, self-bias, and voltage divider bias. Choose a suitable configuration based on the required bias conditions.

- **Calculate the biasing circuit values:** Once the biasing configuration is chosen, calculate the values of the biasing components such as resistors and capacitors required to provide the desired bias conditions. This can be done using FET biasing equations and design formulas.
- **Select the components:** Select the appropriate components based on the calculated values and the specifications of the circuit.
- **Build and test the circuit:** Build the biasing circuit and test it with the FET. Adjust the component values if necessary to obtain the desired bias conditions and optimal performance.
- **Analyze the circuit:** Analyze the circuit to ensure that it meets the desired specifications and performance requirements. This can be done using simulation software or through experimental testing.
- **Optimize the circuit:** If the circuit does not meet the desired specifications or performance requirements, optimize the circuit by adjusting the component values or changing the biasing configuration until the desired results are achieved.

DC simulation was employed to validate the biasing point. The bias circuit network is depicted in Figure 12 after the simulation. It can be observed that the desired values of V_{ds} and I_{ds} , approximately 2.5V and 25mA, respectively, were achieved. This confirms that the bias circuit design was effective in establishing the desired operating point of the circuit.

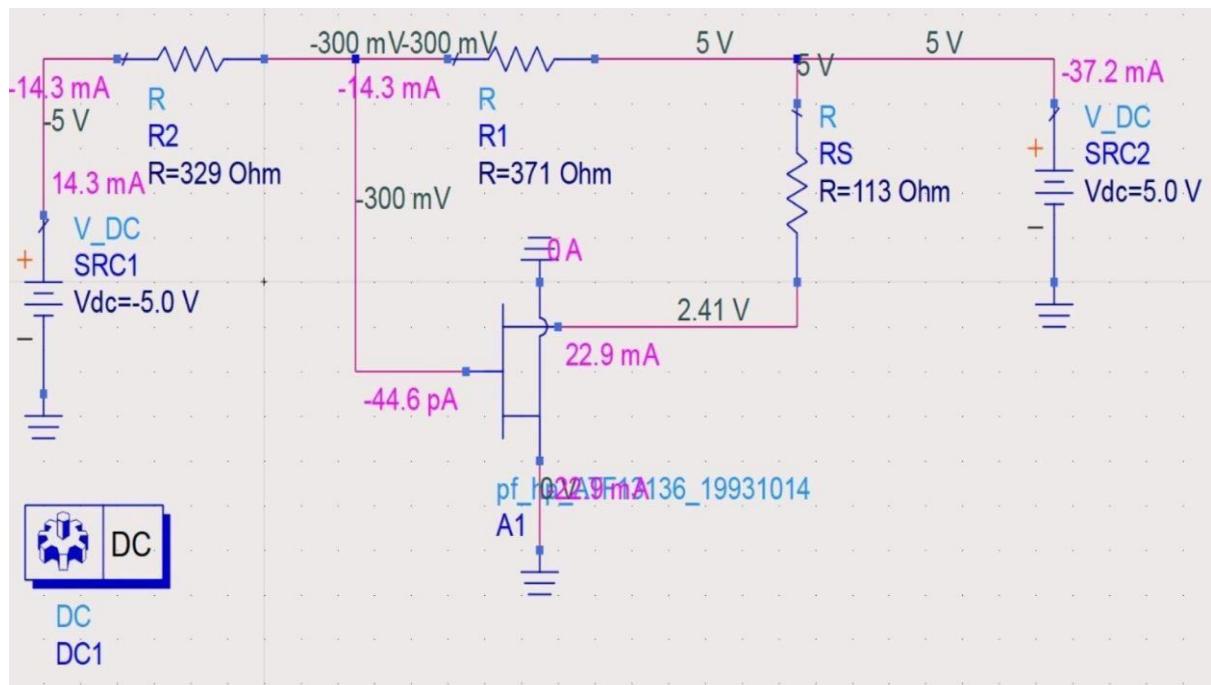


Figure 12 - DC Bias Circuit Simulation

To ensure stability of the Q point, a Voltage Divider Bias Network was utilized in conjunction with a common source topology, where resistor R1 served as feedback resistance providing negative feedback. The circuit employed two power supplies, VDD and VGG, to apply forward and reverse bias to the drain to source and gate to source terminals respectively, while the source was grounded. This configuration resulted in better gain and NF than alternative topologies.

5.2.2 Stability Network Circuit Design (RF/ Microwave Circuit Design)

Designing steps for RF/ Microwave circuit design;

1. Choosing a transistor based on the noise figure along with gain requirements, by considering the S-parameters of the device at specific frequency.
2. DC biasing of the transistor at definite Q point as per mentioned in the datasheet.
3. Determining S-parameters from the datasheet and verify it through simulations for particular values of VDS and IDS.

4. Stability conditions of the transistor are to be checked at a specific frequency with a K- Δ test where the value of stability factor should be greater than 1, and $|\Delta|$ less than 1.
5. If the transistor is not stable for a particular value of frequency, draw stability circles on smith chart to find the stable regions.
6. There are two possible circumstances. For $S_{12} = 0$, use formulas of unilateral design. For $S_{12} \neq 0$, calculate a unilateral figure of merit along with the error range. For small error range, use unilateral analysis otherwise bilateral analysis for design.
7. Design a matching network by using hand calculation values as well as smith chart for the amplifier design.

To determine S-parameters, NF and stability, the schematic is drawn as per Figure 13.

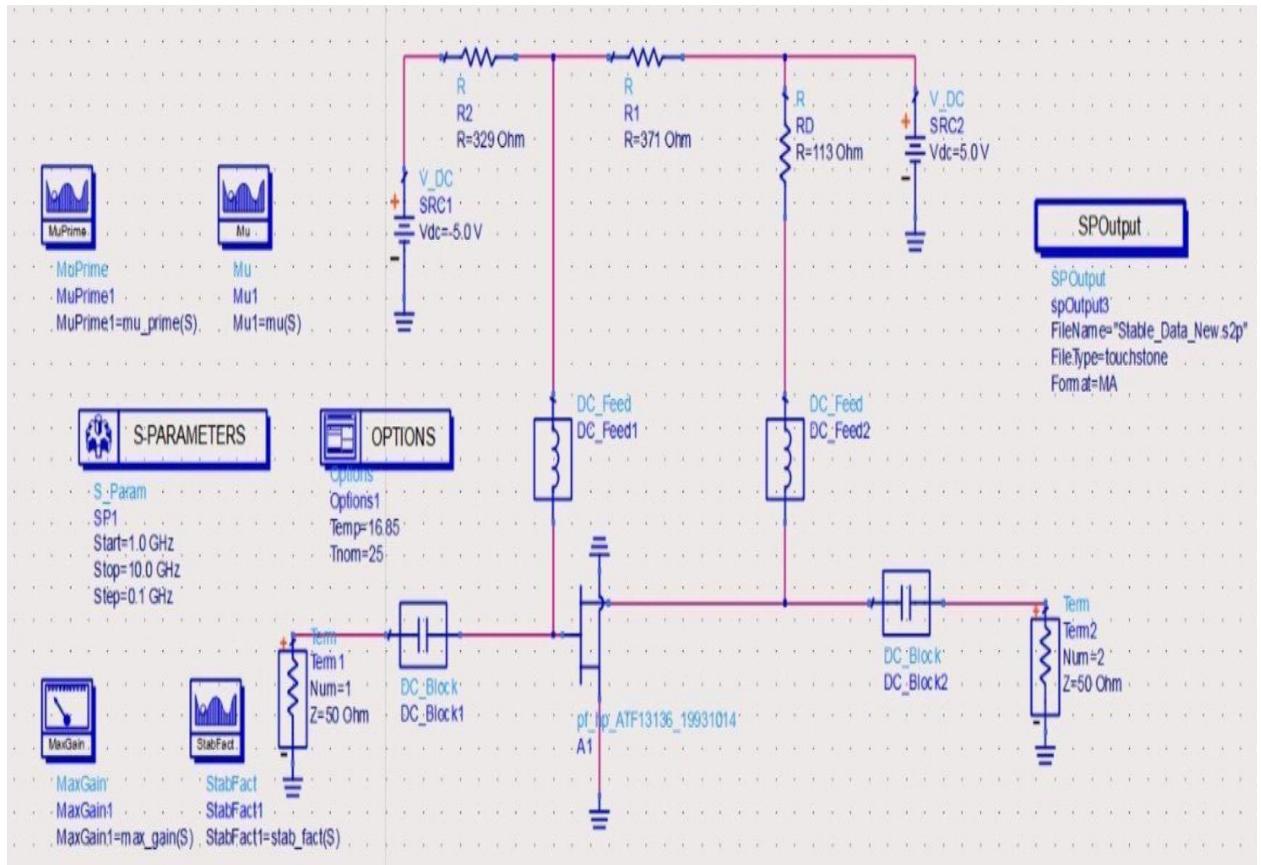


Figure 13 - S-Parameter Simulation Setup

S-parameter simulation is a technique used in the field of electrical engineering to analyze and characterize the behavior of electronic circuits and systems, especially in high-frequency applications. The "S" in S-parameters stands for scattering, and the technique involves measuring the way that electromagnetic waves scatter or reflect off a circuit or device. S-parameter simulation allows engineers to predict and analyze the performance of a circuit or system before it is actually built, which can save time and money in the design process. By simulating how electromagnetic waves will propagate through a circuit or system, engineers can optimize the design to minimize losses, maximize power transfer, and reduce interference and noise. Overall, S-parameter simulation is a powerful tool that enables engineers to design and optimize electronic circuits and systems with greater accuracy, efficiency, and reliability.

DC Blocks and DC Feeds are important components in RF and microwave circuits that serve to isolate DC (direct current) signals from RF (radio frequency) signals. DC Blocks are passive devices that prevent DC current from flowing through the RF transmission line while allowing RF signals to pass through. DC Feeds, on the other hand, allow DC current to pass through while blocking RF signals. These components are commonly used in amplifiers, mixers, and other RF circuits to prevent unwanted interference or damage from DC current. Proper selection and placement of DC Blocks and DC Feeds can significantly improve the performance and reliability of RF and microwave circuits.

After simulation of the schematic Figure 13, maximum gain and stability factor is plotted as per Figure 14 to see whether ATF13136 with DC bias circuit is stable at desired frequency. In Figure 14, it can be seen that the maximum gain is 13.027 and stability factor is 0.945 (less than 1) at 6 GHz. The LNA might be unstable so the LNA need to be stabilized.

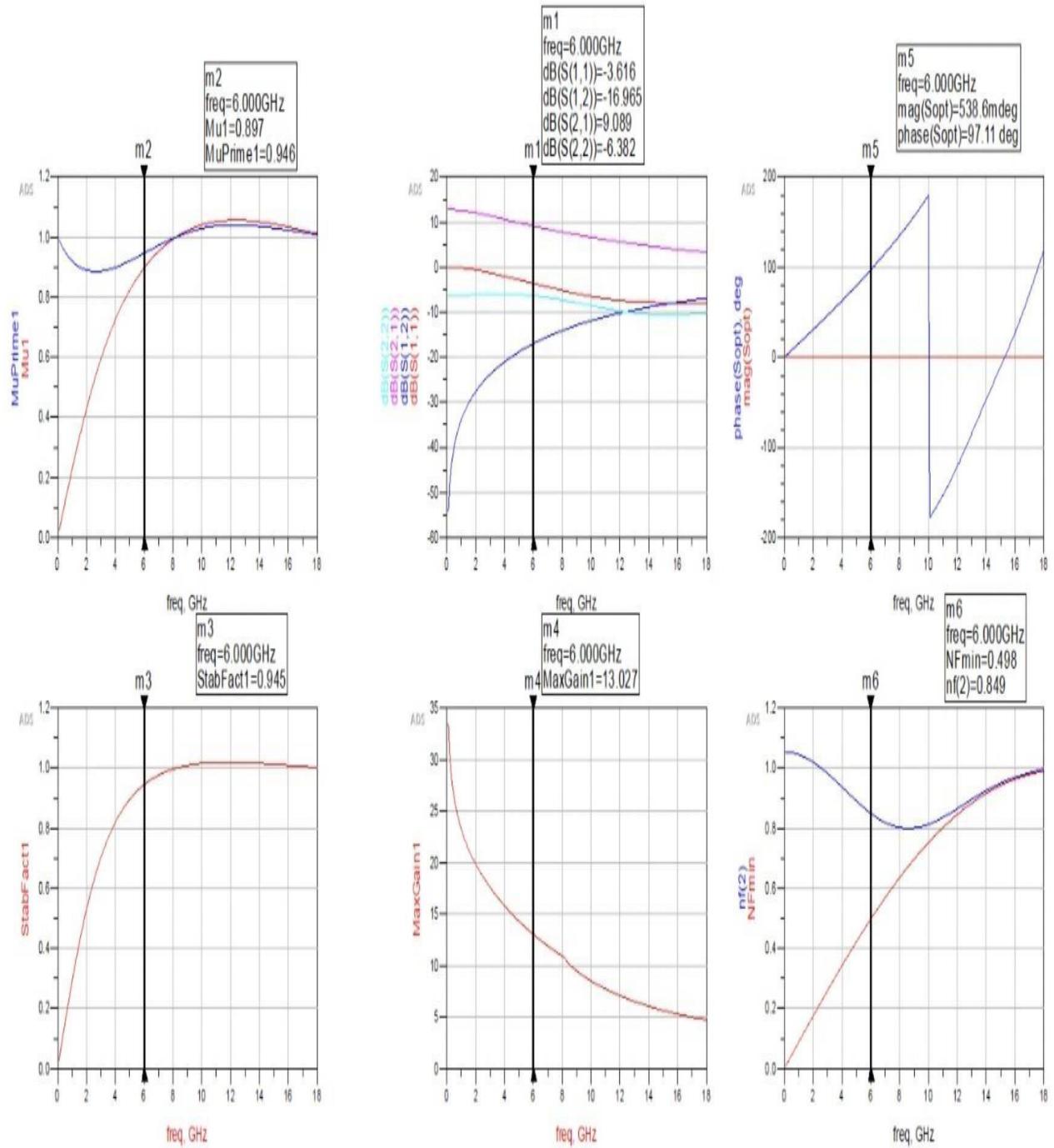


Figure 14 - S-Parameter Simulation Output

To improve the stability of the system, a negative feedback is commonly used. In our design, two small inductors are added at both sources of the ATF13136 to create the feedback path (Figure 15). We also used series and shunt resistances at input and output of the GaAs FET to enhance the stability factor over the entire (2 GHz to 18 GHz) operating range at the expense of Gain and NF, making it unconditionally stable.

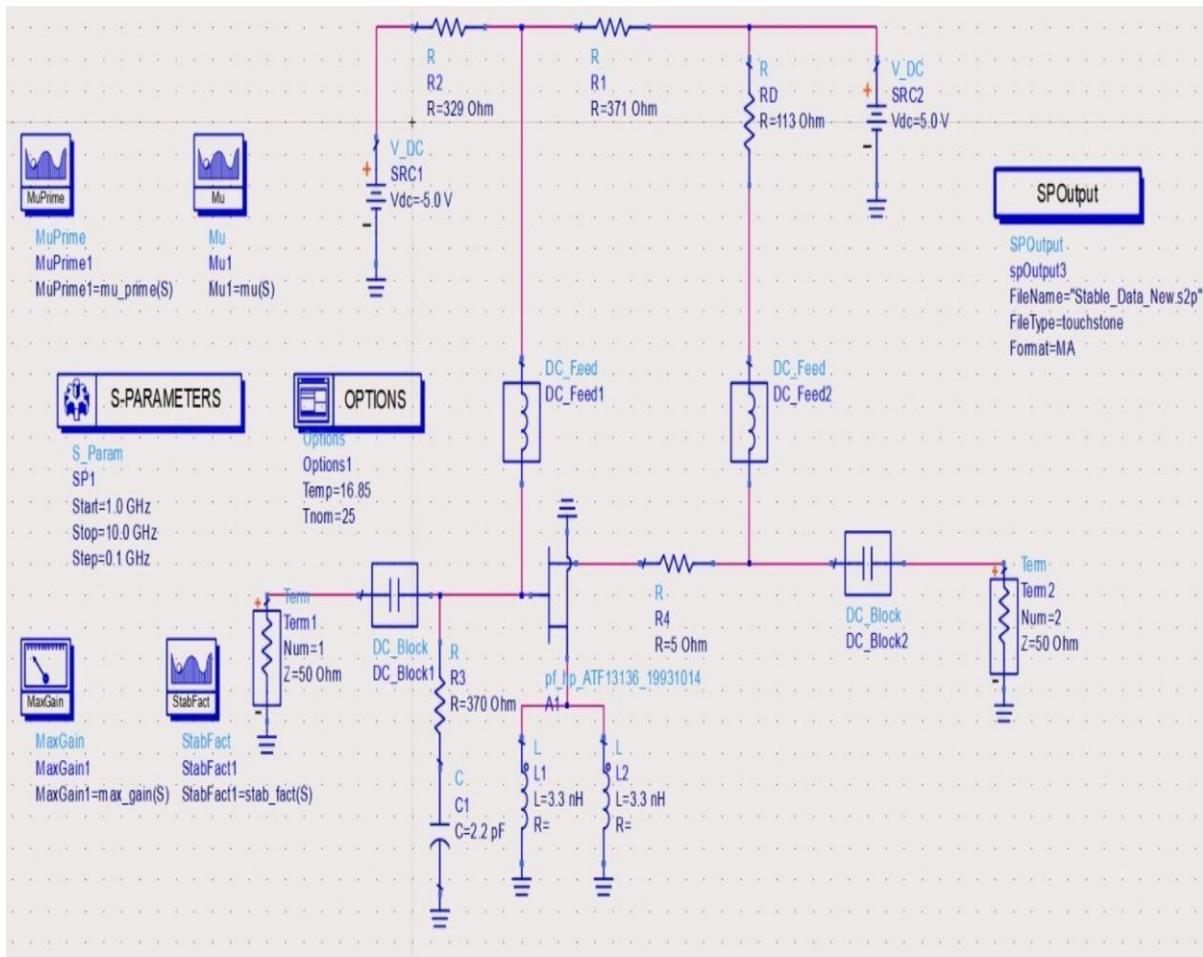


Figure 15 - Noise Optimization using Inductive Source Degeneration

Source inductive degeneration is a technique used in the design of amplifier circuits to improve their stability and performance. It involves the use of an inductor in series with the source terminal of a transistor, which acts as a resistive element at low frequencies but as an inductive element at high frequencies.

The simulation results of the schematic (Figure 15) show that due to negative feedback, the maximum gain is reduced from 13.027dB to 11.166dB as depicted in Figure 16. However, the implementation of source inductive degeneration along with series and shunt resistances at the input and output of the GaAs FET has achieved unconditional stability over the entire operating range (2 GHz - 16 GHz).

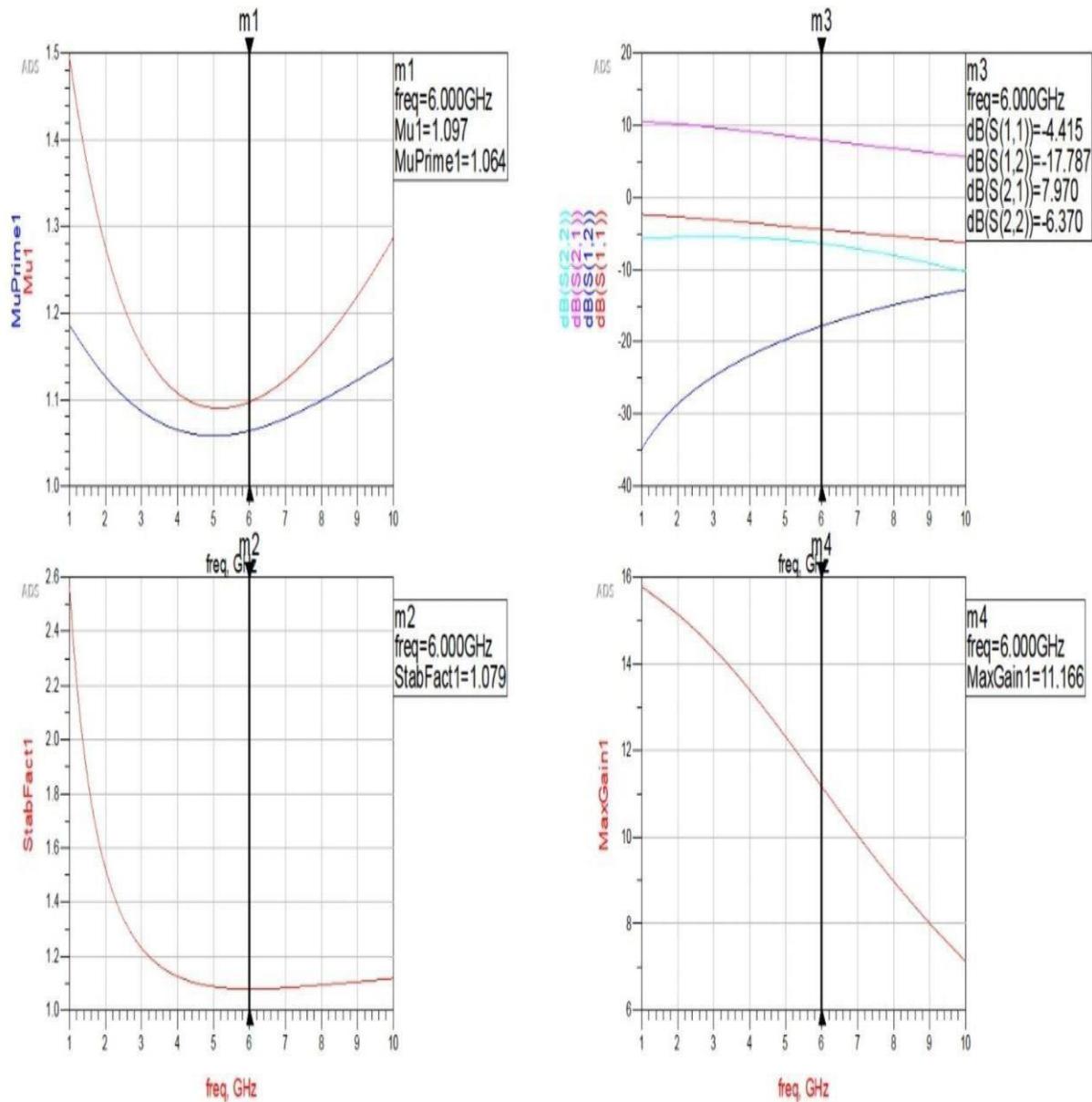


Figure 16 - Output of the Noise Optimization of Amplifier block

Noise optimization in LNA design is crucial for achieving high signal sensitivity and overall system performance. Techniques such as transistor selection, biasing, and matching networks are used to minimize added noise and maximize signal gain. Advanced techniques such as noise canceling and impedance matching can further enhance LNA noise performance.

The DC Feed network was modified by replacing the ideal components with real inductors shown in Figure 17. The inductance values were calculated using the formula given in Figure 18.

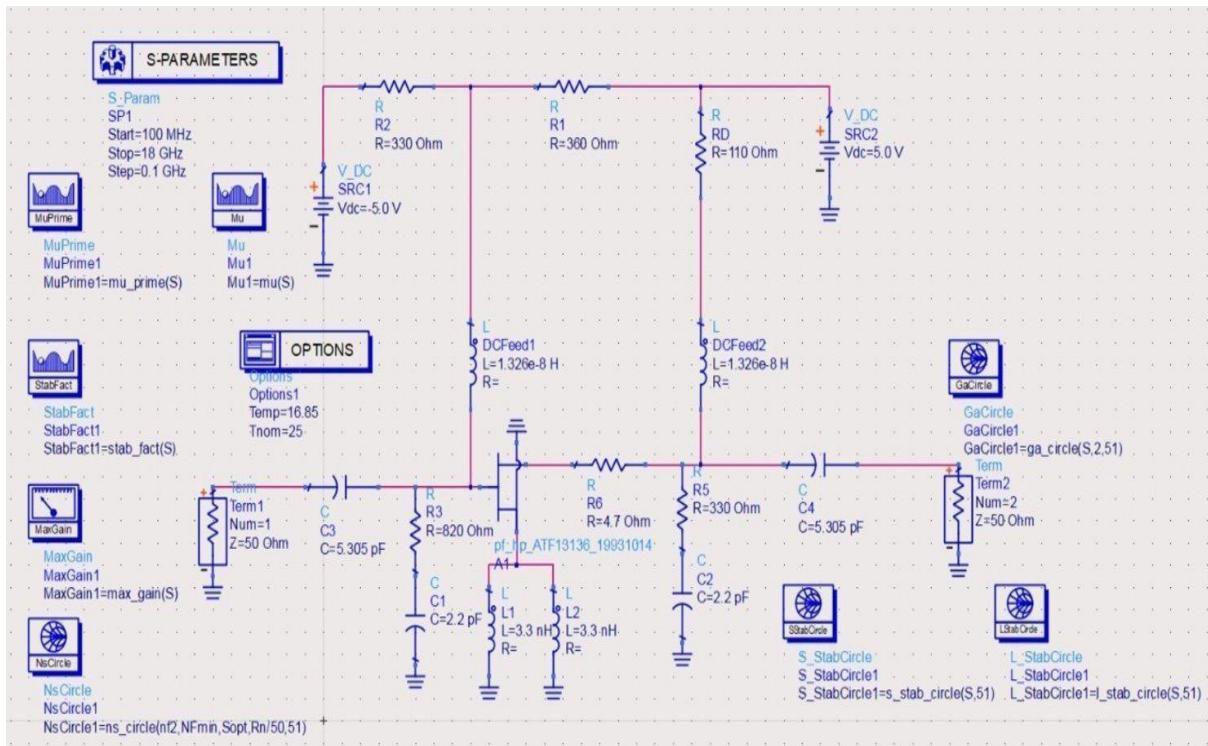


Figure 17 - Replacing the Ideal Block and Feed as Real Values

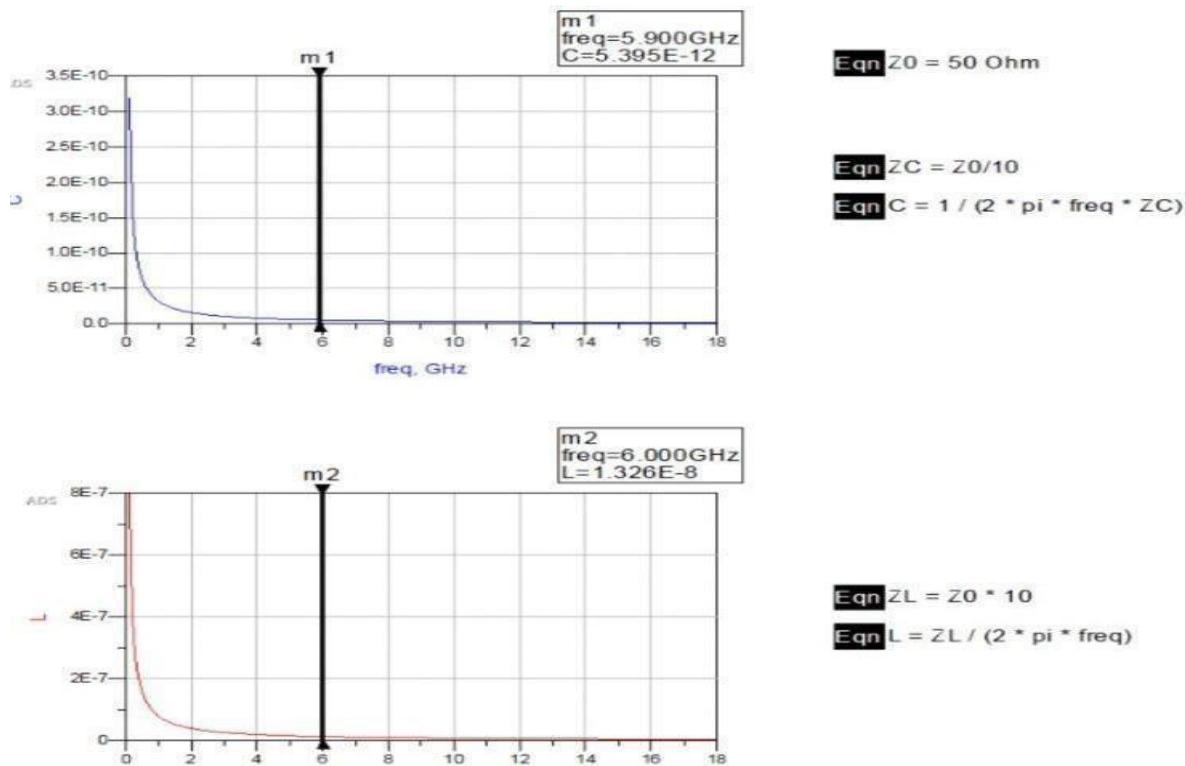


Figure 18 - Real Block Capacitance and Feed Inductance Calculation

The results obtained after replacing the above DC Block and DC Feed with real capacitor and inductor values is shown in the figure 19.

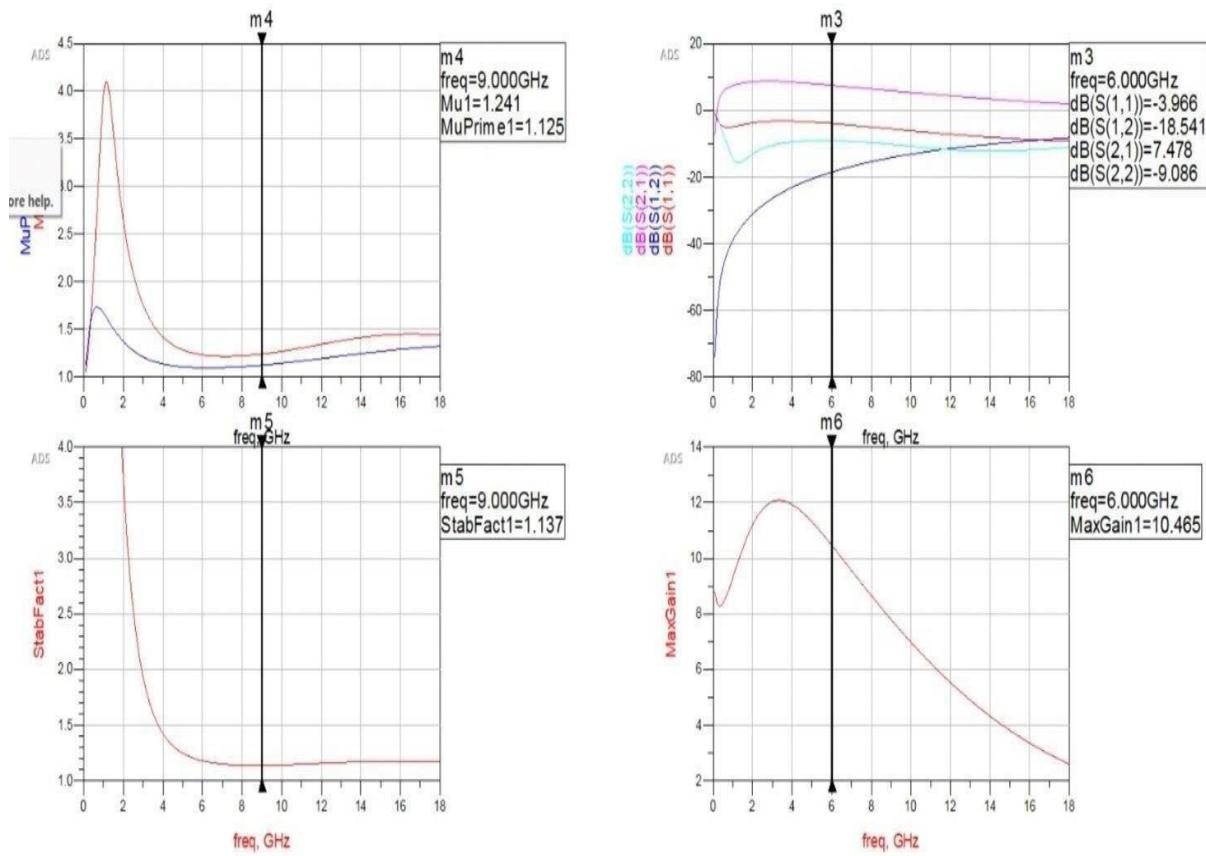


Figure 19 - S-Parameter Simulation Output of Amplifier with Real DC Block and DC Feed

Based on the plotted source and load stability circles in Figure 20, it can be concluded that the designed small signal amplifier is stable.

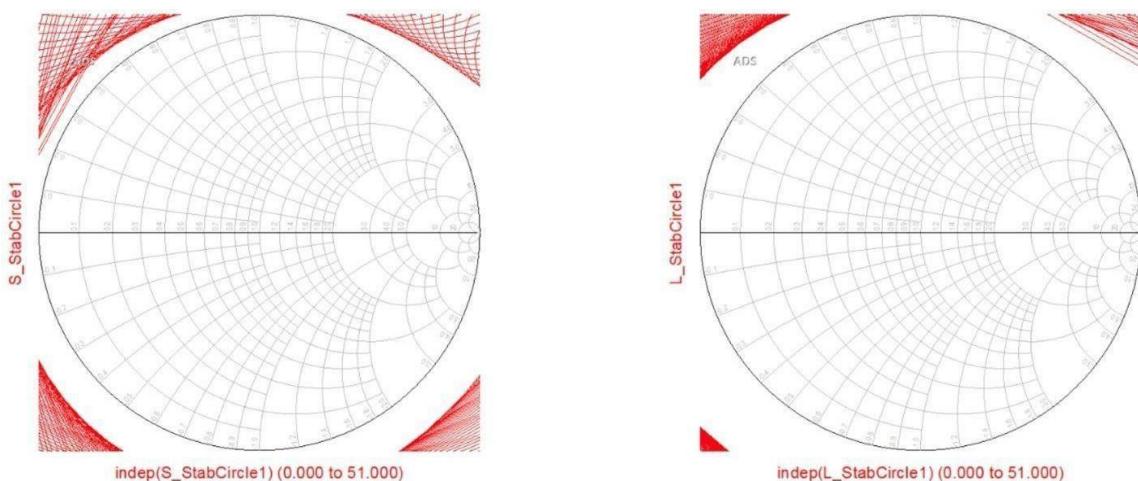


Figure 20 - Source and Load Stability Circles

Therefore, after optimizing the values of resistors, capacitors, and inductors, a small signal amplifier was designed to achieve better performance. The resulting schematic of the small signal amplifier is illustrated in Figure 21.

Load and Source Stability Circles are graphical tools used in RF circuit analysis to determine the stability of the circuit. The stability of an amplifier is assessed by examining the relationship between the input and output impedances of the amplifier. The Load and Source Stability Circles represent the range of input and output impedances for which the amplifier will remain stable.

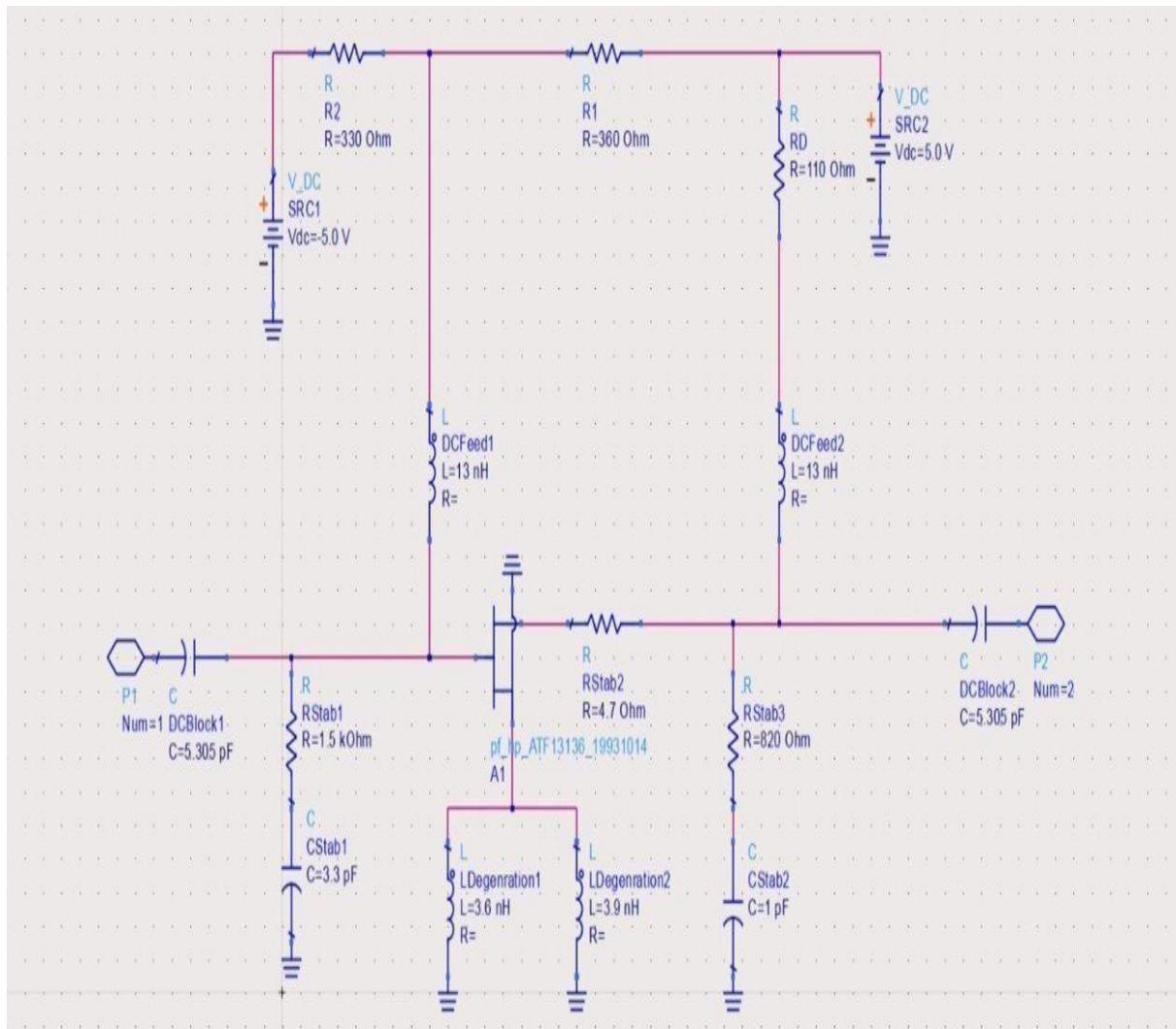


Figure 21 - Basic Amplifier Block

Chapter 6

DESIGNING OF MNA AND MAXIMUM GAIN AMPLIFIER

This chapter talks about the design of every stage of the cascaded amplifier in detail and is divided into three parts:

1. The design of MNA as a single stage using distributed elements.
2. The design of Maximum Gain Amplifier (MGA) as a single stage using distributed elements.
3. The design of a cascaded amplifier using MNA and MGA design.

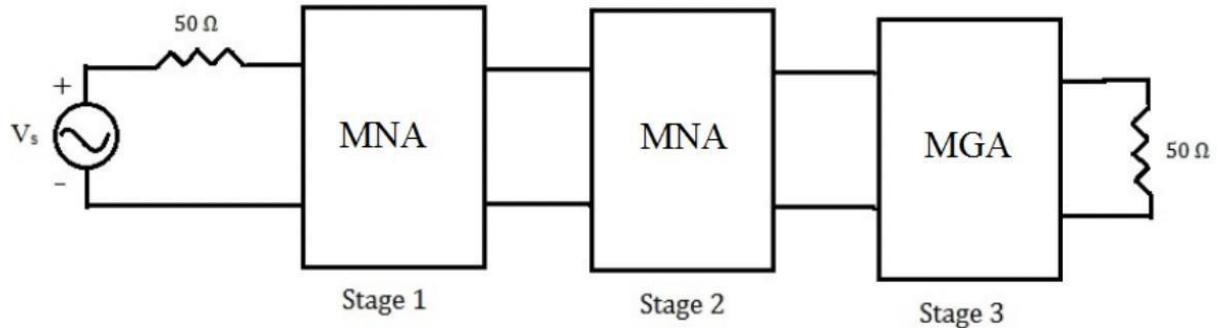


Figure 22 - Block Diagram of Cascaded Design

6.1 DESIGN OF MATCHING NETWORKS

- The key to design a LNA is to keep the noise to the minimum as possible and obtain maximum gain from the design.
- In order to deliver maximum power at an output as well as an input of the design, it is necessary to design the matching networks precisely.
- Matching network can be designed with lumped elements such as resistors, capacitors or else with distributed elements such as transmissionline, stubs.
- In this project, distributed elements are used for designing matching networks as the frequency is quite high.

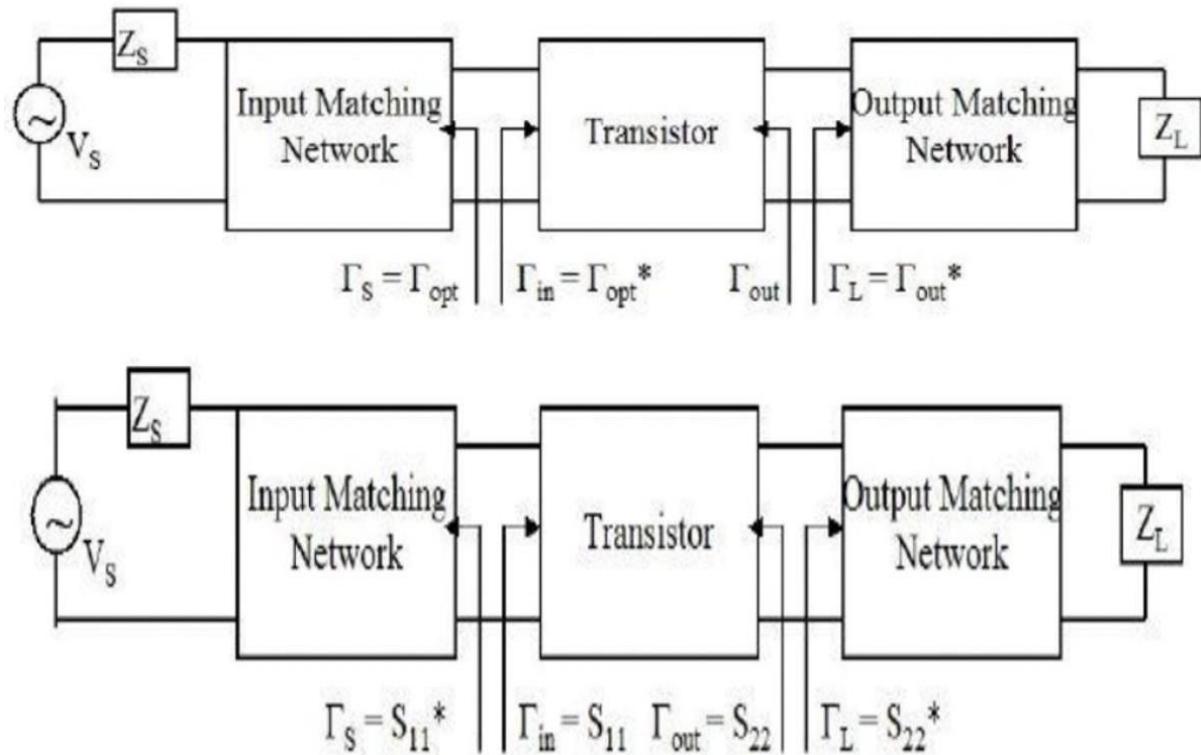


Figure 23 - Matching Network Design Consideration for MNA and MGA

Figure 23 presents the considerations for designing a MNA and Minimum Gain Amplifier. To design a matching circuit, the ESC tool available in ADS software is utilized.

The following steps are followed:

- Determine the source and load impedances to be matched. Enter the characteristic impedance $Z_0 = 50$ Ohms and the central frequency of 6 GHz.
- Enter the load and complex source impedances and lock them. Find the Q circle using the formula $Q = cf/bw$, where cf is the central frequency and bw is the bandwidth.
- Match the load impedance to the source impedance using various lumped and distributed elements available in the component menu.
- Check the circuit return loss performance using the graph tool provided.

6.2 DESIGNING OF MNA

In Figure 24, GammaS and GammaL are plotted in the smith chart along with the required calculations to determine them using S_{opt}. To achieve the lowest NF in the first stage of the amplifier, we choose $\Gamma_S = \Gamma_{opt}$. The reflection coefficients of Γ_L can then be calculated using formulas with the scattering parameters, based on the conjugate matching condition shown in Figure 23.

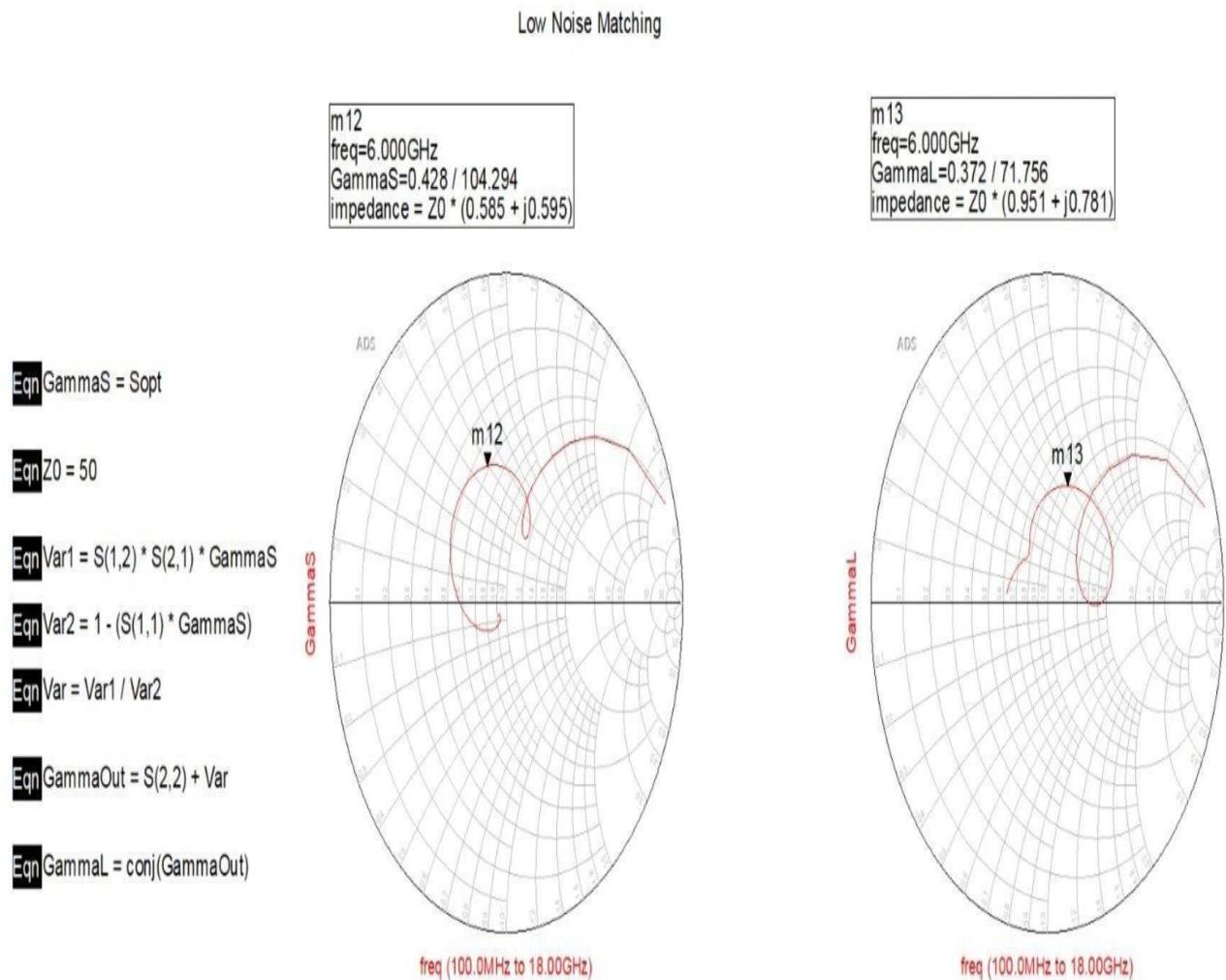


Figure 24 - Low Noise Matching Calculations

Now from the Figure 24 we find that the source impedance and load impedance for our matching circuit is $29.3 + 29.8j$ Ohms and $47.5 + 39j$ Ohms.

6.2.1 Designing of MNA Setup

Now from the Figure 25 we find that the source impedance and load impedance are matched to the input and output circuits using the smith chart (smart component) available in the ADS software.

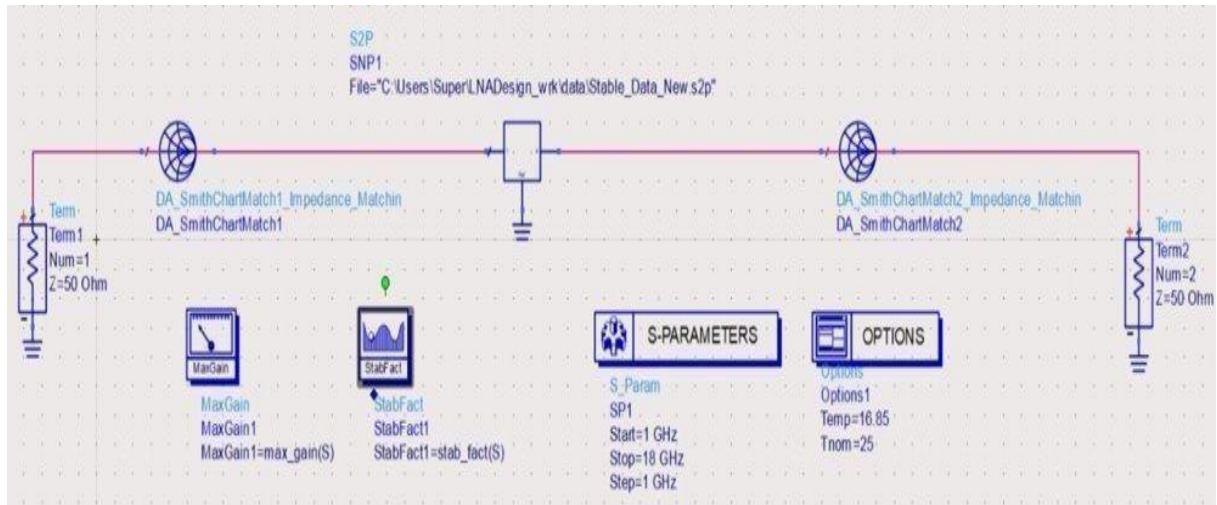


Figure 25 – Designing of MNA Setup

6.2.2 Smith Chart Matching for Input Impedance Matching of MNA

The input impedance matching is performed using the ESC available in the ADS software. Figure 26 shows the trace of the impedance matching on the ESC. Figure 27 shows its schematic in the ADS Advanced Design System Software.

Input impedance matching is a technique used to match the input impedance of an electronic circuit with the output impedance of the source. This is important to minimize signal reflections and optimize power transfer between the source and the circuit. A mismatch in input impedance can lead to loss of signal power and distortion, particularly in high-frequency applications. Techniques such as using matching networks or adding inductors or capacitors in the circuit can be used to achieve input impedance matching.

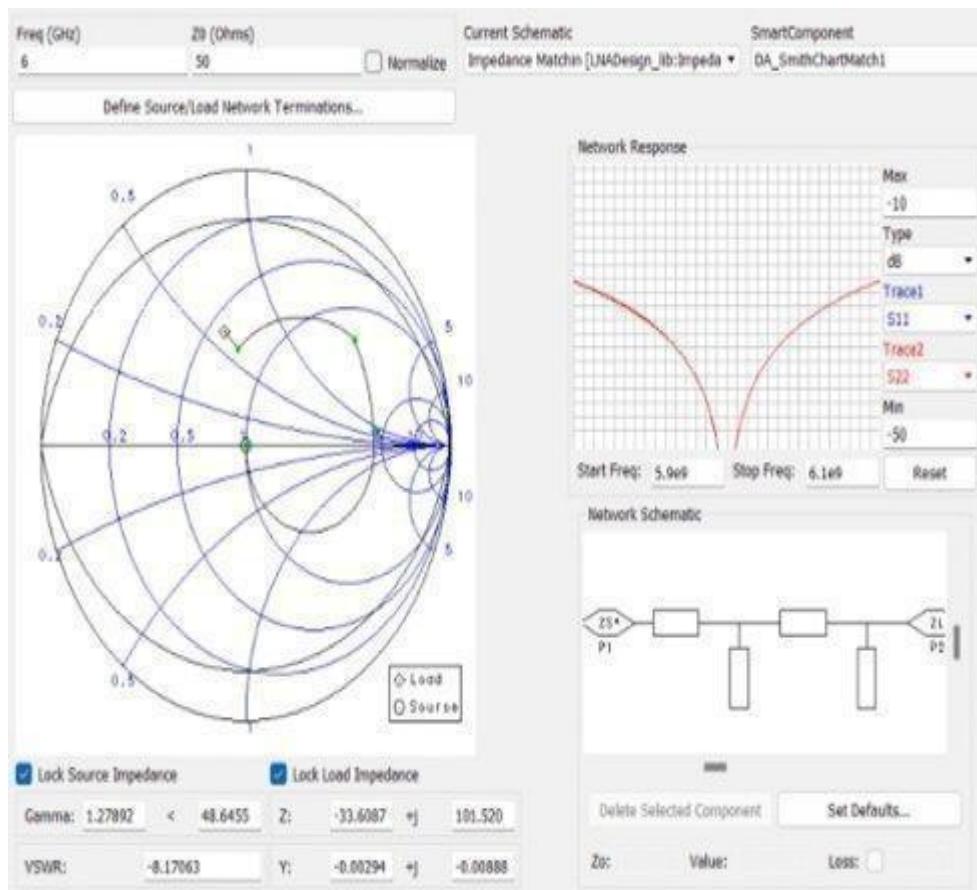


Figure 26 – Input Impedance Matching of MNA using Smith Chart

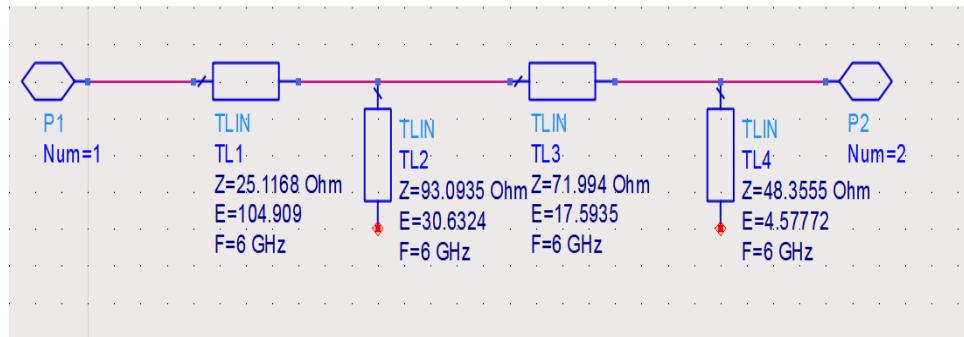


Figure 27 – Input Matching Circuit Schematic (MNA)

6.2.3 Smith Chart Matching for Output Impedance Matching of MNA

The output impedance matching is performed using the ESC available in the ADS software. Figure 28 shows the trace of the impedance matching on the ESC. Figure 29 shows its schematic in the ADS Advanced Design System Software.

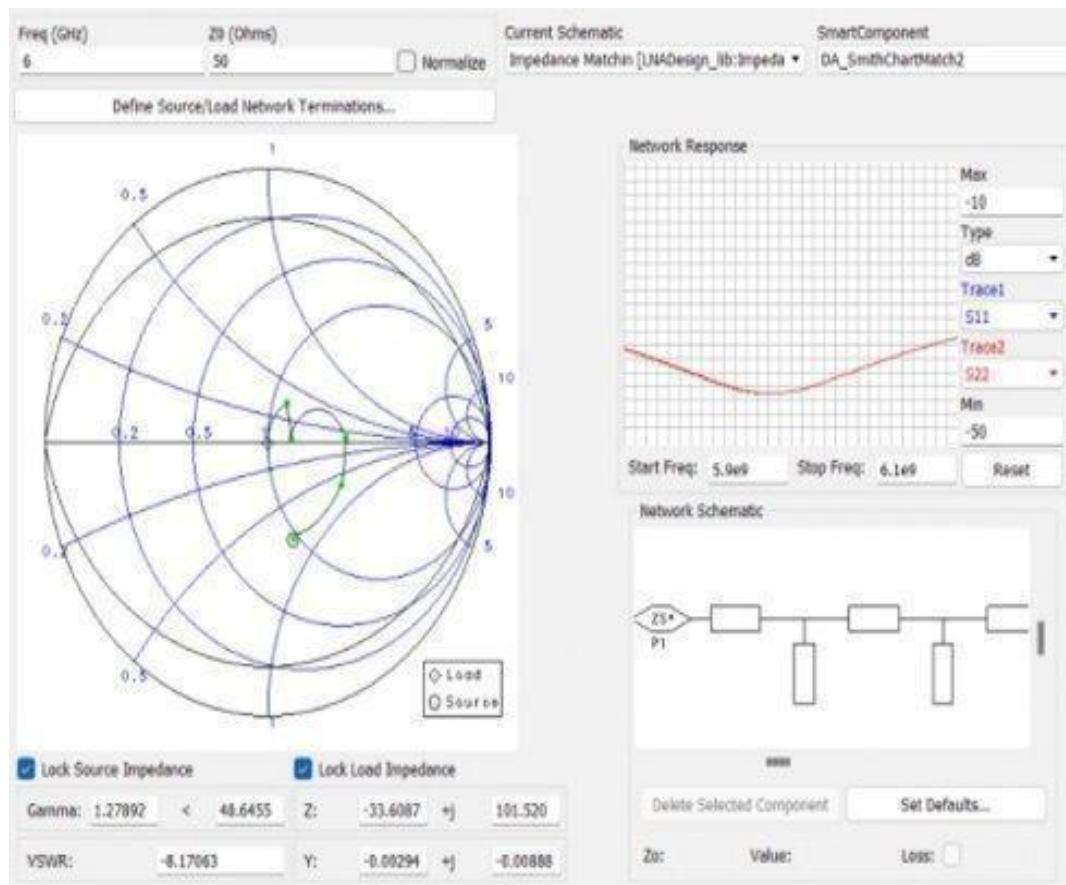


Figure 28 – Output Impedance Matching of MNA using Smith Chart

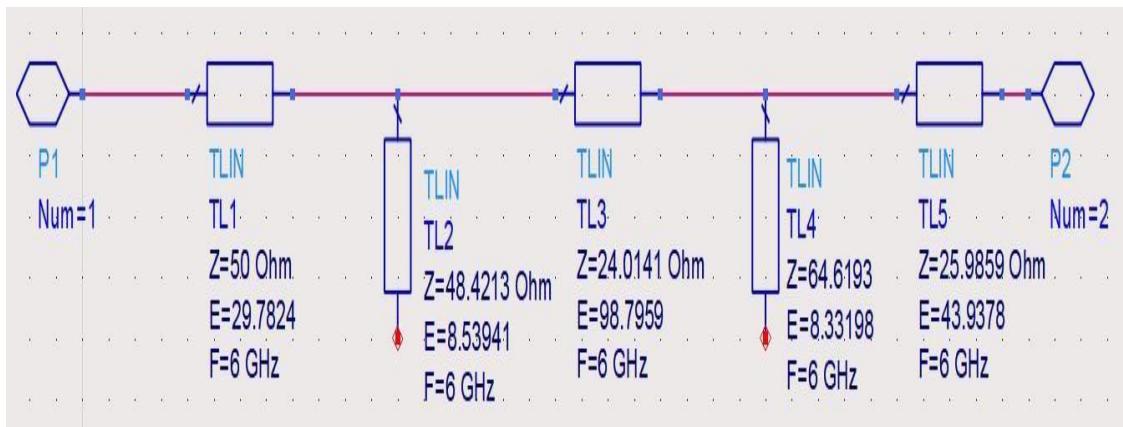


Figure 29 – Output Matching Circuit Schematic (MNA)

6.2.4 Output result of the MNA

In Figure 30 the Maximum Gain, Input and Output Reflection Coefficients, Noise Figure and Stability Factor of the MNA are plotted.

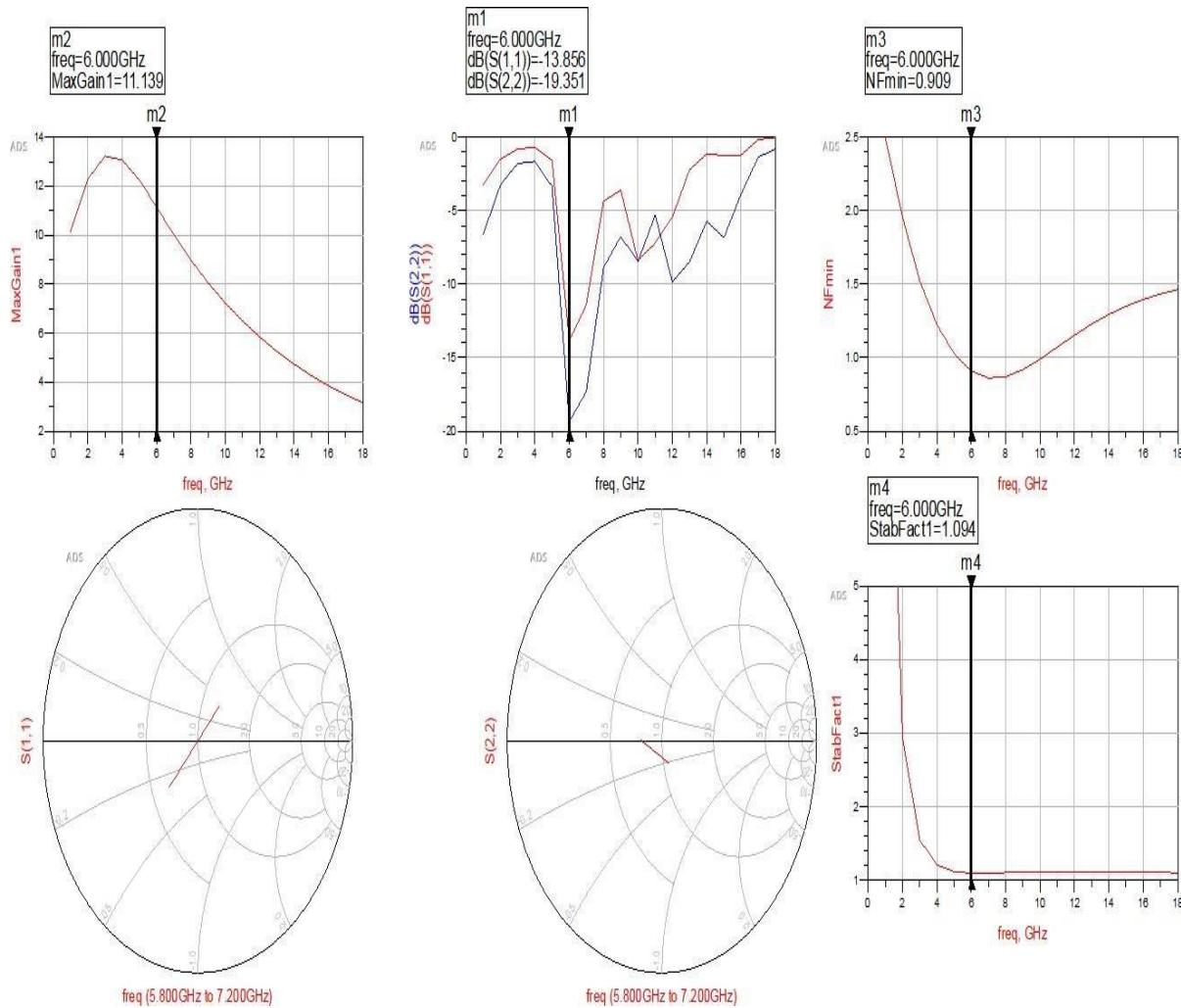


Figure 30 – Output Result of the MNA

In Figure 30 as we see the Input and Output Reflection coefficients (S_{11} and S_{22} respectively) we see that the input and output impedance circuits provide a good matching.

6.3 DESIGNING OF MAXIMUM GAIN AMPLIFIER (MGA)

In Figure 31, Gamma_S and Gamma_L are plotted in the smith chart along with the required calculations to determine them using Sopt. To achieve the Maximum Gain in the final stage of the amplifier, we choose $\Gamma_S = S_{11}^*$. The reflection coefficients of Γ_L can then be calculated using formulas with the scattering parameters, based on the conjugate matching condition shown in Figure 23.

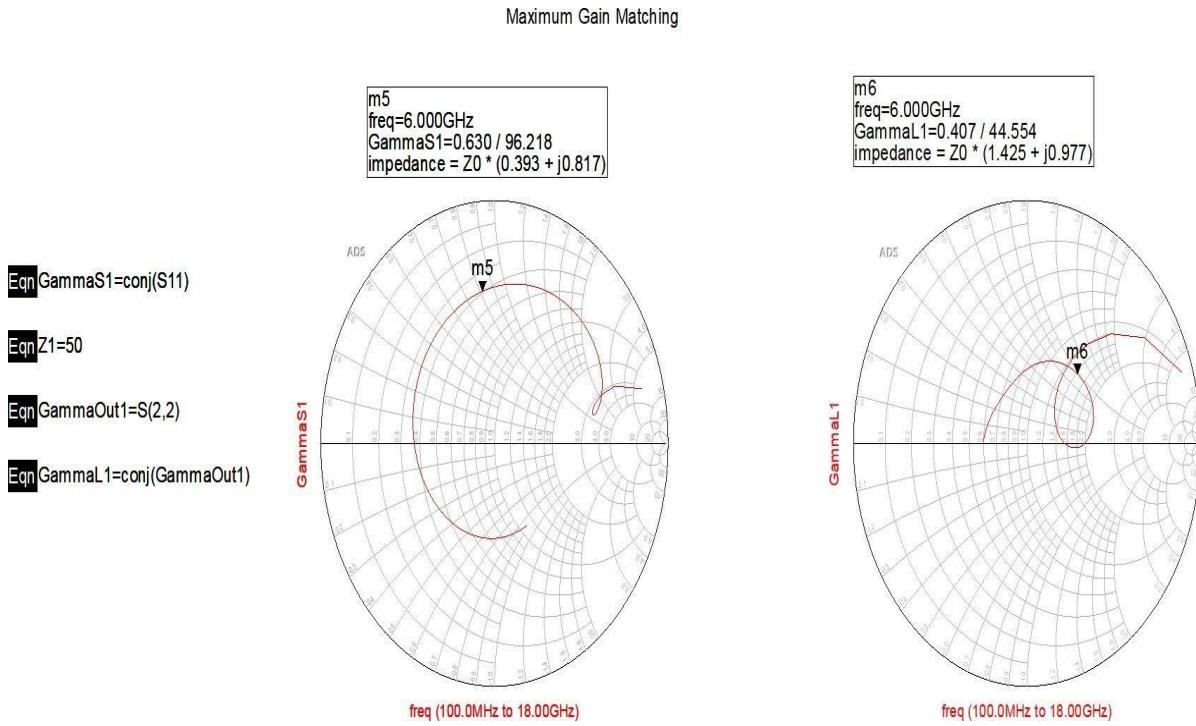


Figure 31 – Finding the Source and Load Impedances for MGA

Now from the Figure 31 we find that the source impedance and load impedance for our matching circuit is $29.3 + 29.8j$ Ohms and $47.5 + 39j$ Ohms.

6.3.1 Designing of Maximum Gain Amplifier Setup

Now from the Figure 31 we find that the source impedance and load impedance are matched to the input and output circuits using the smith chart (smart component) available in the ADS software.

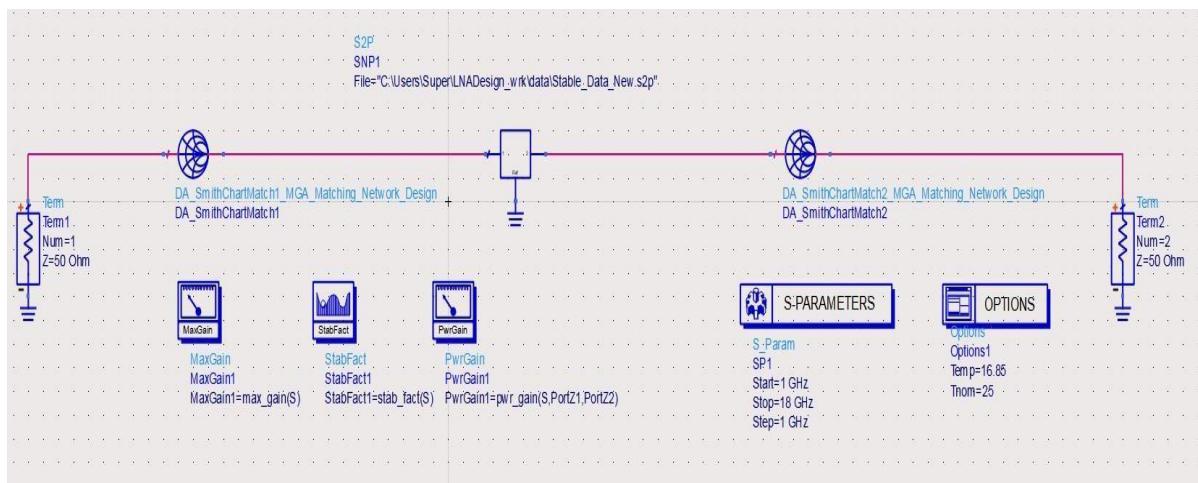


Figure 32 – Designing of Maximum Gain Amplifier Setup.

6.3.2 Smith Chart Matching for Input Impedance Matching of MGA

The input impedance matching is performed using the ESC available in the ADS software. Figure 33 shows the trace of the impedance matching on the ESC. Figure 34 shows its schematic in the ADS Advanced Design System Software.

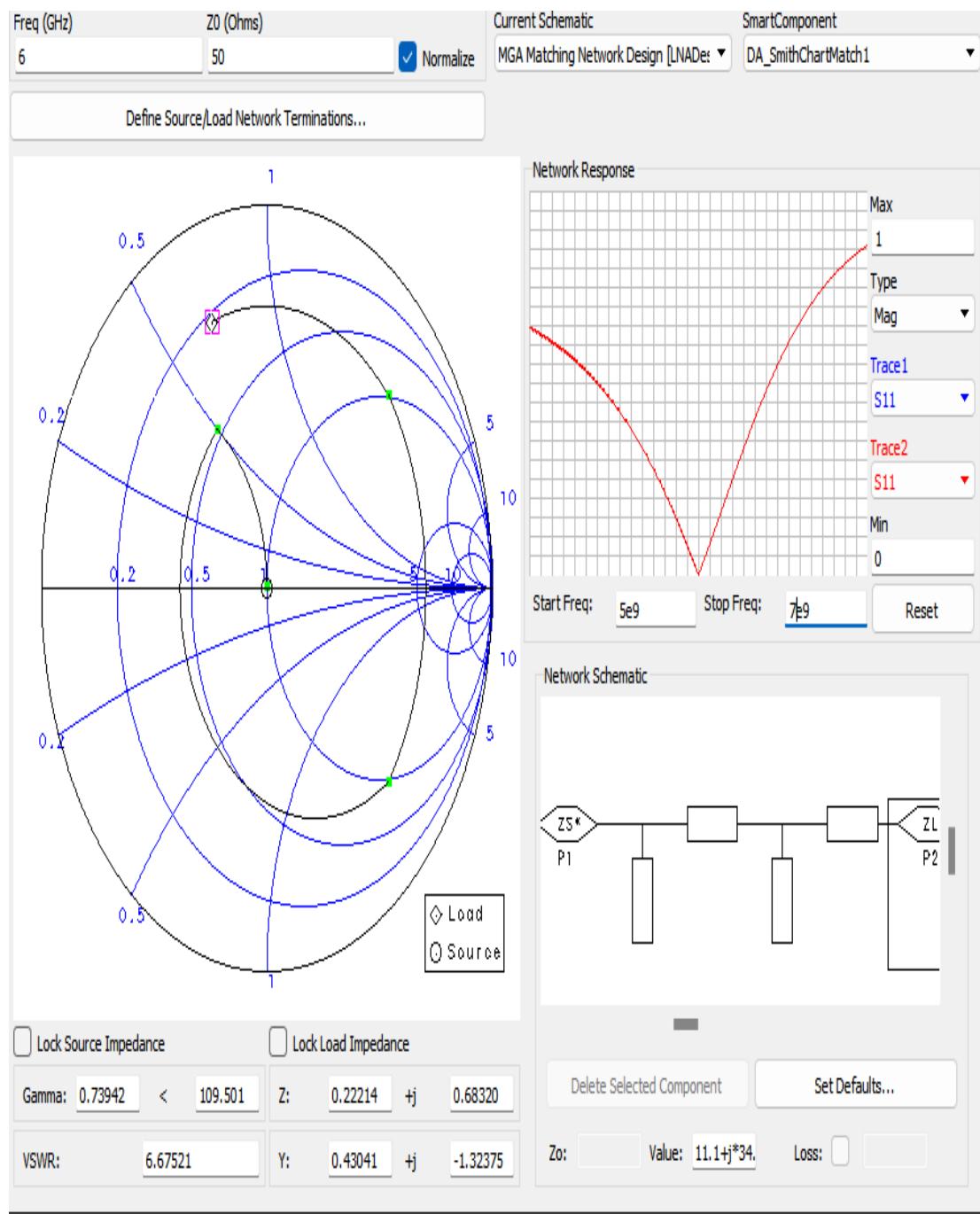


Figure 33 – Input Impedance Matching of MGA using Smith Chart

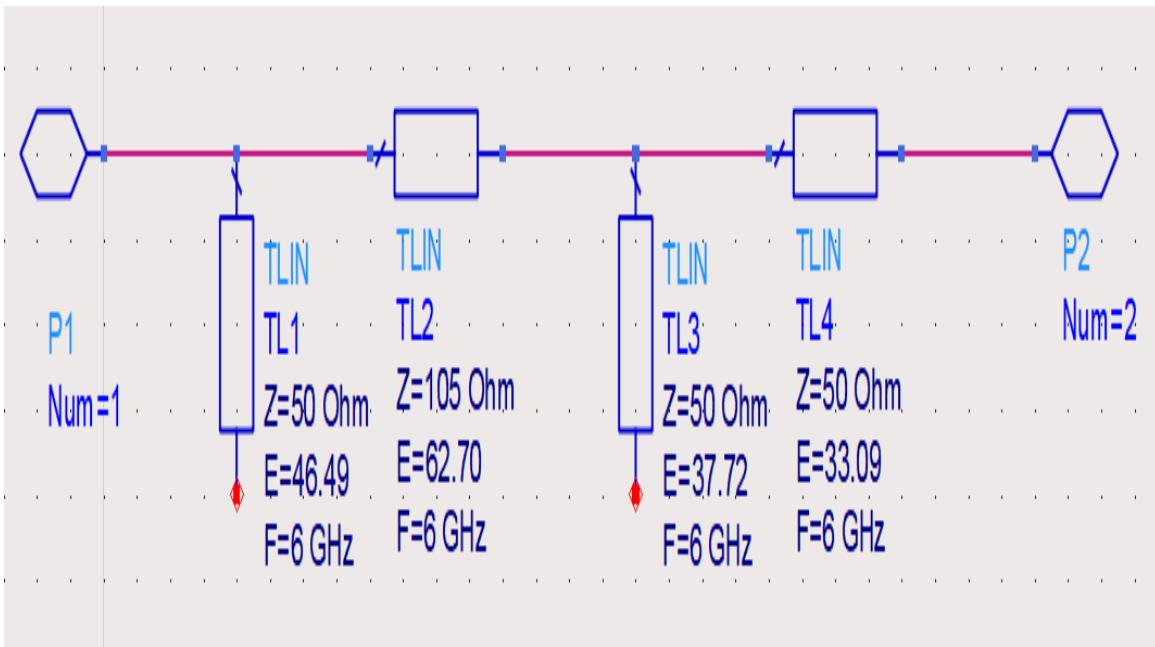


Figure 34 – Input Matching Circuit Schematic (MGA)

6.3.3 Smith Chart Matching for Output Impedance Matching of MGA

The output impedance matching is performed using the ESC available in the ADS software. Figure 35 shows the trace of the impedance matching on the ESC. Figure 36 shows its schematic in the ADS Advanced Design System Software.

Output impedance matching is the process of matching the output impedance of an electronic circuit with the input impedance of the load or receiver. This is important to minimize signal reflections and optimize power transfer between the circuit and the load. A mismatch in output impedance can lead to loss of signal power and distortion, particularly in high-frequency applications. Techniques such as using matching networks, adding resistors or inductors, or using buffer amplifiers can be used to achieve output impedance matching. Thus output impedance matching circuit is employed in the Maximum Gain Amplifier design to ensure the transfer of maximum power from the Maximum Gain Amplifier to the load.

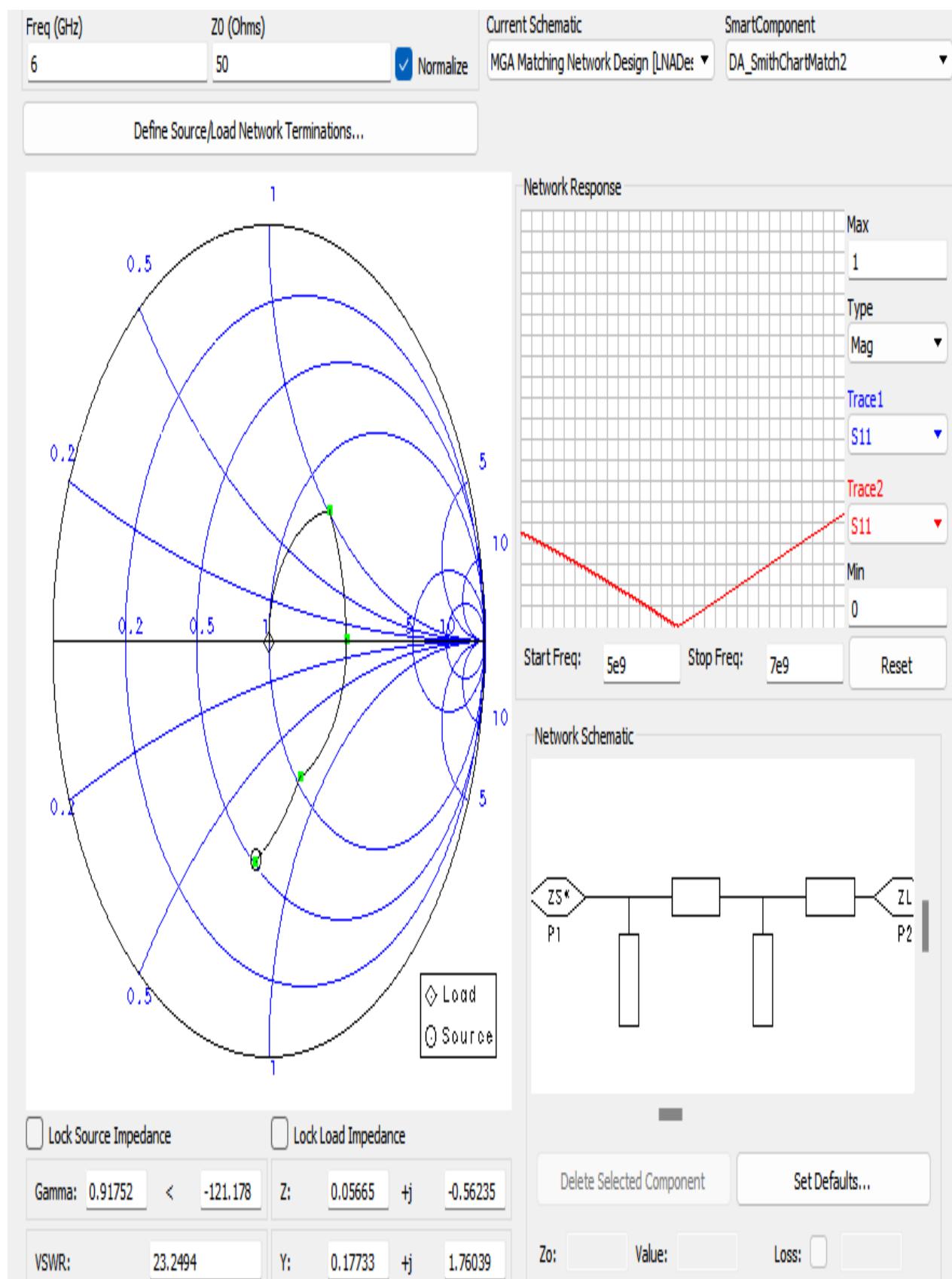


Figure 35 – Output Impedance Matching of MGA using Smith Chart

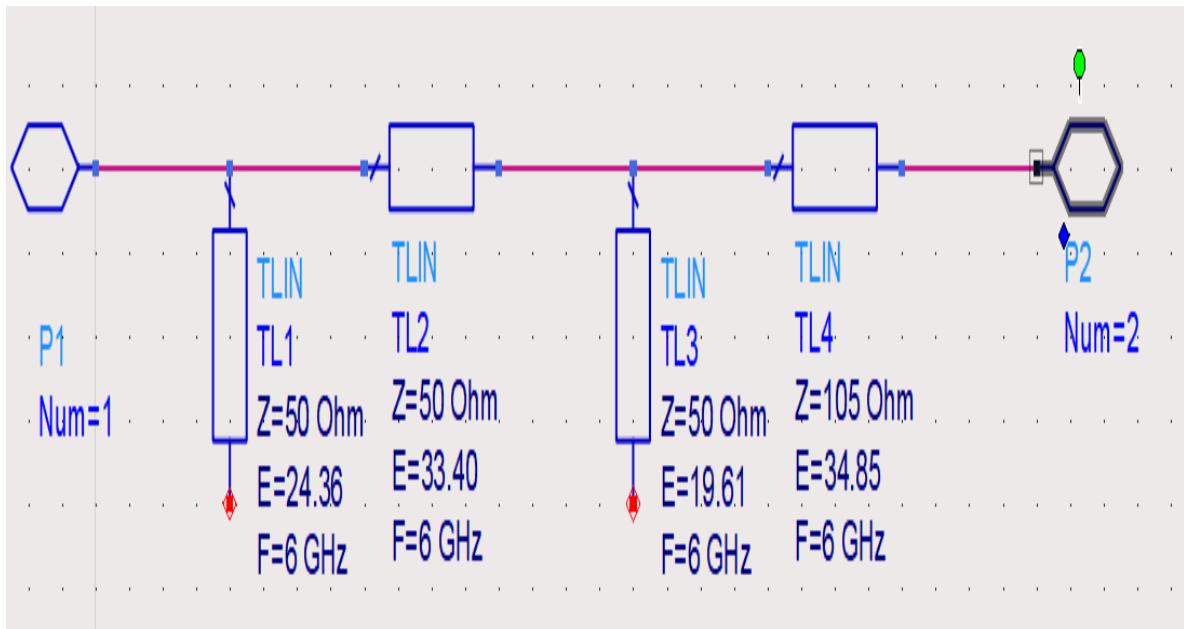


Figure 36 – Output Matching Circuit Schematic (MGA)

6.3.4 Output result of the MGA

In Figure 37 the Maximum Gain, Input and Output Reflection Coefficients, Noise Figure and Stability Factor of the MGA are plotted. Achieving good overall matching in electronic circuits is critical for maximum power transfer and efficient system performance. The use of distributed elements, such as transmission lines and lumped capacitors and inductors, can provide broadband impedance matching and minimize signal reflections. Design considerations include selecting the appropriate transmission line type, impedance, and length, as well as optimizing the capacitance and inductance values of the lumped elements.

MGA design is focused on achieving the highest possible gain with minimum noise and distortion. This involves optimizing the transistor biasing, matching network, and feedback topology to provide maximum voltage gain and stable operation. Trade-offs between gain, bandwidth, and stability must be carefully considered.

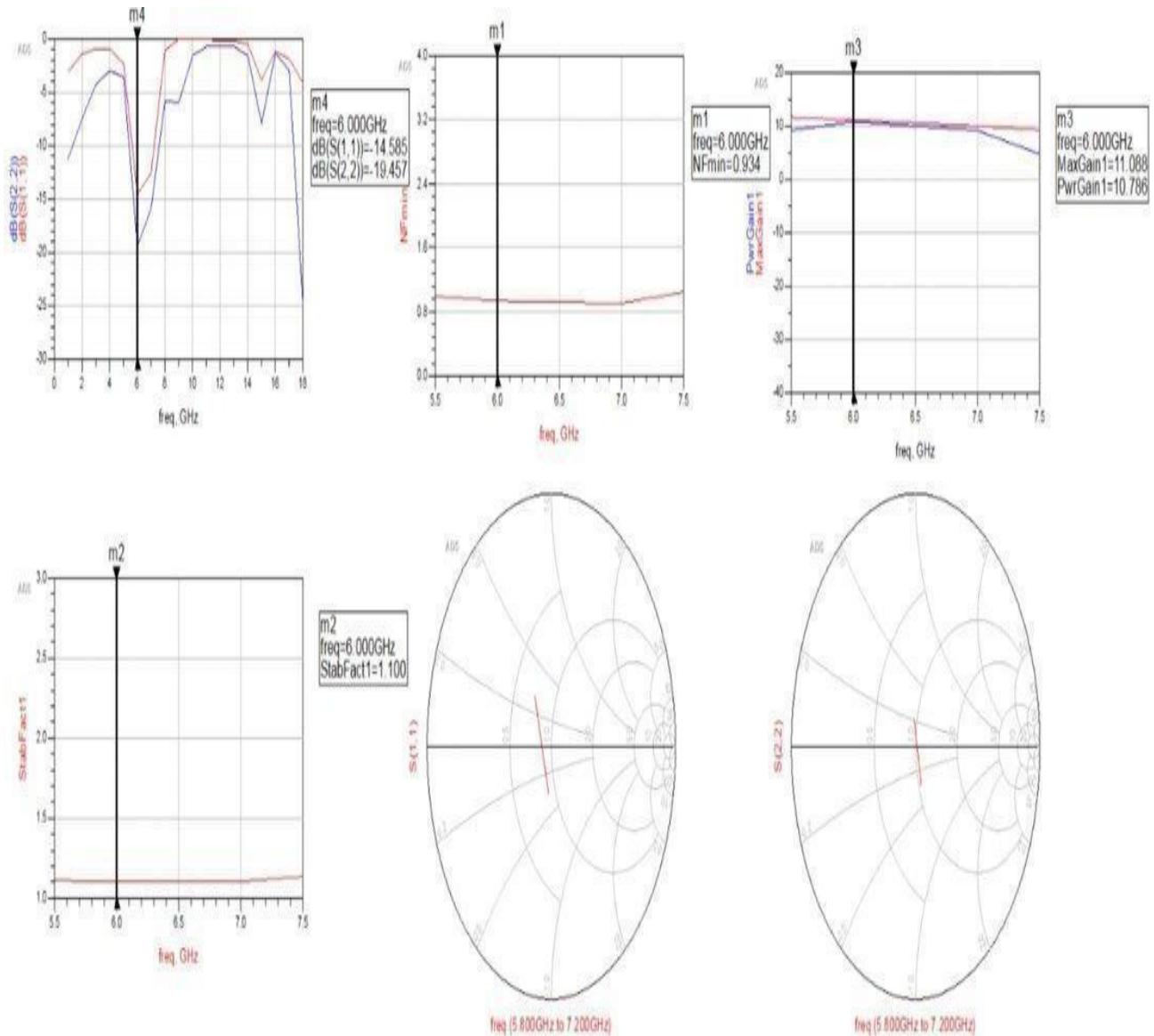


Figure 37 – Output Result of the MGA

In Figure 37 as we see the Input and Output Reflection coefficients (S11 and S22 respectively) we see that the input and output impedance circuits provide a good matching.

6.4 DESIGNING OF CASCADE MNA (CASCADE MNA)

Now we are going to cascade the first two stages of the LNA (First Stage – MNA and the Second Stage – MNA) and design the interstage impedance matching circuit.

6.4.1 Designing of Cascade MNA

Now from the Figure 38 we find that the output impedance of the first stage and input impedance of the second are matched as interstage matching circuits using the smith chart (smart component) available in the ADS software.

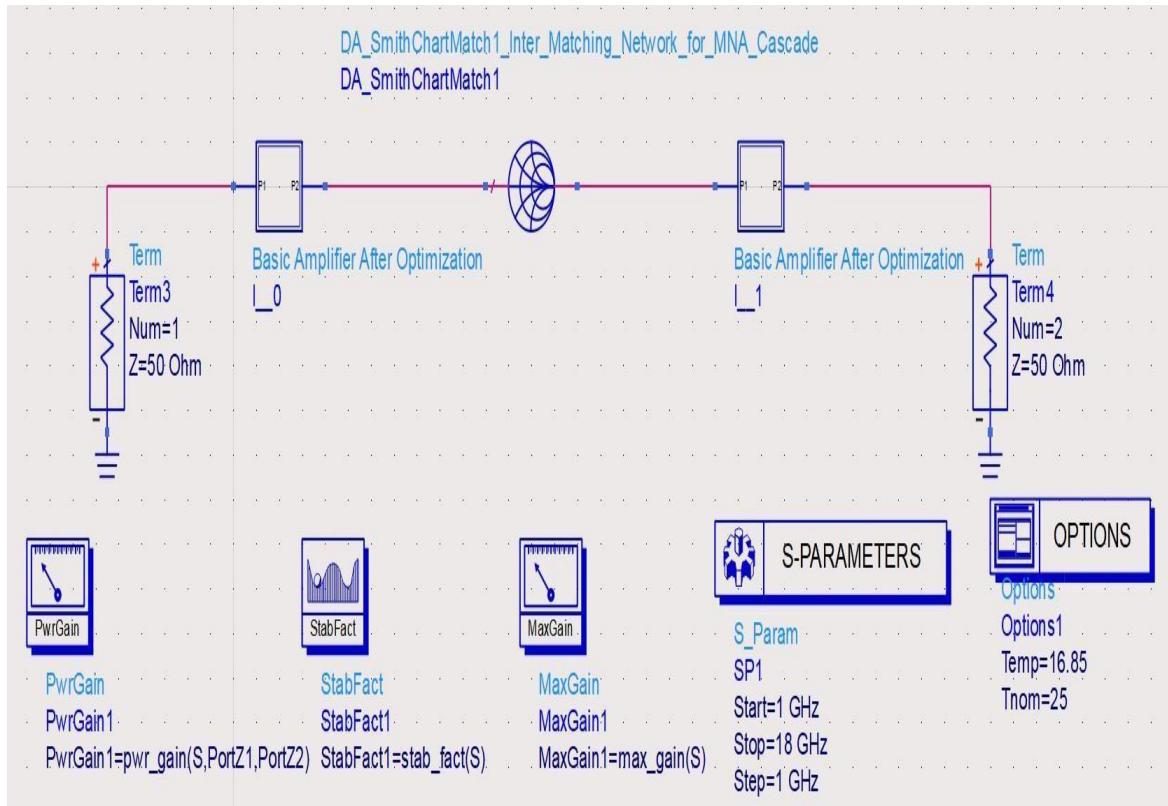


Figure 38 – Designing of Cascade MNA Setup.

6.4.2 Smith Chart Matching for Interstage Impedance Matching of Cascade MNA

The input impedance matching is performed using the ESC available in the ADS software. Figure 39 shows the trace of the impedance matching on the ESC. Figure 40 shows its schematic in the ADS Advanced Design System Software. Cascading refers to the connection of two or more electronic devices or circuits to produce a complex system. It involves connecting the output of one device to the input of the next device in order to increase overall gain or achieve a desired function.

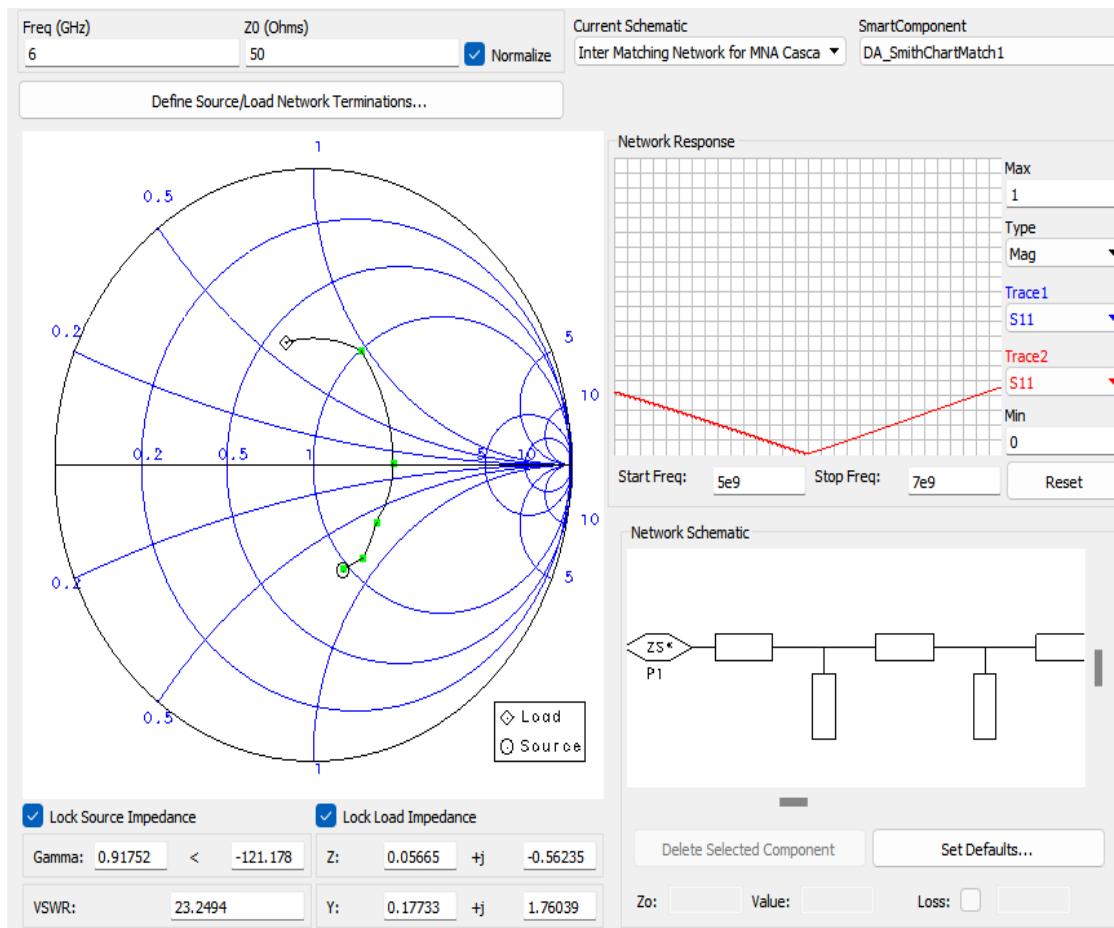


Figure 39 – Input Impedance Matching of MGA using smith chart

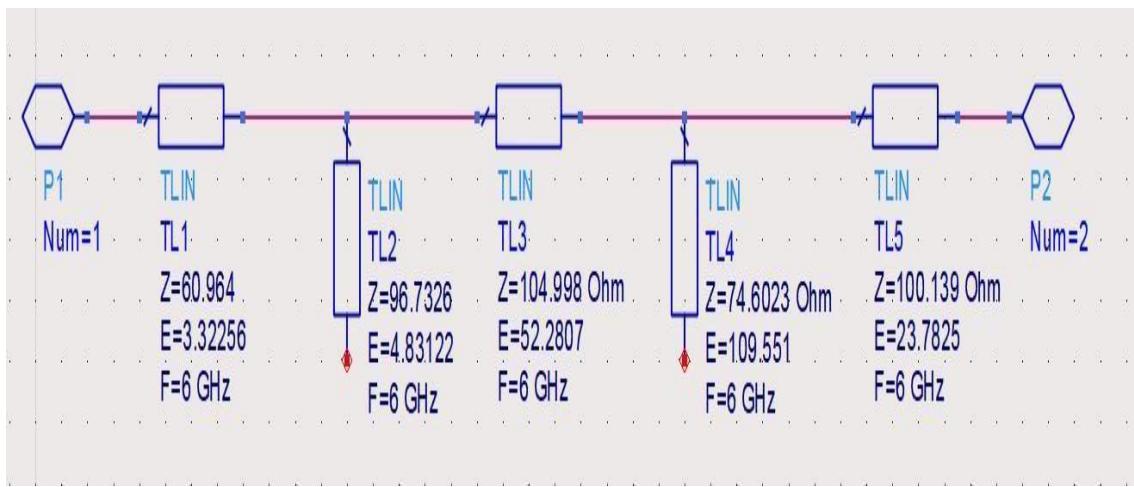


Figure 40 – Interstage Matching Circuit Schematic (Cascade MNA)

6.4.3 Output result of the Cascade MNA

In Figure 41 the Maximum Gain, Input and Output Reflection Coefficients, Noise Figure and Stability Factor of the MNA are plotted.

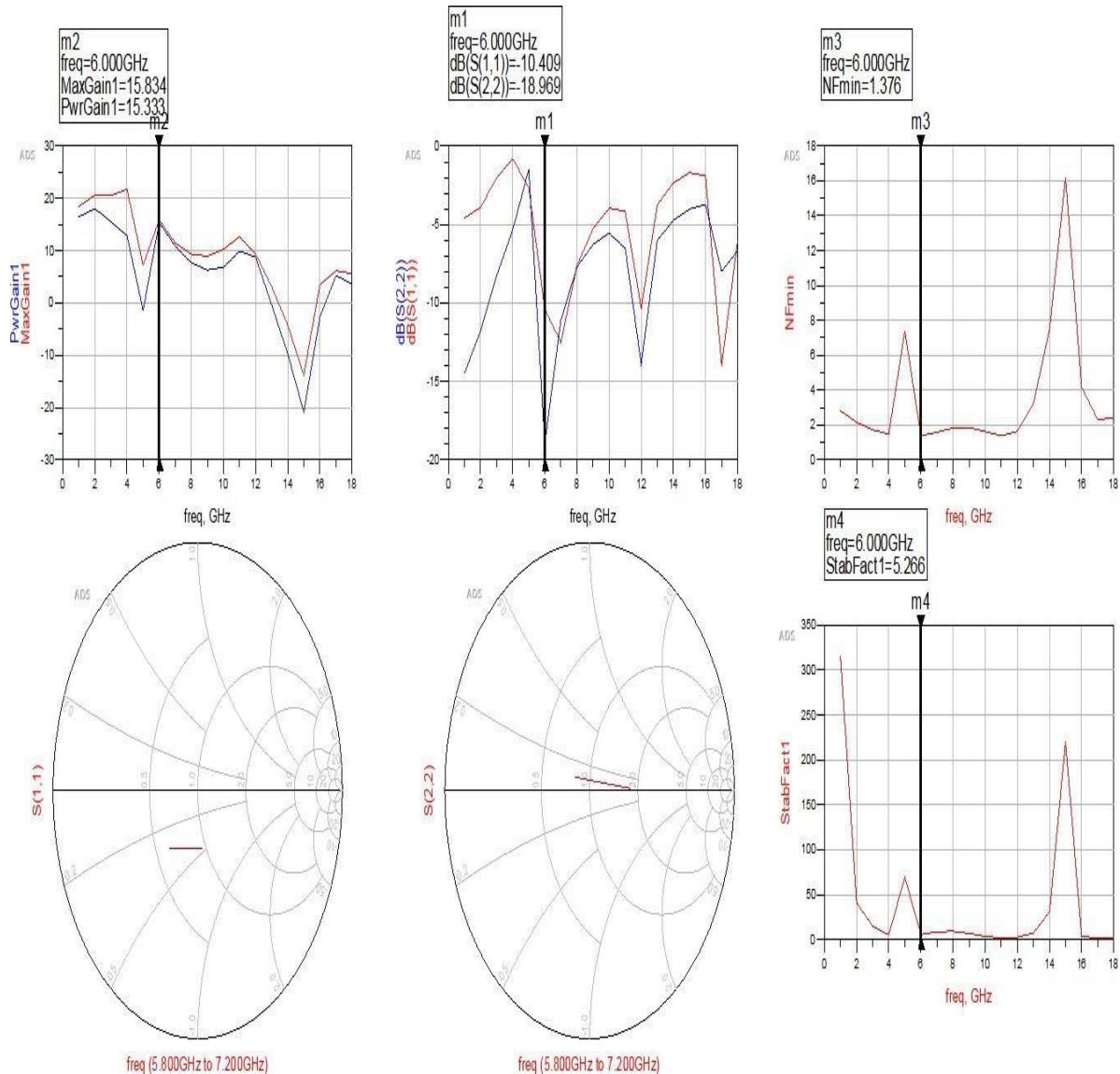


Figure 41 – Output Result of the Cascade MNA

In Figure 41 as we see the Input and Output Reflection coefficients (S_{11} and S_{22} respectively) we see that the input and output impedance circuits provide a good matching.

6.5 DESIGNING OF INTERSTAGE IMPEDANCE MATCHING CIRCUIT OF CASCADE MNA AND FINAL STAGE MGA

Now we are going to cascade the cascade MNA and Final Stage MGA of the LNA and design the interstage impedance matching circuit.

6.5.1 Designing of Interstage Matching Network of Cascade MNA and Final Stage MGA

Now from the Figure 42 we find that the output impedance of the cascade MNA stage and input impedance of the final stage are matched as interstage matching circuits using the smith chart (smart component) available in the ADS software.

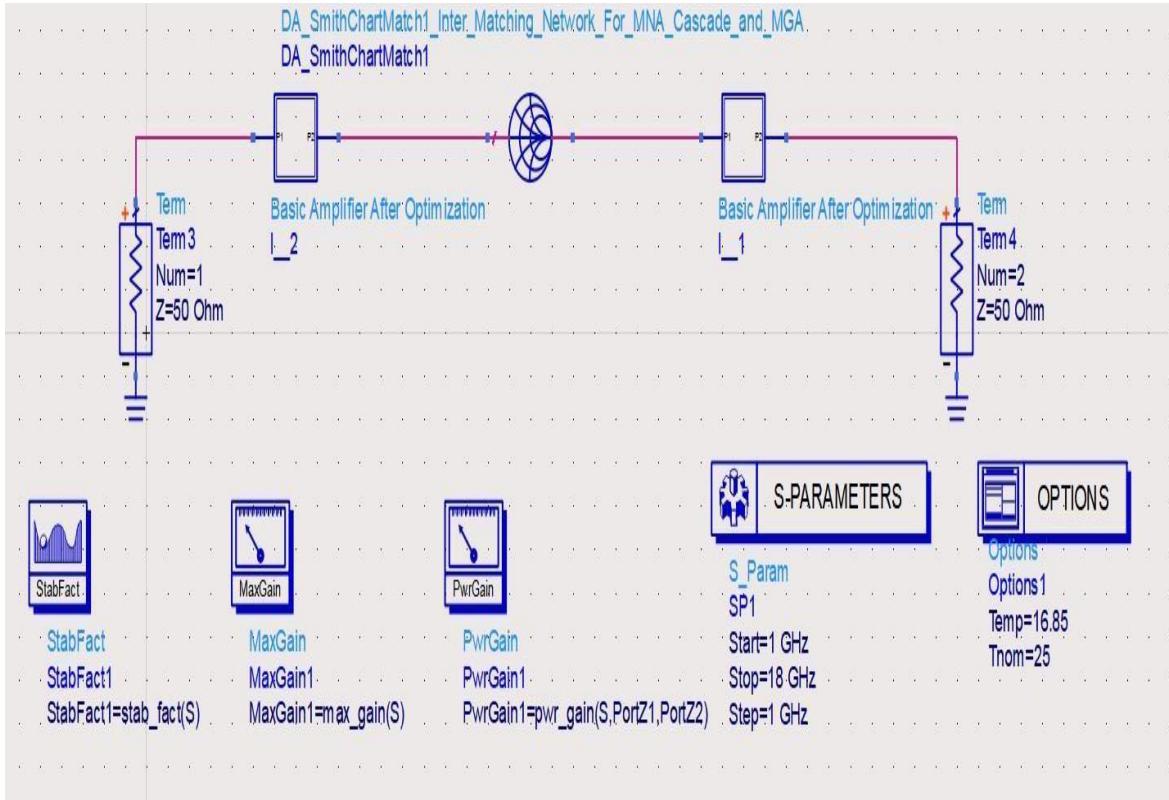


Figure 42 – Designing of Interstage Matching of Cascade MNA and MGA Setup.

6.5.2 Smith Chart Matching for Interstage Impedance Matching of Cascade MNA and Final Stage MGA

The input impedance matching is performed using the ESC available in the ADS software. Figure 43 shows the trace of the impedance matching on the ESC. Figure 44 shows its schematic in the ADS Advanced Design System Software.

Interstage impedance matching is the process of matching the output impedance of one electronic circuit stage with the input impedance of the next stage to maximize power transfer and minimize signal reflections. Mismatches in interstage impedance can lead to signal distortion and loss of power. Techniques such as using coupling capacitors, matching networks, or buffer amplifiers can be used to achieve interstage impedance matching.

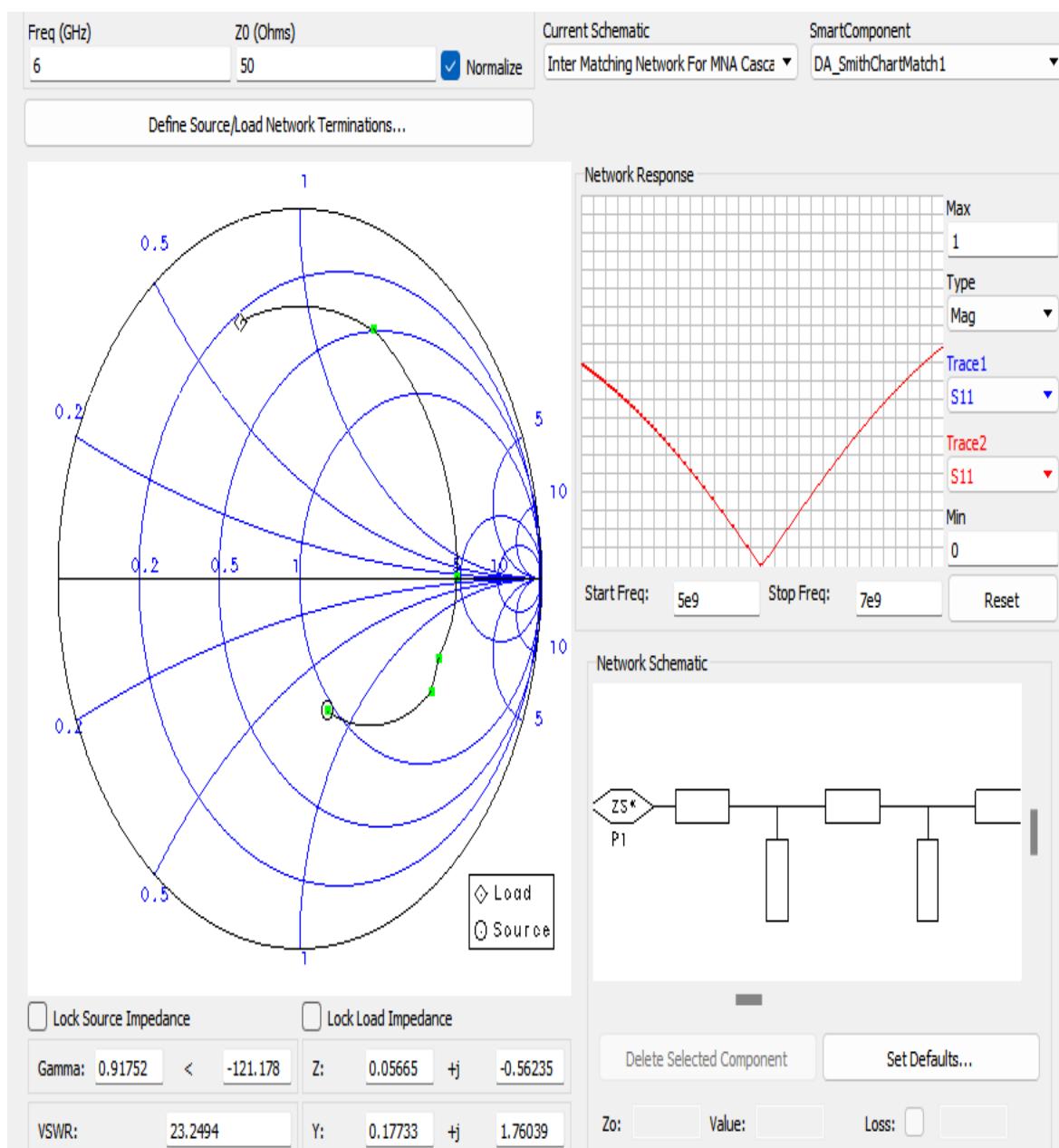


Figure 43 – Interstage Impedance Matching of Cascade MNA and MGA using Smith Chart

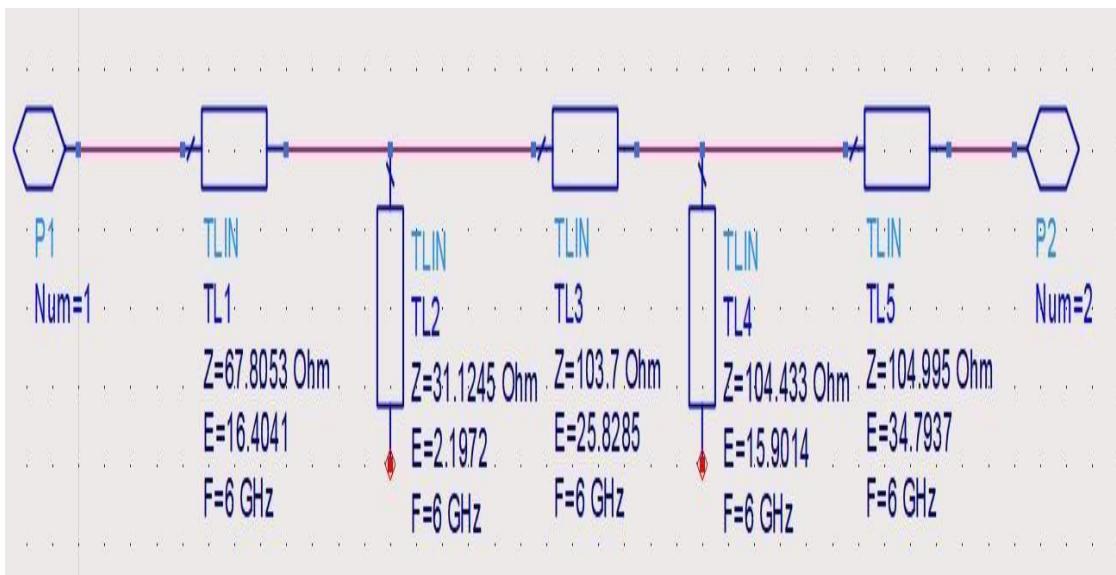


Figure 44 – Interstage Matching Circuit Schematic (Cascade MNA and MGA)

6.5.3 Output result of the Cascade MNA and MGA

In Figure 45 the Maximum Gain, Input and Output Reflection Coefficients, Noise Figure and Stability Factor of the MNA are plotted.

Cascading is a widely used technique in electronic circuits, which involves combining multiple amplification stages to achieve high overall gain and desired performance characteristics. Design considerations include optimizing inter-stage matching, biasing, and feedback networks to ensure maximum gain, bandwidth, and stability while minimizing noise, distortion, and power consumption.

Cascading is commonly used in various electronic applications, including radio frequency (RF) amplifiers, audio amplifiers, and signal processing circuits. It allows for high overall gain, improved signal-to-noise ratio (SNR), and greater flexibility in meeting system specifications, such as frequency response and bandwidth.

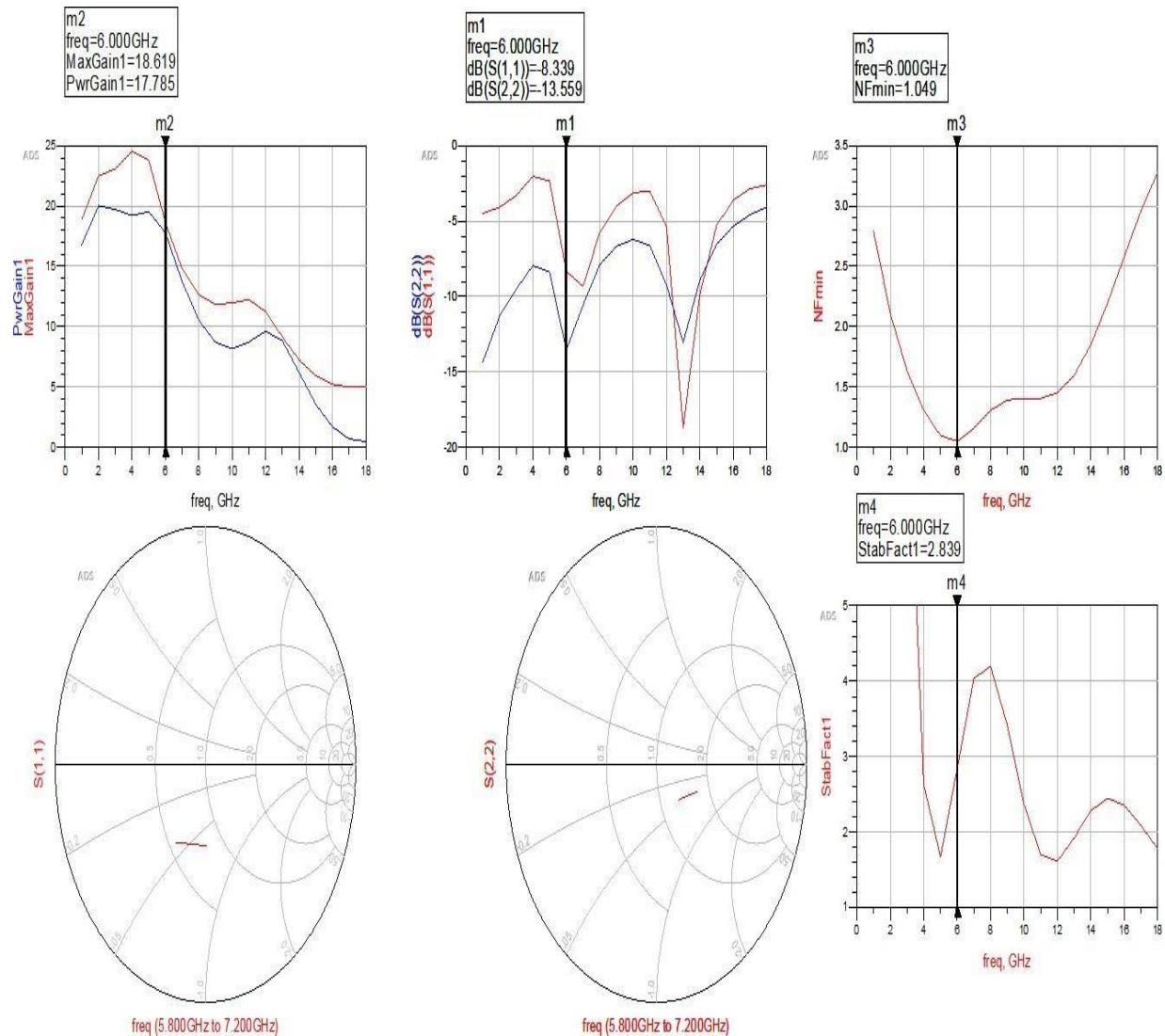


Figure 45 – Output Result of the Cascade MNA and MGA

In Figure 45 as we see the Input and Output Reflection coefficients (S_{11} and S_{22} respectively) we see that the input and output impedance circuits provide a good matching.

Cascading of amplifiers in a radio frequency (RF) system can have both positive and negative effects on the overall system performance. The advantages include increased gain, while the disadvantages include increased noise figure and potential instability. Proper design and analysis of the cascaded stages are required to ensure optimal performance of the overall system.

Chapter 7

DESIGNING OF MICROSTRIP LINES USING THE IDEAL TRANSMISSION LINES

This chapter will cover the process of replacing the theoretical transmission line found in the impedance matching circuits discussed in previous chapters with microstrip lines. The LineCalc tool will be utilized to facilitate this process. The following discussion will present a detailed analysis of the steps involved in this transformation, in accordance with academic writing conventions.

7.1 REPLACING THE IDEAL TRANSMISSION LINES WITH MICROSTRIPS LINES

To replace ideal transmission lines with microstrip lines, a step-by-step procedure must be followed.

- Firstly, a suitable substrate must be selected for the microstrip lines. We have used, Rogers RO4350B substrate can be used in this case.
- Secondly, the MSUB component from the microstrip line library must be placed, and the electrical properties of the selected substrate should be assigned to it.
- Thirdly, the matching circuit containing the ideal transmission line must be copied and pasted onto the new schematic where the MSUB component is present.
- Fourthly, the LineCalc tool, which is available in the toolbar, should be opened, and the electrical properties of the selected substrate must be entered as required.
- Fifthly, the transmission line impedance and electrical length must be entered, and the "synthesize" button should be pressed.
- Finally, the microstrip line from the microstrip library can be placed, and the calculated width and length of the microstrip line

can be entered. This process should be repeated for all ideal transmission lines, replacing them with their corresponding microstrip lines.

By following these steps, the ideal transmission lines in the impedance matching circuits can be efficiently replaced with microstrip lines using the LineCalc tool.

Microstrip transmission lines are widely used in electronic circuits due to their compact size and ease of integration. The design of microstrip lines requires careful consideration of parameters such as impedance, dielectric constant, and substrate thickness. The line and width of microstrip lines can be calculated manually using equations, or with the aid of software tools such as LineCalc, which can optimize the dimensions for a specific set of design requirements. Accurate line and width calculation is critical for achieving the desired electrical performance and avoiding signal degradation.

LineCalc is a software tool used for designing transmission lines, such as microstrip or stripline, by providing calculations for characteristic impedance, electrical length, and attenuation. The LineCalc tool, provided by ADS software, offers a user-friendly interface for designing and optimizing microstrip transmission lines. Figure 46 shows the interface, which allows the user to input the required electrical parameters, such as the substrate material, transmission line impedance, and electrical length, and then generates the corresponding microstrip dimensions. The tool also provides simulation and optimization capabilities to refine the design and ensure optimal performance.

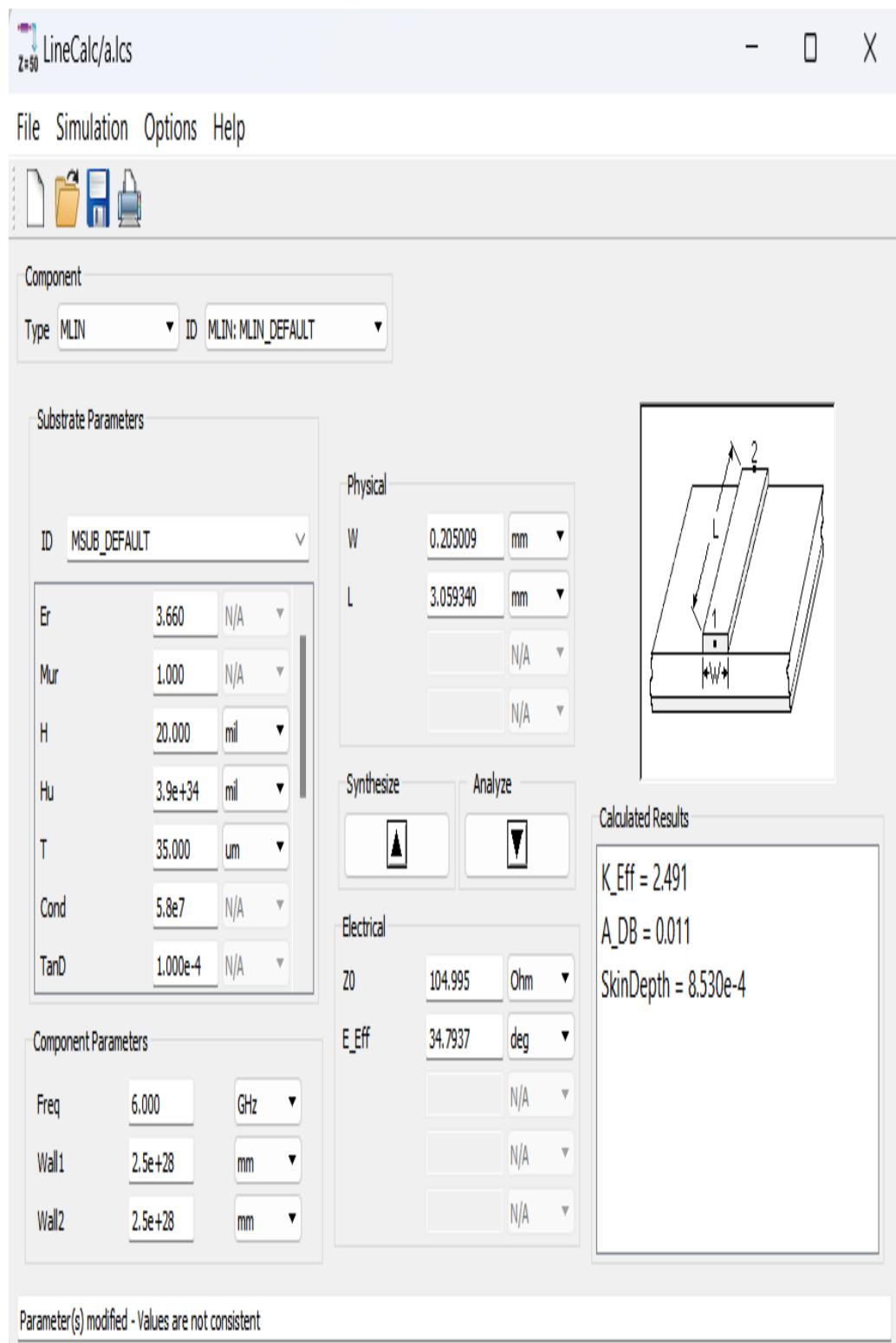


Figure 46 – LineCalc user interface

Chapter 8

Final Design of the LNA

This chapter presents a comprehensive analysis of the final design of a LNA, in which three different stages of amplifiers are cascaded to achieve the desired performance. The first two stages are dedicated to minimum noise amplification, while the third stage is designed for maximum gain amplification. The design also incorporates the use of microstrip lines to replace the ideal transmission lines in the input, output, and interstage matching networks. This chapter provides a comprehensive overview of the design process and its impact on the overall performance of the LNA.

8.1 FINAL LNA SCHEMATIC

The final design of the LNA consists of three amplification stages, with the first two stages specifically designed for minimum noise amplification and the third stage optimized for maximum gain amplification. The matching circuitry of the amplifier is comprised of microstrip lines, which have replaced the ideal transmission lines used in the earlier stages of design. Figure 47 provides a detailed schematic of the LNA, specifically designed to comply with the WLAN IEEE 802.11 ax standard. The use of microstrip lines in the matching circuitry provides the LNA with improved performance in terms of electrical properties, including impedance, electrical length, and dimensions.

LNA is a critical component in RF receiver systems, providing high gain with low noise figure. LNAs are used to amplify the weak signal received from the antenna with minimum added noise. LNAs are typically placed at the front-end of a receiver to provide the initial amplification and sensitivity needed for proper signal reception.

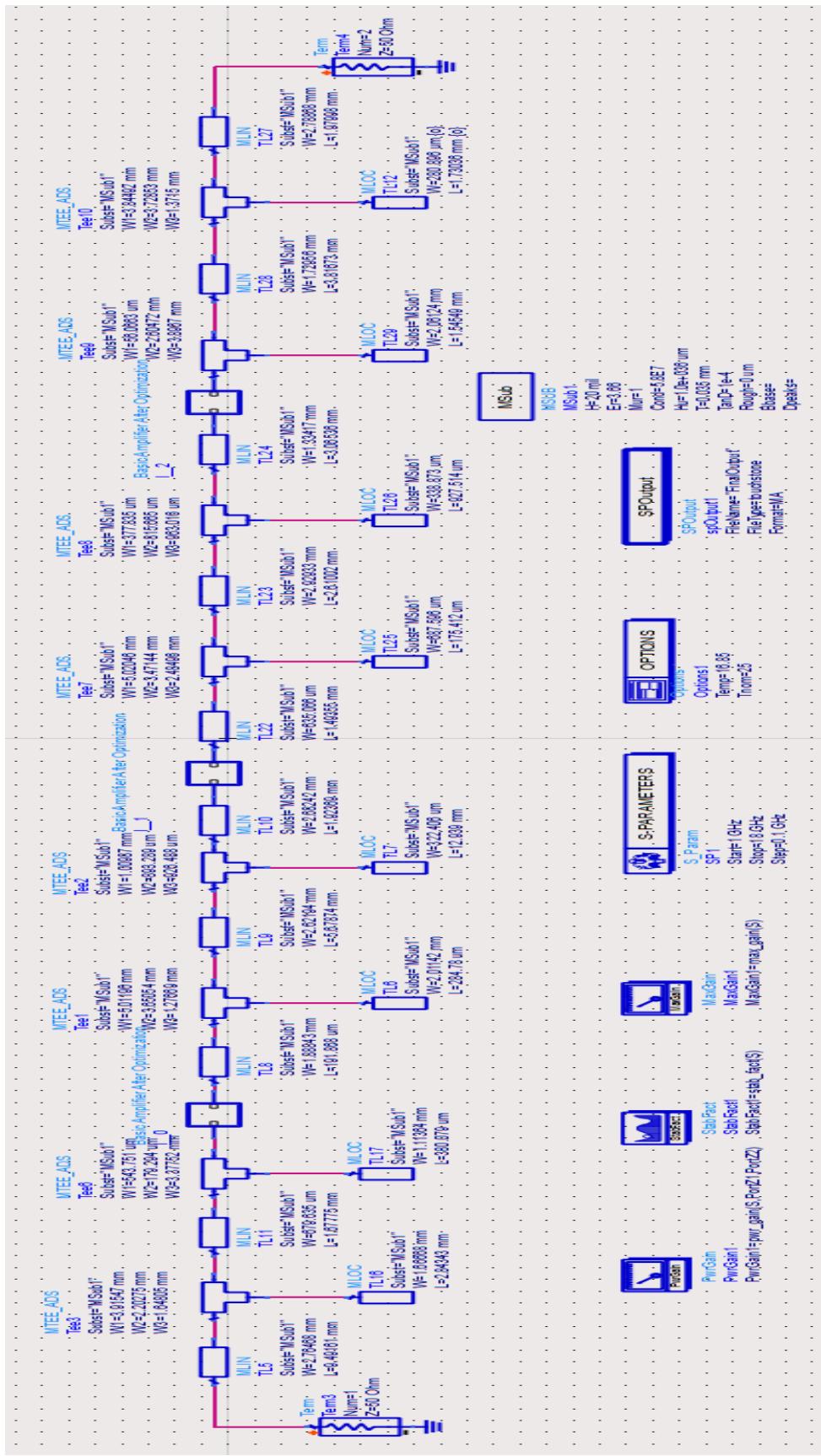


Figure 47 – LNA for WLAN IEEE 802.11 ax

8.2 OUTPUT RESULT OF THE WHOLE LNA for WLAN IEEE 802.11 ax Standard

In Figure 48 the Maximum Gain, Maximum Power Gain, Input and Output Reflection Coefficients, Noise Figure, Noise figure and Stability Factor of the MNA are plotted.

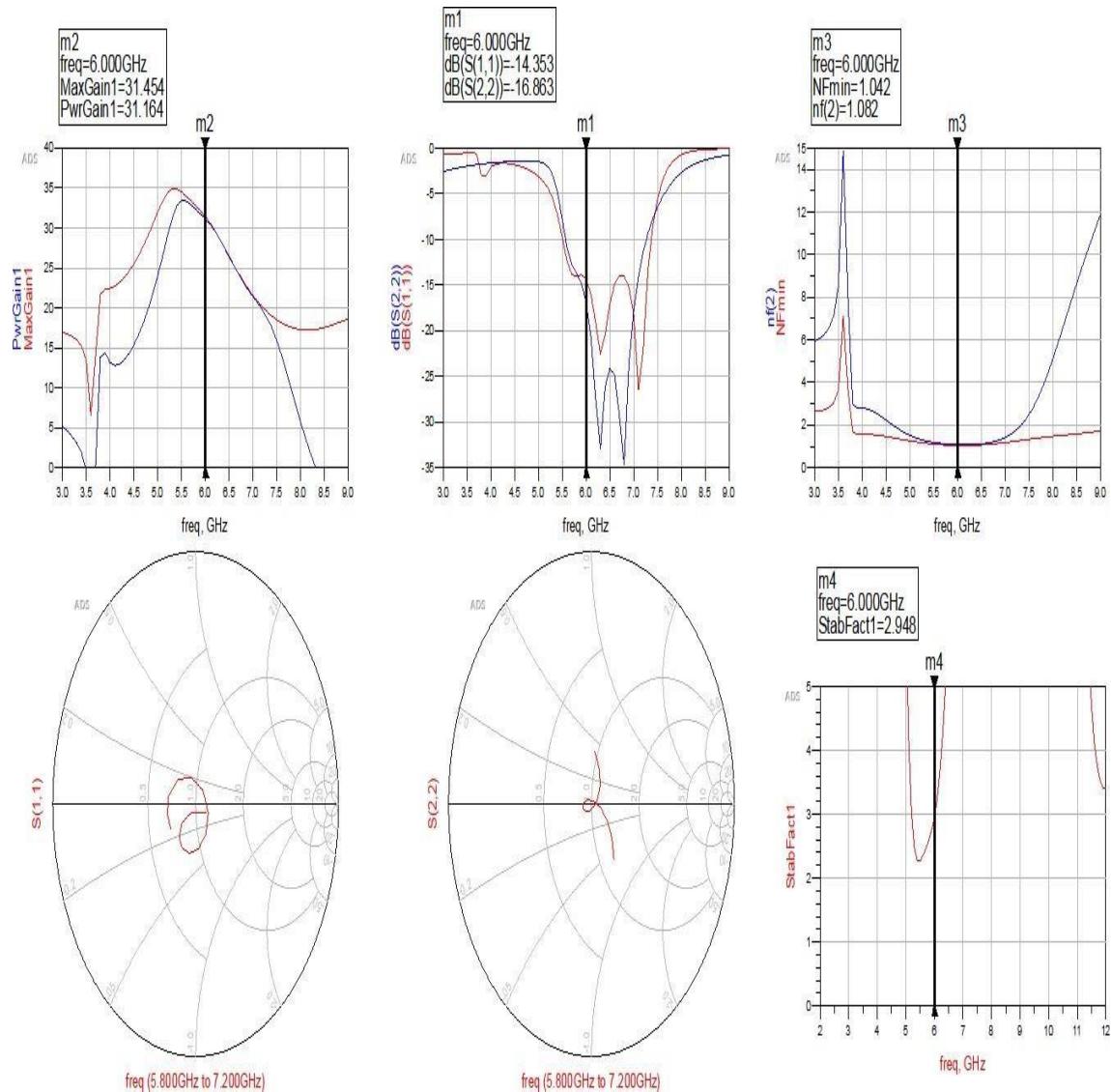


Figure 48 – Output Result of the LNA

According to Figure 48, our designed LNA achieved a Maximum Gain and Maximum Power gain of 31.54 dB and 31.16 dB, respectively, within the 6 GHz

frequency range. As the current gain of the common source topology is less than or equal to unity, the power gain is approximately equal to the voltage gain.

Moreover, the input and output reflection coefficients (S_{11} and S_{22}) were maintained at relatively low levels (below -15 dB) throughout the operating frequency band of 5.9 GHz to 7.2 GHz. At 6 GHz, specifically, the S_{11} and S_{22} values were -14.35 dB and -16.86 dB, respectively. Therefore, our LNA exhibited good impedance matching across the operating bandwidth.

Further, the individual Smith chart plots of input and output reflection coefficients indicated that the S_{11} and S_{22} values were near the unity point 1, indicating good impedance matching. Additionally, the Noise Figure (NF_{min}) remained low within the operating frequency range of 5.9 GHz to 7.2 GHz (around 1.09 dB), and the overall Noise Figure of the LNA was 1.042 dB at 6 GHz. Finally, the LNA exhibited unconditional stability across the frequency range of 2 GHz to 12 GHz.

A LNA is a critical component of the RF receiver that amplifies the weak signals received from the antenna without adding significant noise to the signal. LNAs have high power gain and low noise figure, which are essential for improving the overall performance of the receiver. The LNA is the first stage in the RF receiver, and its performance directly affects the overall sensitivity and selectivity of the receiver. There are several design techniques used to optimize the performance of an LNA, including the use of proper biasing, careful selection of the transistor, and circuit topology. Therefore, designing an efficient and effective LNA is crucial for improving the performance of wireless communication systems.

Chapter 9

CONCLUSION AND FUTURE ENHANCEMENT

9.1 CONCLUSION

In this project, a three-stage LNA has been designed, analysed and optimized. Low-noise amplifiers work in microwave receiver systems, and we develop it logically. Firstly, a transistor, with code ATF-13136 at the operating point ($V_{ds}=2.5$ V, $I_d=24$ mA), is selected as an active device for the key amplification device among products from more than 20 famous manufacturer companies, also the substrate is determined from the manufacturer library embedded inADS Advanced Design System Software as components for LNA. Secondly, the ideal bias circuit, the input matching network, the output network and the inter-stage network are designed in sequence and added to the transistor. Here the ideal design used the ideal transmission lines. Thirdly, the practical three-stage LNA is developed based on the ideal design after the tuning and optimization. We replaced the transmission line to the microstrip lines and expanded the project's frequency from the central frequency to the frequency band in the design goal. The final three-stage LNA fully satisfies the design goal as represented in table 7.1, that is, maximum gain between 25-28 dB, NoiseFigure less than 1.5 dB, and return loss less than -15 dB in the frequency band of 5.9-7.2 dB.

Table 3 – Conclusion Table

Parameters	Design Goals	Result Achieved
Maximum Gain	25 – 28 dB	31.54 dB
Noise Figure	< 1.5 dB	1.042 dB
Input Return Loss	< -15 dB	-14.35 dB
Output return Loss	< -15 dB	-16.86 dB

9.2 FUTURE ENHANCEMENT

In the field of WLAN applications, future enhancements in LNA design may involve the use of advanced techniques to improve linearity, dynamic range, and power efficiency. One potential approach is the use of wideband or multiband LNAs that can operate across multiple frequency bands, enabling greater flexibility in wireless communication systems. Another avenue for improvement is the integration of LNAs with other components, such as filters or mixers, to reduce system complexity and improve overall performance. Additionally, the use of advanced digital signal processing techniques, such as adaptive filtering or interference cancellation, may enable the design of highly robust and reliable WLAN systems. Overall, future advancements in LNA design for WLAN applications are focused on enabling higher data rates, longer ranges, and improved quality of service in wireless networks.

APPENDIX A

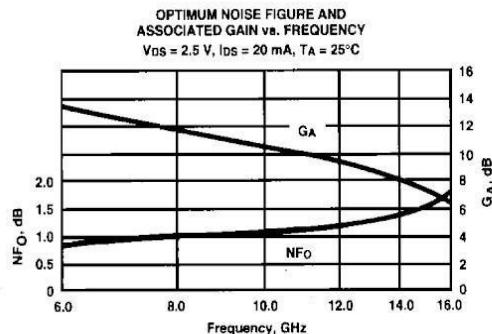
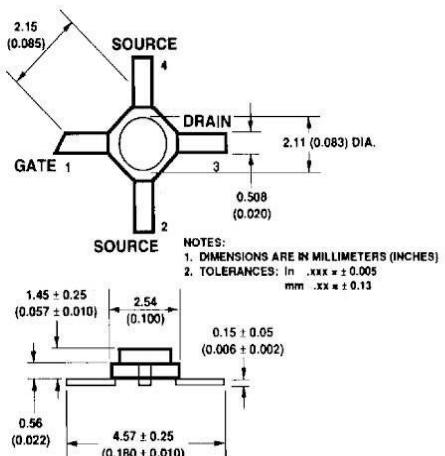
ATF-13136
2-16 GHz Low Noise
Gallium Arsenide FET
Features

- **Low Noise Figure:** 1.2 dB typical at 12 GHz
- **High Associated Gain:** 9.5 dB typical at 12 GHz
- **High Output Power:** 17.5 dBm typical $P_{1\text{ dB}}$ at 12 GHz
- **Cost Effective Ceramic Microstrip Package**
- **Tape-and-Reel Packaging Option Available²**

Description

The ATF-13136 is a high performance gallium arsenide Schottky-barrier-gate field effect transistor housed in a cost effective microstrip package. Its premium noise figure makes this device appropriate for use in the first stage of low noise amplifiers operating in the 2-16 GHz frequency range.

This GaAs FET device has a nominal 0.3 micron gate length with a total gate periphery of 250 microns. Proven gold based metallization systems and nitride passivation assure a rugged, reliable device.

36 micro-X Package¹

Noise Parameters: $V_{DS} = 3$ V, $I_{DS} = 20$ mA

Freq. GHz	NFO dB	Gamma Opt Mag	Ang	$R_{N/50}$
4.0	0.5	.58	87	.22
6.0	0.8	.47	130	.18
8.0	1.0	.37	-163	.17
12.0	1.2	.47	-65	.80
14.0	1.4	.52	-15	1.20

Electrical Specifications, $T_A = 25^\circ\text{C}$

Symbol	Parameters and Test Conditions	Units	Min.	Typ.	Max.
NFO	Optimum Noise Figure: $V_{DS} = 2.5$ V, $I_{DS} = 15 - 30$ mA	dB		1.0	1.4
GA	Gain @ NFO: $V_{DS} = 2.5$ V, $I_{DS} = 15 - 30$ mA	dB		11.5	
P _{1 dB}	Output Power @ 1 dB Gain Compression: $V_{DS} = 4$ V, $I_{DS} = 40$ mA	dBm		17.5	
G _{1 dB}	1dB Compressed Gain: $V_{DS} = 4$ V, $I_{DS} = 40$ mA	dB	8.5	8.5	
gm	Transconductance: $V_{DS} = 2.5$ V, $V_{GS} = 0$ V	mmho	25	55	
Idss	Saturated Drain Current: $V_{DS} = 2.5$ V, $V_{GS} = 0$ V	mA	40	50	90
V _p	Pinchoff Voltage: $V_{DS} = 2.5$ V, $I_{DS} = 1$ mA	V	-4.0	-1.5	-0.5

Notes: 1. Long leadend 35 package available upon request.

2. Refer to PACKAGING section "Tape-and-Reel Packaging for Surface Mount Semiconductors".

ATF-13136, 2-16 GHz
Low Noise Gallium Arsenide FET

Absolute Maximum Ratings

Parameter	Symbol	Absolute Maximum ¹
Drain-Source Voltage	V _{DS}	+5 V
Gate-Source Voltage	V _{GS}	-4 V
Drain Current	I _{DS}	I _{DSS}
Power Dissipation ^{2,3}	P _T	225 mW
Channel Temperature	T _{CH}	175°C
Storage Temperature ⁴	T _{STG}	-65°C to +175°C

Thermal Resistance: $\theta_{JC} = 400^\circ\text{C}/\text{W}$; T_{CH} = 150°C
 Liquid Crystal Measurement; 1 μm Spot Size⁵

Notes:

1. Operation of this device above any one of these parameters may cause permanent damage.
2. Case Temperature = 25°C.
3. Derate at 2.5 mW/°C for T_{CASE} > 85°C.
4. Storage above +150°C may tarnish the leads of this package making it difficult to solder into a circuit. After a device has been soldered into a circuit, it may be safely stored up to 175°C.
5. The small spot size of this technique results in a higher, though more accurate determination of θ_{JC} than do alternate methods. See MEASUREMENTS section for more information.

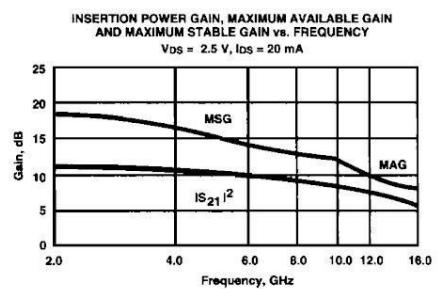
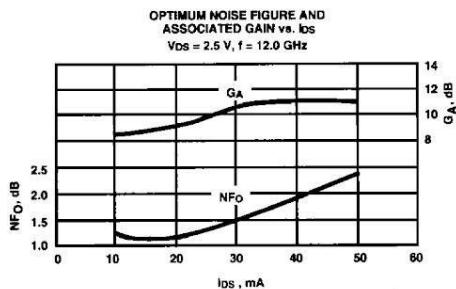
Part Number Ordering Information

Part Number	Devices Per Reel	Reel Size
ATF-13136-TR1	1000	7"
ATF-13136-TR2	4000	13"
ATF-13136-STR	1	STRIP

For more information, see "Tape and Reel Packaging for Semiconductor Devices", page 14-14.

Typical Performance, T_A = 25°C

(unless otherwise noted)



Typical Scattering Parameters: Common Source, Z₀ = 50 Ω

T_A = 25°C, V_{DS} = 2.5 V, I_{DS} = 20 mA

Freq. GHz	S ₁₁		S ₂₁		S ₁₂		S ₂₂	
	Mag	Ang	dB	Mag	Ang	dB	Mag	Ang
2.0	.95	-42	11.2	3.65	134	-26.7	.046	62
3.0	.87	-65	10.7	3.43	112	-24.2	.062	40
4.0	.84	-85	10.3	3.28	93	-22.3	.077	31
5.0	.78	-104	10.1	3.21	73	-20.3	.097	18
6.0	.69	-128	10.4	3.30	52	-18.6	.117	7
7.0	.59	-163	10.4	3.32	27	-17.3	.137	-12
8.0	.54	157	9.8	3.10	2	-17.0	.142	-27
9.0	.55	121	9.2	2.89	-19	-16.3	.153	-43
10.0	.54	93	8.7	2.71	-41	-16.0	.159	-58
11.0	.56	64	8.1	2.54	-61	-16.2	.155	-73
12.0	.61	37	7.4	2.34	-84	-16.8	.144	-89
13.0	.65	19	6.8	2.18	-102	-17.6	.132	-100
14.0	.65	7	6.4	2.09	-120	-18.0	.126	-114
15.0	.67	-6	5.9	1.98	-139	-18.2	.123	-119
16.0	.68	-25	5.3	1.84	-170	-18.4	.120	-134

A model for this device is available in the DEVICE MODELS section.

APPENDIX B



RO4000® Series

High Frequency Circuit Materials

RO4000® hydrocarbon ceramic laminates are designed to offer superior high frequency performance and low cost circuit fabrication. The result is a low loss material which can be fabricated using standard epoxy/glass (FR-4) processes offered at competitive prices.

The selection of laminates typically available to designers is significantly reduced once operational frequencies increase to 500 MHz and above. RO4000 material possesses the properties needed by designers of RF microwave circuits and matching networks and controlled impedance transmission lines. Low dielectric loss allows RO4000 series material to be used in many applications where higher operating frequencies limit the use of conventional circuit board laminates. The temperature coefficient of dielectric constant is among the lowest of any circuit board material (Chart 1), and the dielectric constant is stable over a broad frequency range (Chart 2). For reduced insertion loss, LoPro® foil is available (Chart 3). This makes it an ideal substrate for broadband applications.

RO4000 material's thermal coefficient of expansion (CTE) provides several key benefits to the circuit designer. The expansion coefficient of RO4000 material is similar to that of copper which allows the material to exhibit excellent dimensional stability, a property needed for mixed dielectric multi-layer boards constructions. The low Z-axis CTE of RO4000 laminates provides reliable plated through-hole quality, even in severe thermal shock applications. RO4000 series material has a Tg of >280°C (536°F) so its expansion characteristics remain stable over the entire range of circuit processing temperatures.

RO4000 series laminates can easily be fabricated into printed circuit boards using standard FR-4 circuit board processing techniques. Unlike PTFE based high performance materials, RO4000 series laminates do not require specialized via preparation processes such as sodium etch. This material is a rigid, thermoset laminate that is capable of being processed by automated handling systems and scrubbing equipment used for copper surface preparation.

RO4003C™ laminates are currently offered in various configurations utilizing both 1080 and 1674 glass fabric styles, with all configurations meeting the same laminate electrical performance specification. Specifically designed as a drop-in replacement for the RO4003C™ material, RO4350B™ laminates utilize RoHS compliant flame-retardant technology for applications requiring UL 94V-0 certification. These materials conform to the requirements of IPC-4103, slash sheet /10 for RO4003C, see note #1 for RO4350B slash sheet determination.



Data Sheet



FEATURES AND BENEFITS:

- RO4000 materials are reinforced hydrocarbon/ceramic laminates - not PTFE
 - Designed for performance sensitive, high volume applications
- Low dielectric tolerance and low loss
 - Excellent electrical performance
 - Allows applications with higher operating frequencies
 - Ideal for broadband applications
- Stable electrical properties vs. frequency
 - Controlled impedance transmission lines
 - Repeatable design of filters
- Low thermal coefficient of dielectric constant
 - Excellent dimensional stability
- Low Z-axis expansion
 - Reliable plated through holes
- Low in-plane expansion coefficient
 - Remains stable over an entire range of circuit processing temperatures
- Volume manufacturing process
 - RO4000 laminates can be fabricated using standard glass epoxy processes
 - Competitively priced
 - CAF resistant

SOME TYPICAL APPLICATIONS:

- Cellular Base Station Antennas and Power Amplifiers
- RF Identification Tags
- Automotive Radar and Sensors
- LNB's for Direct Broadcast Satellites



Chart 1: RO4000 Series Materials Dielectric Constant vs. Temperature

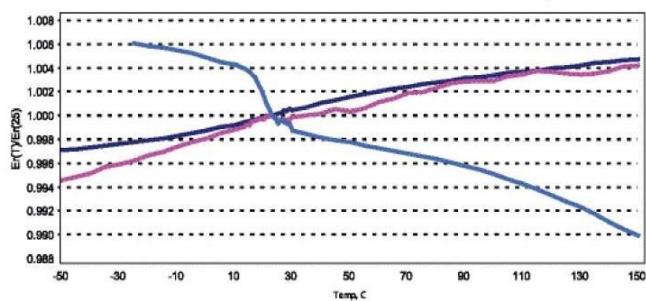


Chart 2: RO4000 Series Materials Dielectric Constant vs. Frequency

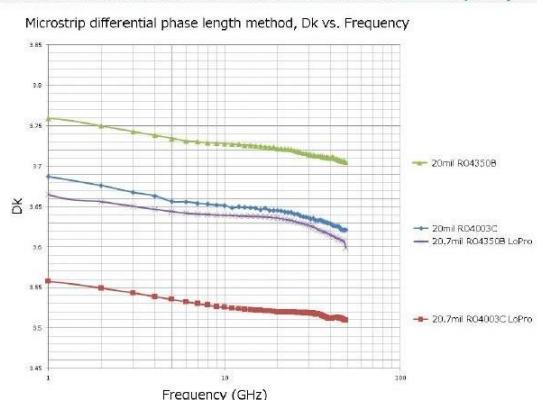
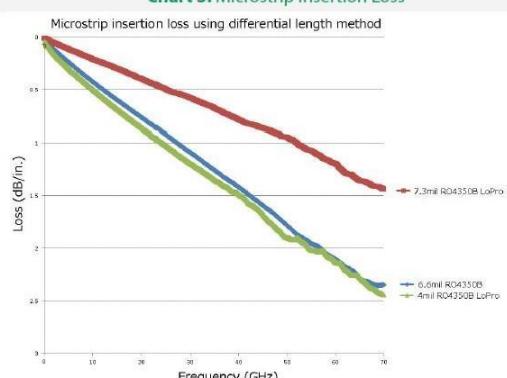


Chart 3: Microstrip Insertion Loss



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Property	Typical Value		Direction	Units	Condition	Test Method
	RO4003C	RO4350B				
Dielectric Constant, ϵ_r Process	3.38 ± 0.05	(⁽¹⁾ 3.48 ± 0.05	Z	-	10 GHz/23°C	IPC-TM-650 2.5.5.5 Clamped Stripline
(⁽²⁾ Dielectric Constant, ϵ_r Design	3.55	3.66	Z	-	8 to 40 GHz	Differential Phase Length Method
Dissipation Factor tan, d	0.0027 0.0021	0.0037 0.0031	Z	-	10 GHz/23°C 2.5 GHz/23°C	IPC-TM-650 2.5.5.5
Thermal Coefficient of ϵ_r	+40	+50	Z	ppm/°C	-50°C to 150°C	IPC-TM-650 2.5.5.5
Volume Resistivity	1.7×10^{10}	1.2×10^{10}	-	MΩ·cm	COND A	IPC-TM-650 2.5.17.1
Surface Resistivity	4.2×10^9	5.7×10^9	-	MΩ	COND A	IPC-TM-650 2.5.17.1
Electrical Strength	31.2 (780)	31.2 (780)	Z	kV/mm (V/mil)	0.51mm (0.020")	IPC-TM-650 2.5.6.2
Tensile Modulus	19,650 (2,850) 19,450 (2,821)	16,767 (2,432) 14,153, (2,053)	X Y	MPa (ksi)	RT	ASTM D638
Tensile Strength	139 (20.2) 100 (14.5)	203 (29.5) 130 (18.9)	X Y	MPa (ksi)	RT	ASTM D638
Flexural Strength	276 (40)	255 (37)	-	MPa (kpsi)	-	IPC-TM-650 2.4.4
Dimensional Stability	<0.3	<0.5	X,Y	mm/m (mils/inch)	after etch +E2/150°C	IPC-TM-650 2.4.39A
Coefficient of Thermal Expansion	11 14 46	10 12 32	X Y Z	ppm/°C	-55 to 288°C	IPC-TM-650 2.4.41
Tg	>280	>280	-	°C TMA	A	IPC-TM-650 2.4.24.3
Td	425	390	-	°CTGA		ASTM D3850
Thermal Conductivity	0.71	0.69	-	W/m/K	80°C	ASTM C518
Moisture Absorption	0.06	0.06	-	%	48 hrs immersion 0.060" sample Temperature 50°C	ASTM D570
Density	1.79	1.86	-	g/cm³	23°C	ASTM D792
Copper Peel Strength	1.05 (6.0)	0.88 (5.0)	-	N/mm (pli)	after solder float 1 oz. EDC Foil	IPC-TM-650 2.4.8
Flammability	N/A	(⁽³⁾ V-0	-	-	-	UL 94
Lead-Free Process Compatible	Yes	Yes	-	-	-	-

NOTES:

- (1) RO4350B 4 mil laminates have a process Dk of 3.33 ± 0.05 and are in conformance with IPC-4103A/240. All other RO4350B laminate thicknesses are /11 and /240 compliant.
 (2) The design Dk is an average number from several different tested lots of material and on the most common thickness's. If more detailed information is required, please contact Rogers Corporation or refer to Rogers' technical papers in the Rogers Technology Support Hub available at <http://www.rogerscorp.com>.
 (3) RO4350B LoPro® laminates do not share the same UL designation as standard RO4350B laminates. A separate UL qualification may be necessary.

Typical values are a representation of an average value for the population of the property. For specification values contact Rogers Corporation.

RO4000 LoPro laminate uses a modified version of the RO4000 resin system to bond reverse treated foil. Values shown above are RO4000 laminates without the addition of the LoPro resin. LoPro foil results in an overall thickness increase of approximately 0.0007" (18µm) per core.

The LoPro Resin Dk is approximately 2.4. However, when used in combination with the base laminate system, the average design Dk noted in the data sheet table should be used. (The design Dk value decreases by about 0.1 as the core thickness decreases from 0.020" to 0.004".)

Prolonged exposure in an oxidative environment may cause changes to the dielectric properties of hydrocarbon based materials. The rate of change increases at higher temperatures and is highly dependent on the circuit design. Although Rogers' high frequency materials have been used successfully in innumerable applications and reports of oxidation resulting in performance problems are extremely rare, Rogers recommends that the customer evaluate each material and design combination to determine fitness for use over the entire life of the end product.

Standard Thicknesses	Standard Panel Sizes	Standard Claddings
RO4003C: 0.008" (0.203mm) +/- 0.0010" 0.012" (0.305mm) +/- 0.0010" 0.016" (0.406mm) +/- 0.0015" 0.020" (0.508mm) +/- 0.0015" 0.032" (0.813mm) +/- 0.0020" 0.060" (1.524mm) +/- 0.0040"	24" X 18" (610 X 457 mm) 24" X 21" (610 X 533 mm) 24" X 36" (610 X 915 mm) 48" X 36" (1219 X 915 mm) *Additional panel sizes available	<u>Electrodeposited Copper Foil</u> 1/2 oz. (18µm) HH/HH 1 oz. (35µm) H1/H1 *Additional cladding weights are available
RO4350B: 0.004" (0.10mm) +/- 0.0007" 0.0066" (0.17mm) +/- 0.0007" 0.010" (0.25mm) +/- 0.0010" 0.020" (0.51mm) +/- 0.0015" 0.030" (0.76mm) +/- 0.0020" 0.060" (1.52mm) +/- 0.0040"		

*Additional non-standard thicknesses available from 0.0066" - 0.060" in varying increments

*Contact Customer Service or Sales Engineering to inquire about additional available product configurations

The information in this data sheet is intended to assist you in designing with Rogers' circuit materials. It is not intended to and does not create any warranties express or implied, including any warranty of merchantability or fitness for a particular purpose or that the results shown on this data sheet will be achieved by a user for a particular purpose. The user should determine the suitability of Rogers' circuit materials for each application.

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Department of Electronics and Communication Engineering

Vision and Mission of the Institute

Vision:

To impart state-of-the art technical education, including sterling values and shining character, producing engineers who contribute to nation building thereby achieving our ultimate objective of sustained development of an unparalleled society, nation and world at large.

Mission:

Meenakshi Sundararajan Engineering College, Chennai constantly strives to be a Centre of Excellence with the singular aim of producing students of outstanding academic excellence and sterling character to benefit the society, our nation and the world at large.

To achieve this, the college ensures

- Continuous up gradation of its teaching faculty to ensure a high standard of quality education and to meet the ever-changing needs of the society.
- Constant interaction with its stakeholders.
- Linkage with other educational institutions and industries at the national and international level for mutual benefit.
- Provision of research facilities and infrastructure in line with global trends.
- Adequate opportunities and exposure to the students through suitable programs, to mould their character and to develop their personality with an emphasis on professional ethics and moral values.



Department of Electronics and Communication Engineering

Vision and Mission of the Department

Vision:

To emerge as a centre of excellence in offering quality education to produce students technically competent, socially responsible and industry ready graduates in electronics and communication engineering.

Mission:

The above vision will be achieved by

M1: Ensuring effective teaching learning methodologies.

M2: Inculcating creative thinking through innovative and group work exercises. **M3:** Developing and motivating research ability among students by establishing research linkage with leading industries.

M4: Equipping faculty and students with the latest developments in Electronics and Communication and to face the challenges.

Program Educational Objectives (PEOs)

PEO1: To provide appropriate knowledge in applying the concepts of basic electronics & Communication engineering.

PEO2: To be able to identify, analyze and solve engineering problems in the field of electronics & communication engineering.

PEO3: To provide an opportunity to work in multidisciplinary groups and research environments.

PEO4: To educate and inculcate professional ethics, human values, self-confidence and awareness of societal needs.

PEO5: To motivate the students in intellectual pursuits, lifelong learning in order to develop different perspectives of technological developments.



Program Outcomes (POs)

PO1: Engineering Knowledge Apply the knowledge of Engineering Mathematics, Basic Sciences, Engineering Fundamentals, and Engineering Specialization to the solution of complex Information Science and Engineering problems.

PO2: Problem analysis Identify, formulate, review research literature, and analyze complex engineering problems of Information Science and Engineering reaching substantiated conclusions using first principles of Engineering Mathematics and Engineering Sciences.

PO3: Design/development of solutions Design solutions for complex Information Science problems and design system components or processes of Information Science and Engineering that meet the specified needs with appropriate consideration for the public health and safety, and the cultural, societal, and environmental considerations.

PO4: Conduct investigations of complex problems Use research-based knowledge and research methods including design of experiments, analysis and interpretation of data, and synthesis of the information to provide valid conclusions in Information Science and Engineering.

PO5: Modern tool usage Create, select, and apply appropriate techniques, resources, and modern engineering and IT tools including prediction and modeling to complex engineering activities with an understanding of the limitations in Information Science and Engineering.

PO6: The engineer and society Apply reasoning informed by the contextual knowledge to assess societal, health, safety, legal and cultural issues and the consequent responsibilities relevant to the professional engineering practice in Information Science and Engineering.



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PO7: Environment and sustainability understand the impact of the professional engineering solutions in Information Science and Engineering in societal and environmental contexts, and demonstrate the knowledge of, and need for sustainable development.

PO8: Ethics Apply ethical principles and commit to professional ethics and responsibilities and norms of the Information Science and Engineering practice.

PO9: Individual and team work Function effectively as an individual, and as a member or leader in diverse teams, and in multidisciplinary settings.

PO10: Communication Communicate effectively on complex Information Science engineering activities with the engineering community and with society at large, such as, being able to comprehend and write effective reports and design documentation, make effective presentations, and give and receive clear instructions.

PO11: Project management and finance Demonstrate knowledge and understanding of the engineering and management principles and apply these to one's own work, as a member and leader in a team, to manage projects and in multidisciplinary environments. **PO12: Life-long learning** Recognize the need for and have the preparation and ability to engage in independent and life-long learning in the broadest context of technological change.

Program Specific Outcomes (PSOs)

PSO1: Demonstrate principles of basic electronic circuits, digital electronics, microprocessor and signal processing.

PSO2: Design systems for applications in the areas of communication, networking and embedded systems.

PSO3: Design low cost quality, energy efficient and eco-friendly products.



Course Outcomes

EC 8811/ C413 PROJECT WORK

TITLE OF PROJECT: LOW NOISE AMPLIFIER DESIGN FOR WLAN

IEEE 802.11ax STANDARDS

At the end of the course, the students will be able to:

C413.1	Understand the concept of LNA MMIC design using ADS software.
C413.2	Apply the concept of the stability design, noise optimization using inductive source degeneration, minimum noise amplifier design and maximum noise amplifier design.
C413.3	Create the impedance matching circuit for the different stages of the LNA.
C413.4	Analyze the results obtained from the simulation using the electronic smith charts and rectangular plots.
C413.5	Evaluate the quantitative and qualitative effectiveness of the output obtained.



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CO-PO Mapping

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
C413.1	3	3	3	2	3	2	2	3	3	3	3	2
C413.2	3	3	2	3	3	2	2	2	3	2	3	2
C413.3	3	2	3	3	2	2	2	2	2	3	2	3
C413.4	3	2	2	2	3	3	2	2	2	2	3	1
C413.5	2	2	2	2	2	2	2	3	3	3	2	2
C413	2.8	2.4	2.4	2.4	2.6	2.2	2.0	2.4	2.6	2.6	2.6	2.0

CO-PSO Mapping

CO	PSO1	PSO2	PSO3
C413.1	3	2	1
C413.2	3	2	1
C413.3	2	2	2
C413.4	2	2	2
C413.5	1	2	1
C413	2.2	2	1.4



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CO-PO Calculation