Alexandria University

Faculty of Engineering

Electronics and Communications Engineering Program

2023-2024

Full Custom Design of

4-Bit Ripple Carry Adder

VLSI - EEC 433

Spring 2024

By Student:

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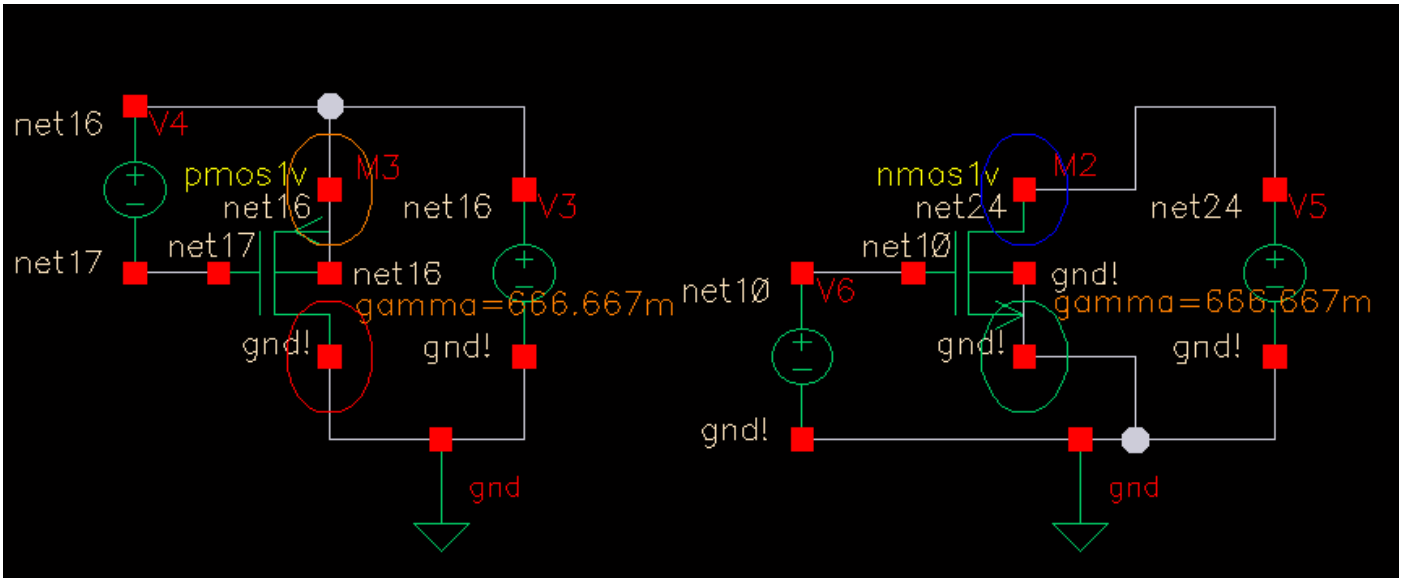
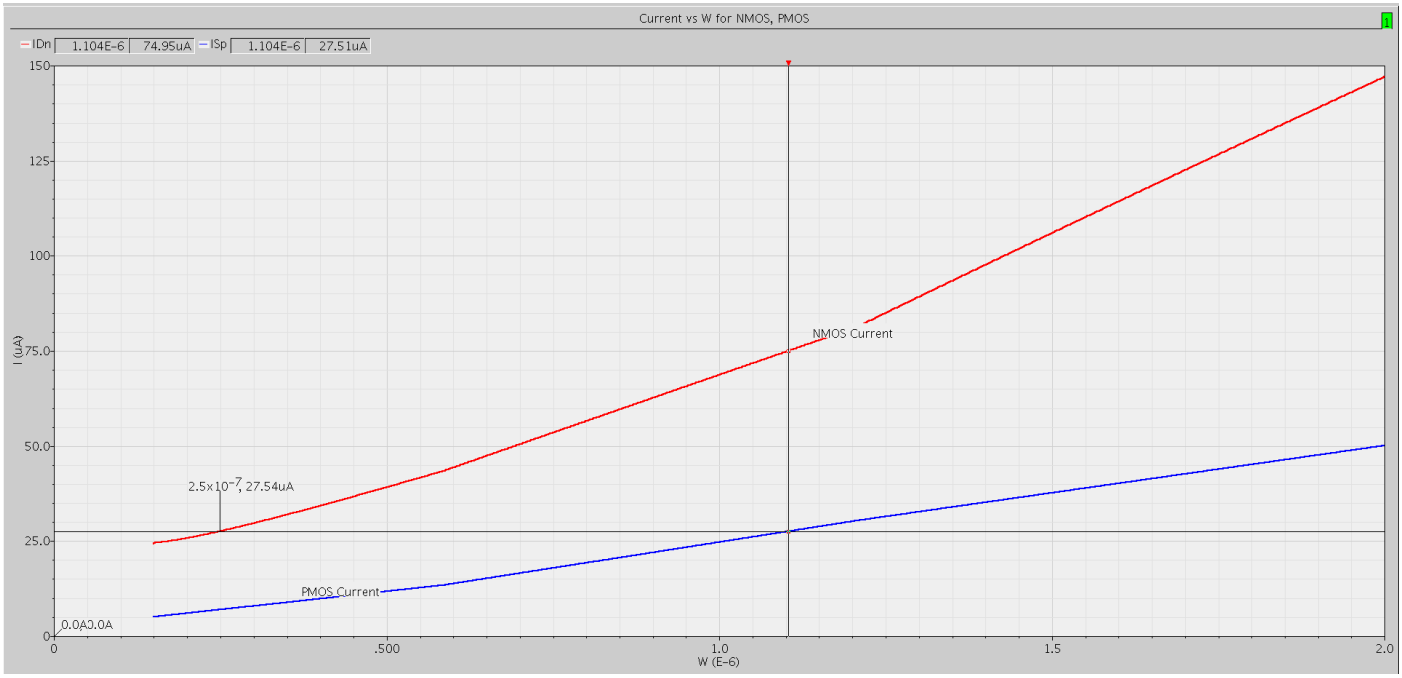
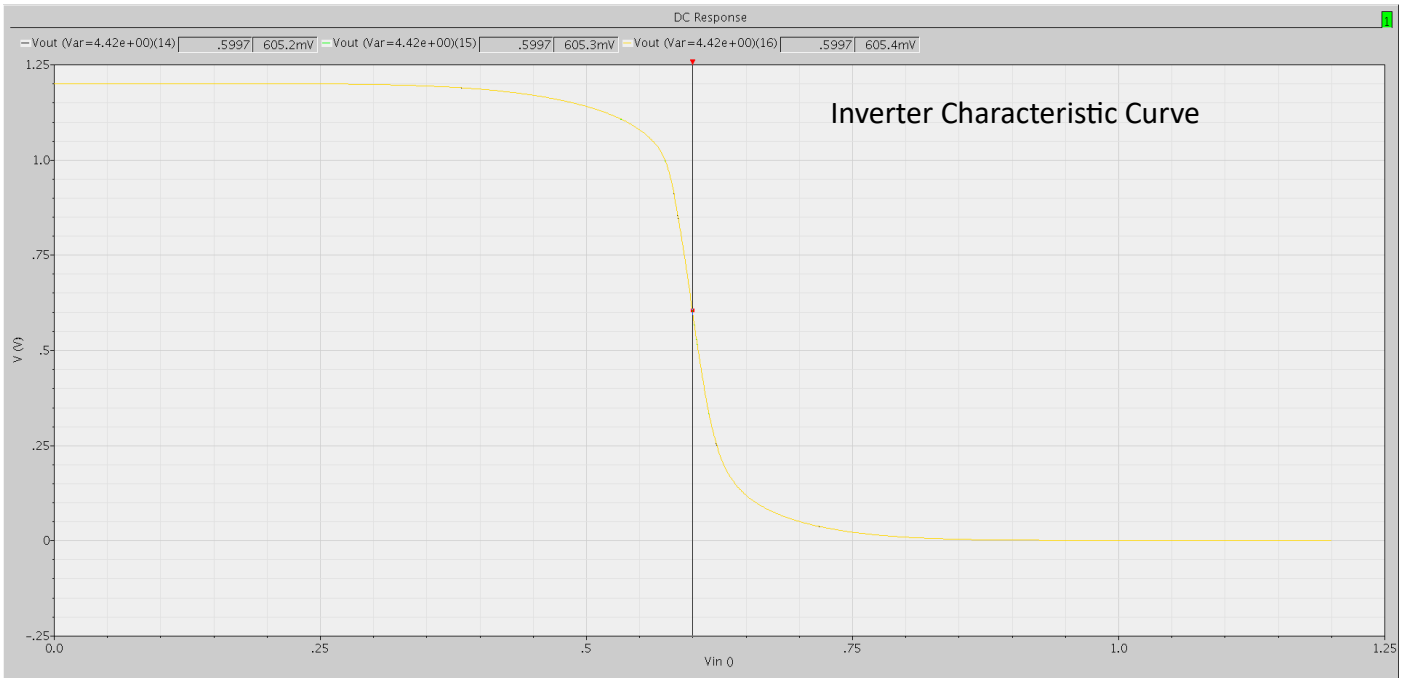
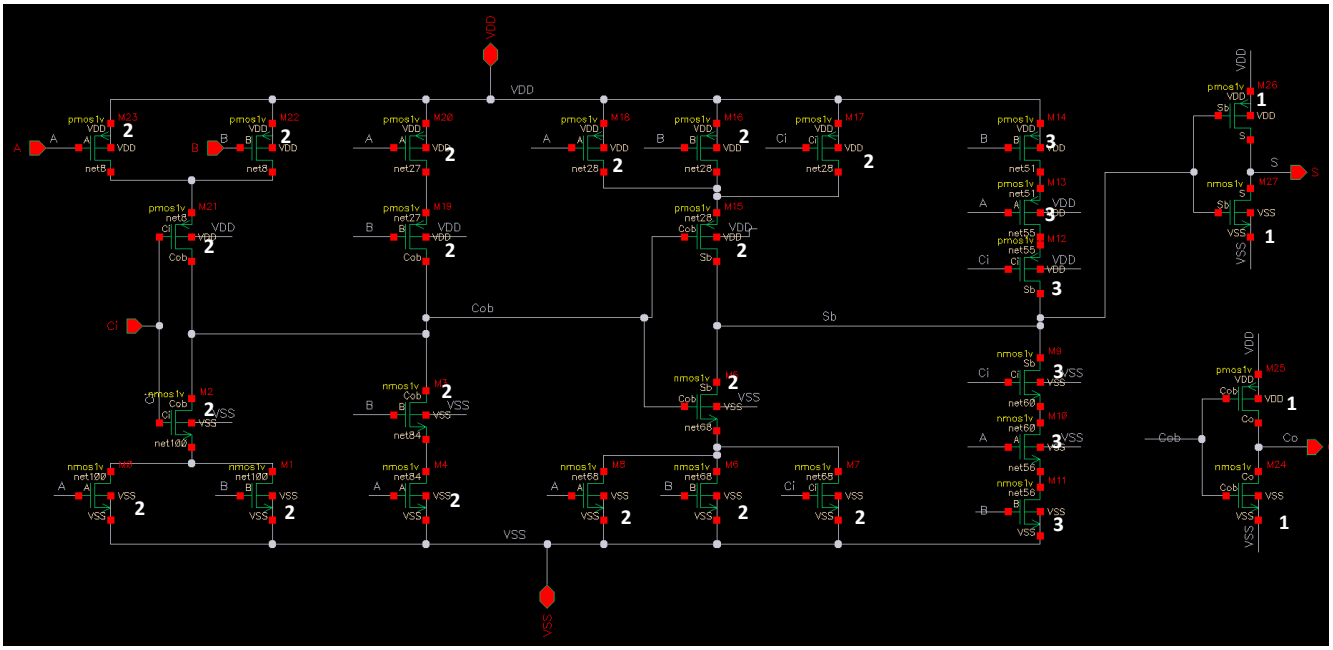
Electronics and Communications Engineering

Alexandria University

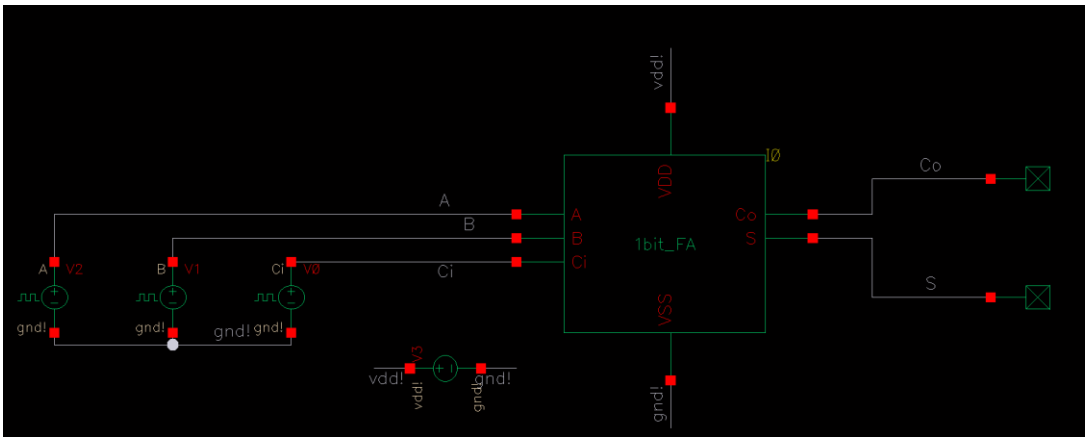

net16
V4
pmos1v
M3
net16
net16
V3
net17
net17
net16
gamma=666.667m
gnd!
gnd!
gnd
net10
V6
nmos1v
M2
net24
net24
V5
net10
gnd!
gamma=666.667m
gnd!
gnd!
gnd


Current vs W for NMOS, PMOS
IDn 1.104E-6 74.95uA
ISp 1.104E-6 27.51uA
150
125
100
75.0
50.0
25.0
0
I (uA)
NMOS Current
2.5x10^-7, 27.54uA
PMOS Current
0.0A0.0A
0
.500
1.0
1.5
2.0
W (E-6)

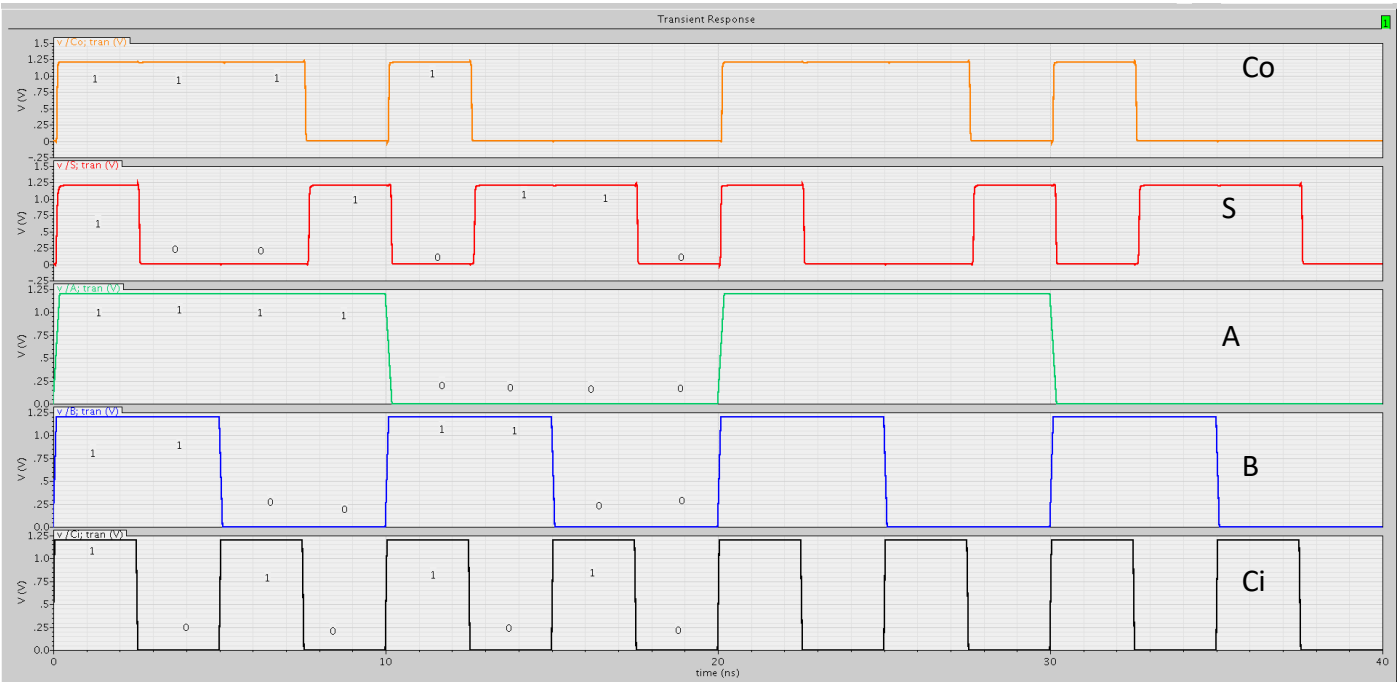

DC Response
Vout (Var=4.42e+00)(14) .5997 605.2mV
Vout (Var=4.42e+00)(15) .5997 605.3mV
Vout (Var=4.42e+00)(16) .5997 605.4mV
Inverter Characteristic Curve
1.25
1.0
.75
.5
.25
0
-.25
V (V)
0.0
.25
.5
.75
1.0
1.25
Vin 0



Full Adder Circuit Schematic



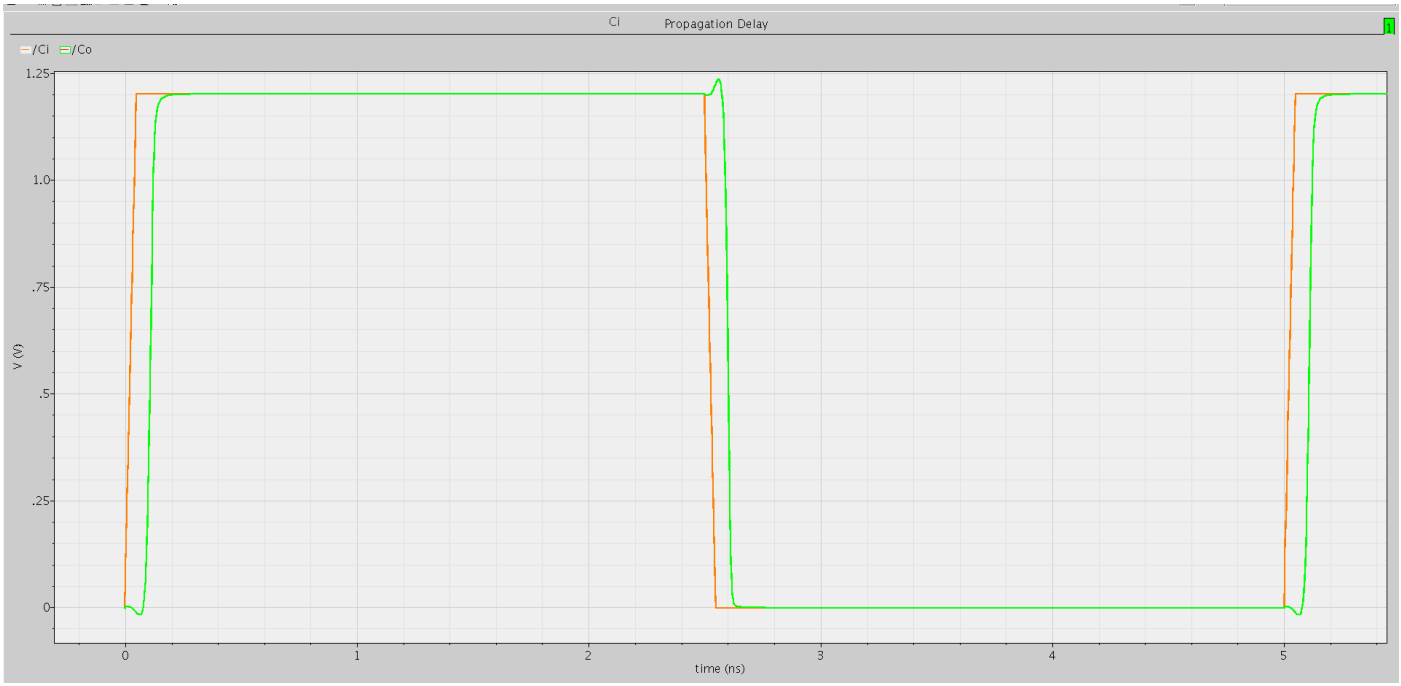
1 bit Full Adder symbol and Test bench

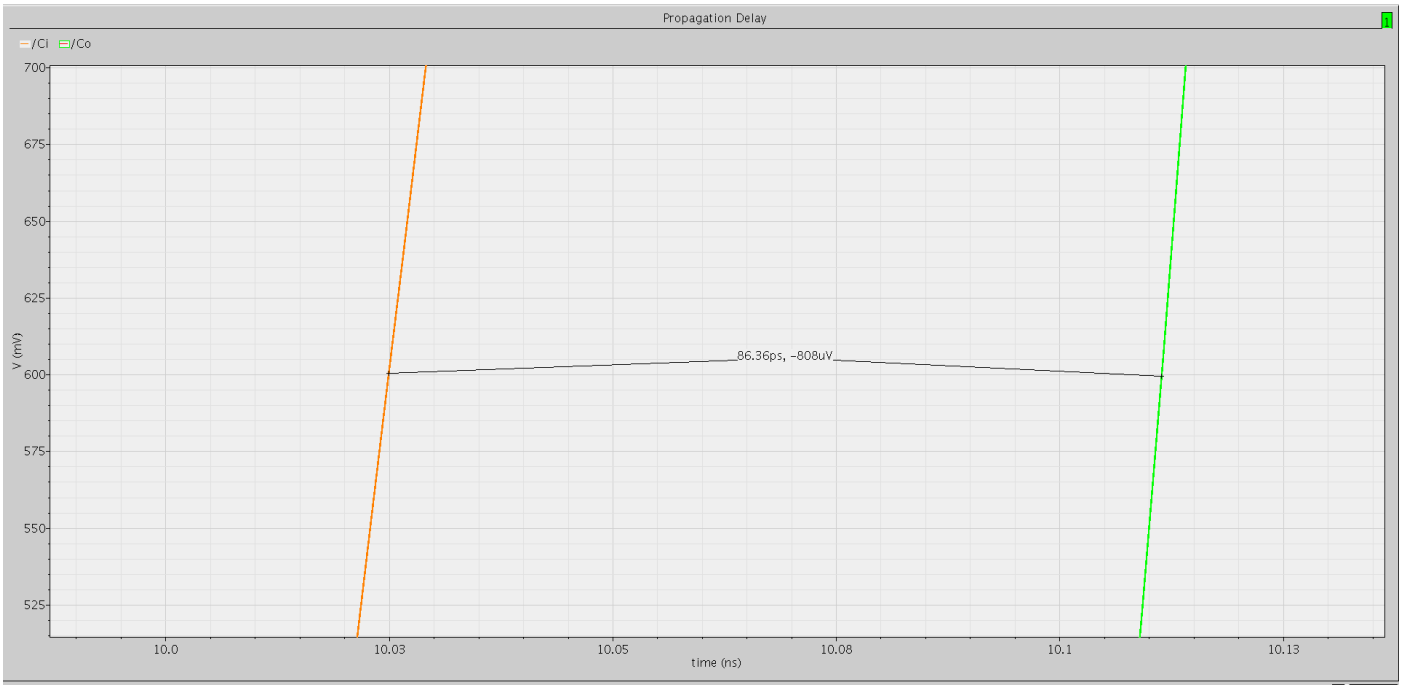


Verifying the Functionality of the Full Adder Circuit

Names	Value
delay(VT("/Co") 0.6 1 "either" V...	-8.664E-11

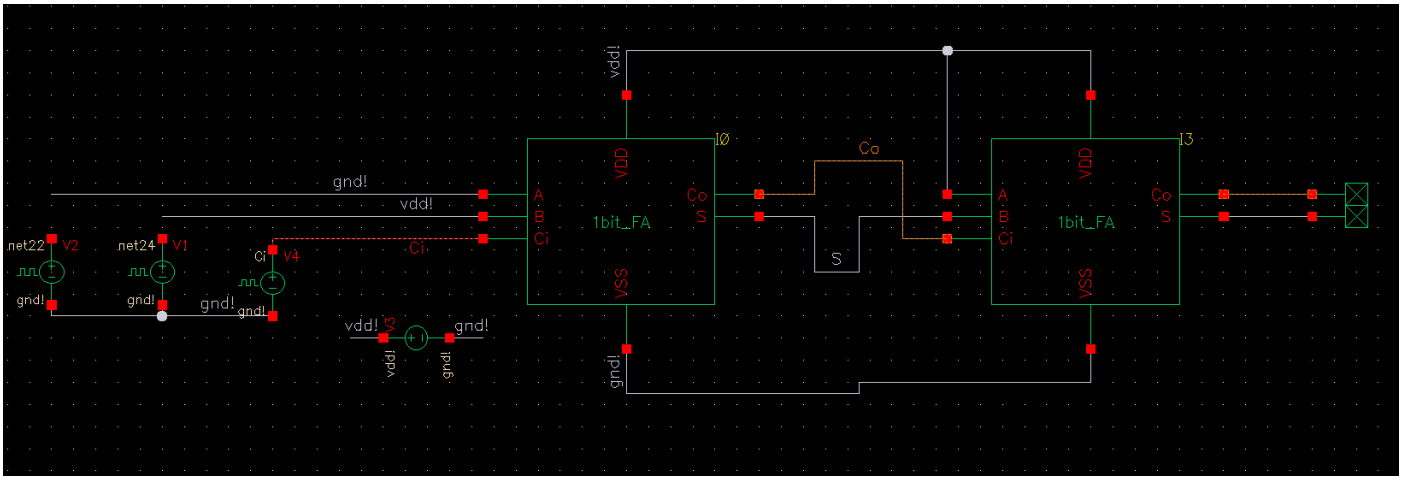
Propagation delay for single 1-bit full adder without load = 86.64 pS





Names	Value
average(abs(i("/V3/PLUS" ?result...	1.552E-5

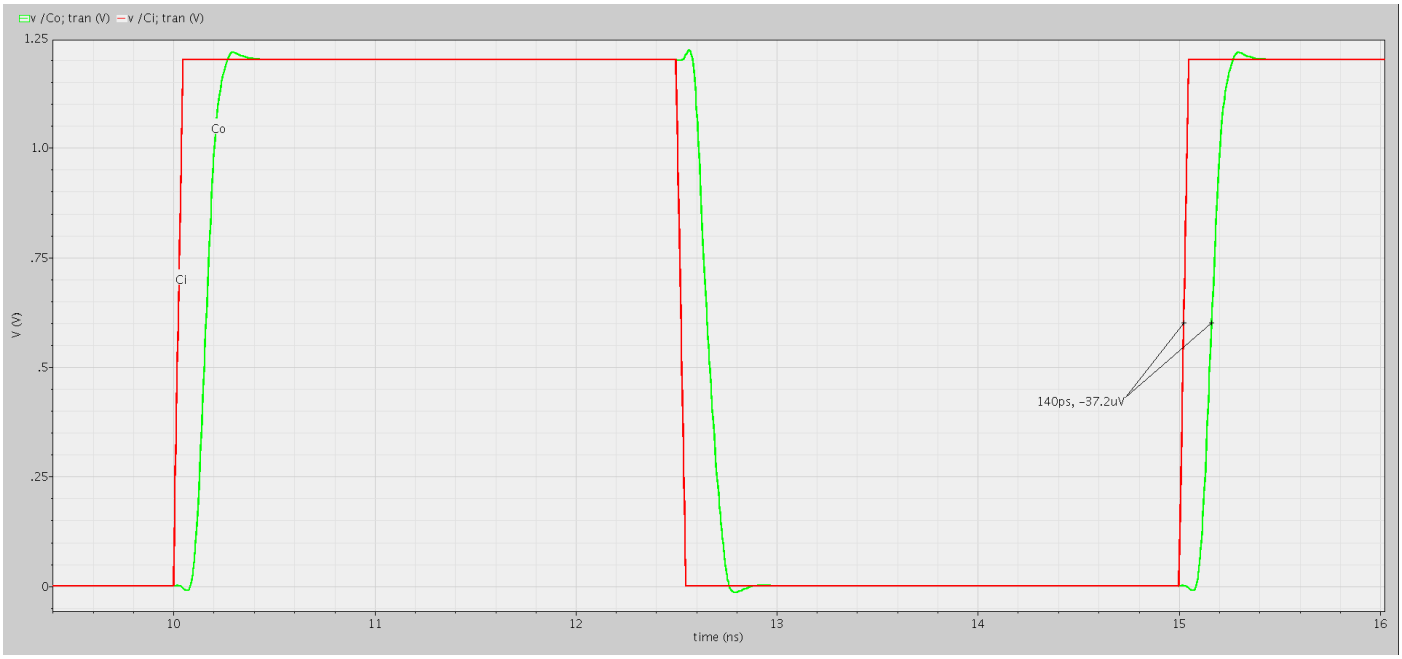
Power Consumption = 15.5 uW

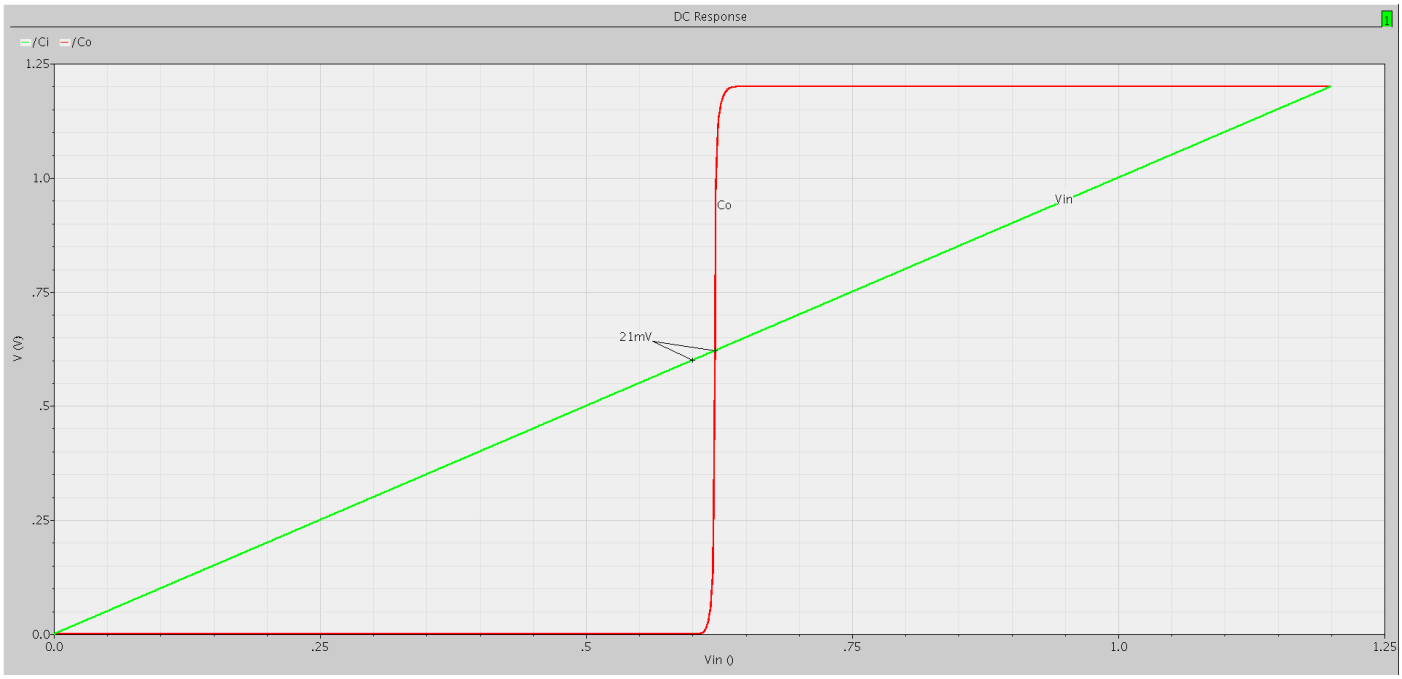


Test bench schematic for calculating the propagation delay with 1 FA Load

Names	Value
delay(VT("/Co") 0.6 1 "either" V...	-1.392E-10

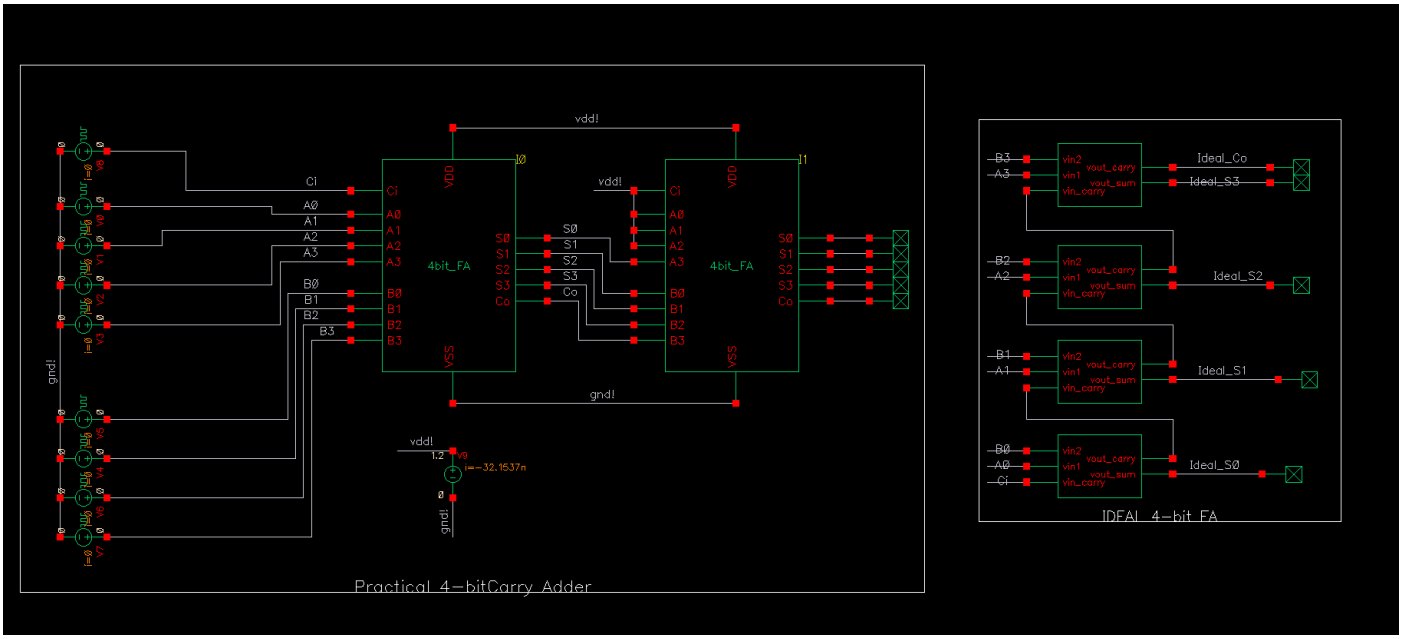
Propagation delay for one loaded 1-bit FA = 139.2 pS



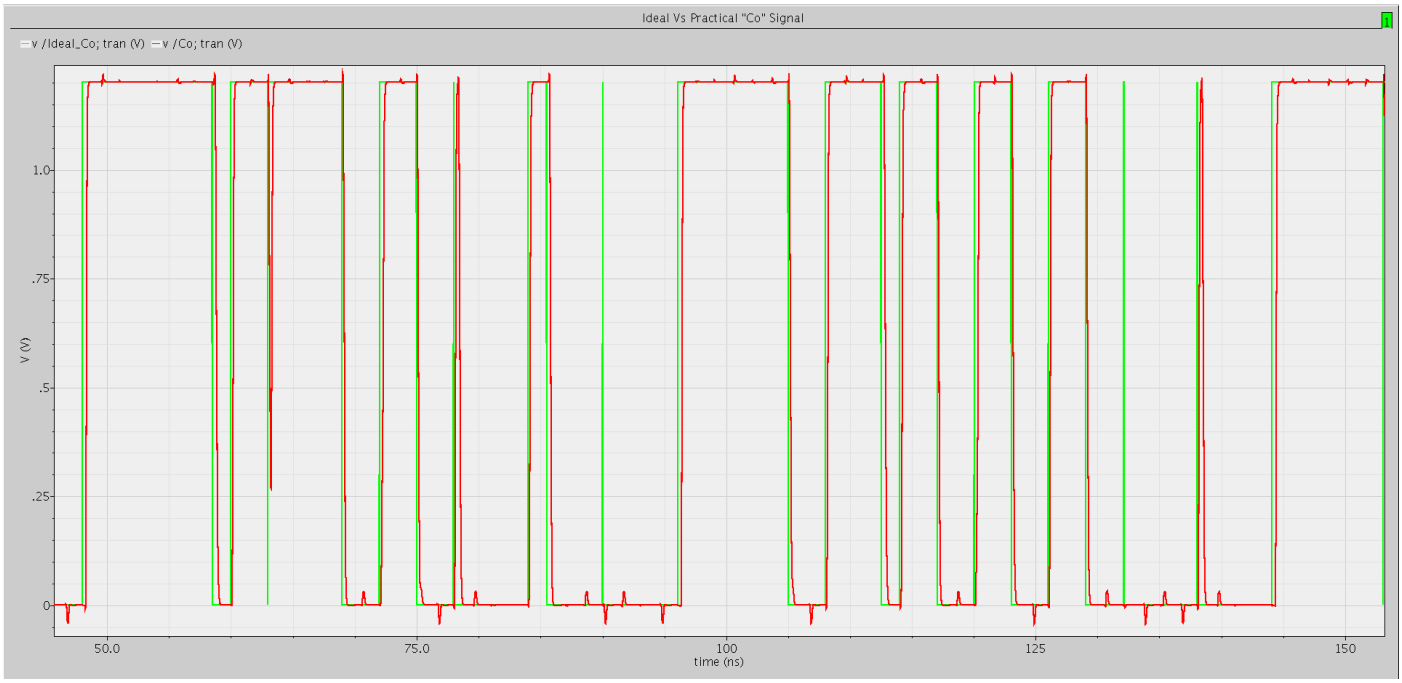


DC Transfer Characteristics, Changing “Cin” from 0 to 1.2 V linearly and monitoring “Co”.

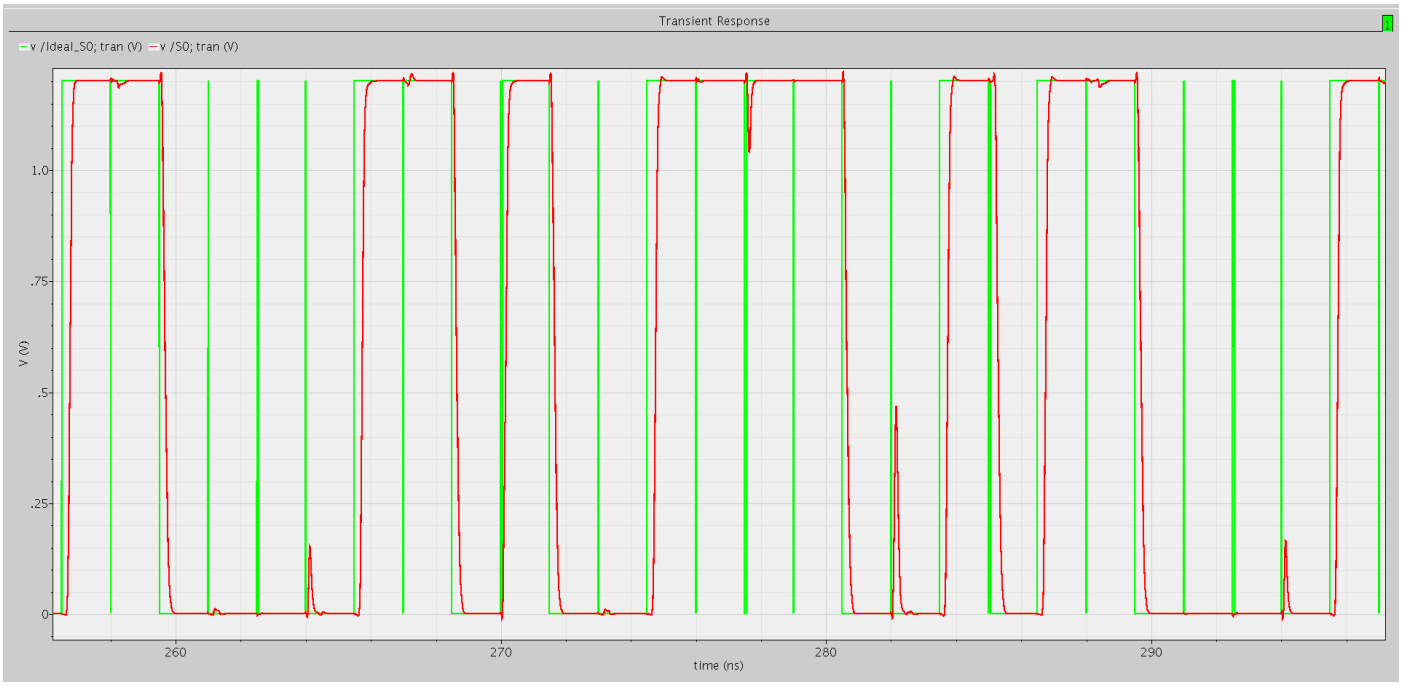
The mid point is 620 mV, we can redesign for closer point to 600 mV.



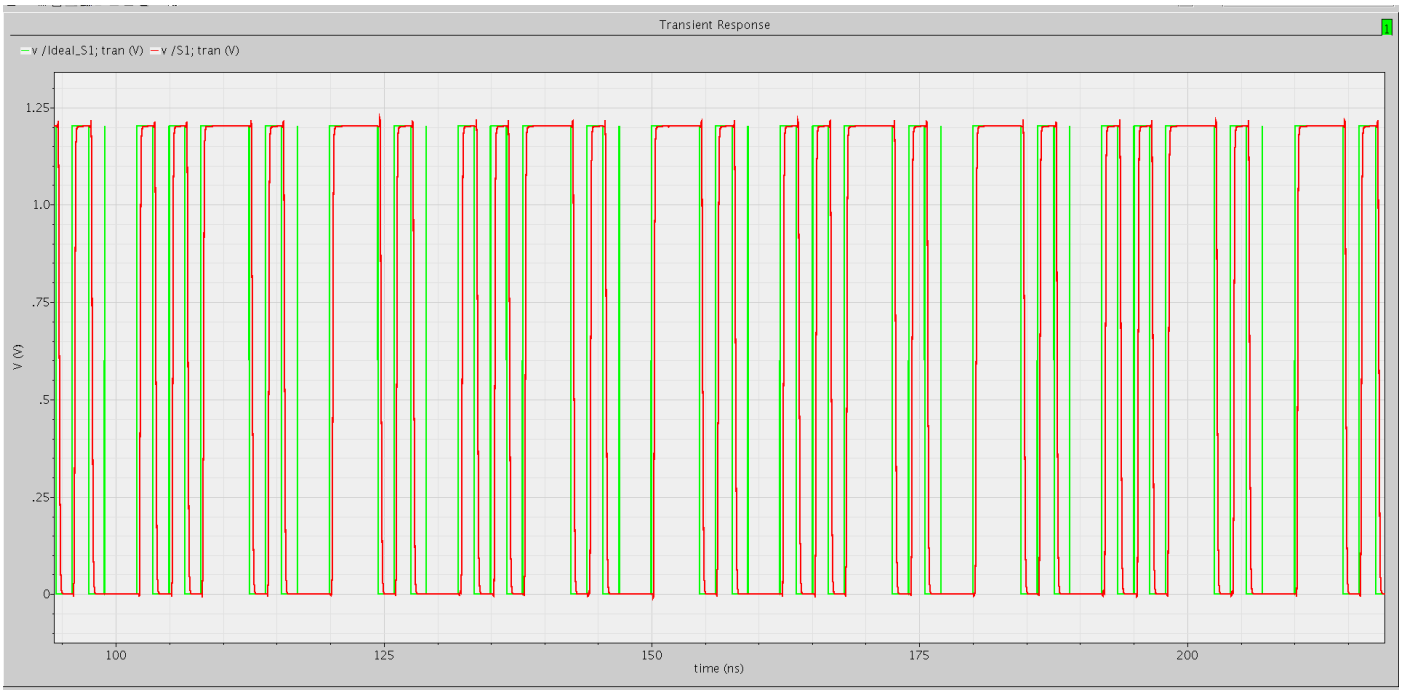
Circuit Test Bench, with Ideal 4-bit Carry Adder to verify the output of the designed Circuit



Ideal and Practical “Co” signals

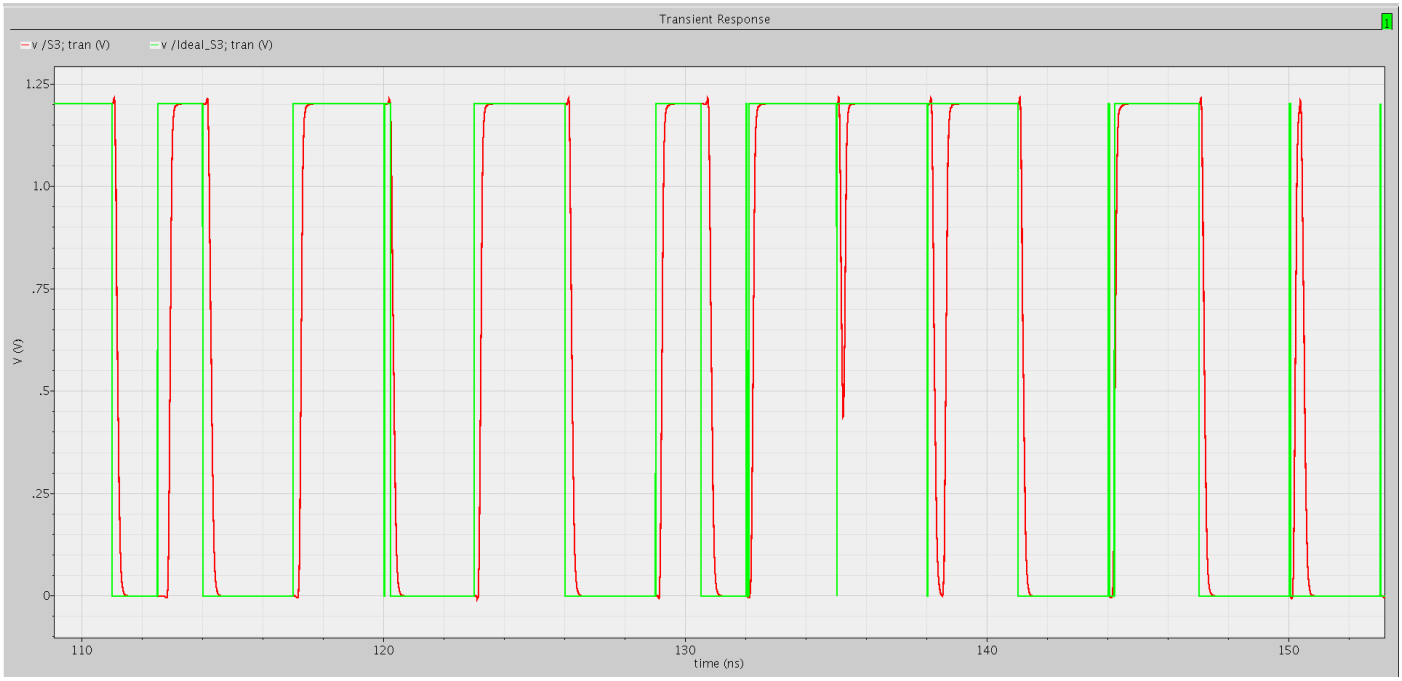


Ideal and Practical “S0” signals



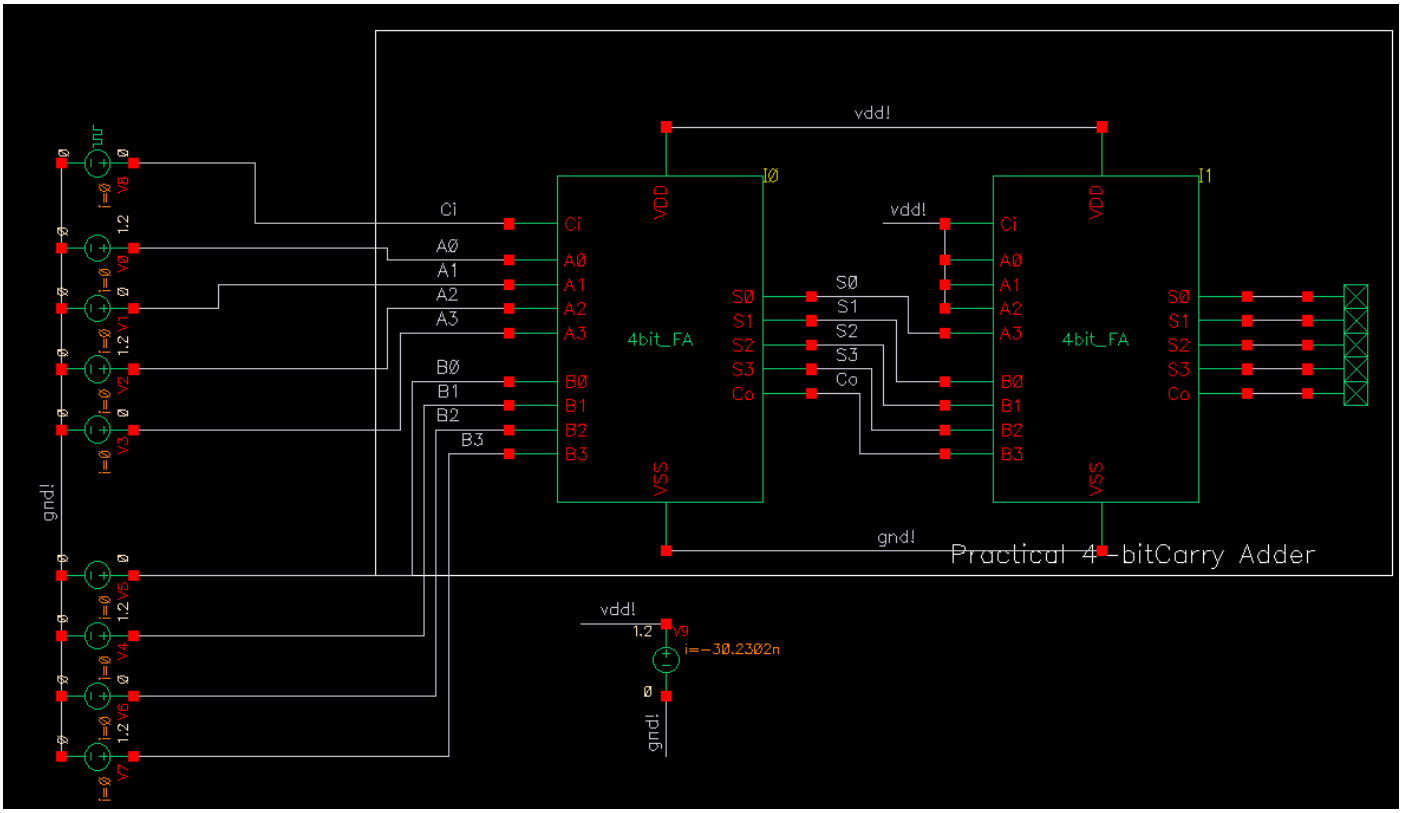
Ideal and Practical “S1” signals

Ideal and Practical “S2” signals



Ideal and Practical “S3” signals

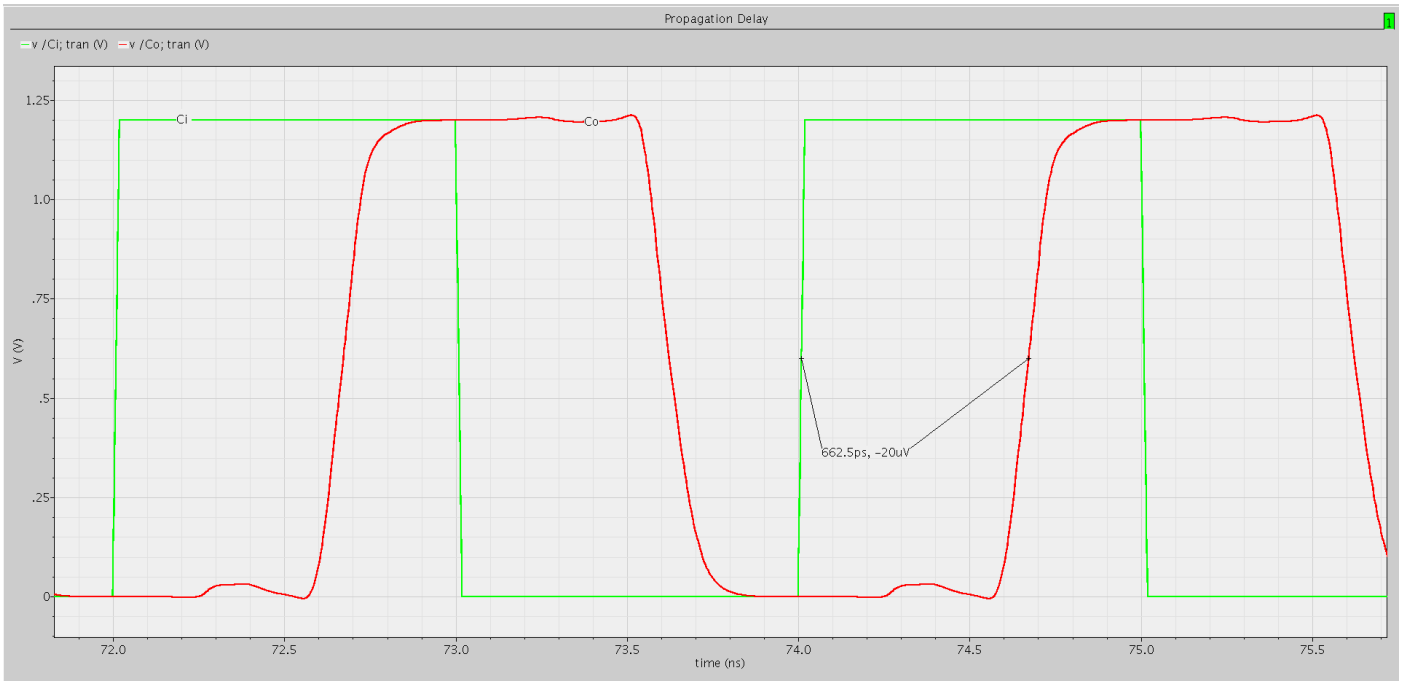
Now we have verified the functionality of the 4-bit ripple carry adder designed circuit.



We have set Ci to 500 MHz clock while A = 0101 , B = 1010, so as to mirror the input carry to the output carry.

Names	Value
delay(VT("/Ci") 0.6 1 "either" VT...	6.622E-10

Propagation Delay of the 4-bit ripple adder between Ci and Co of the final stage = 662.5 pS

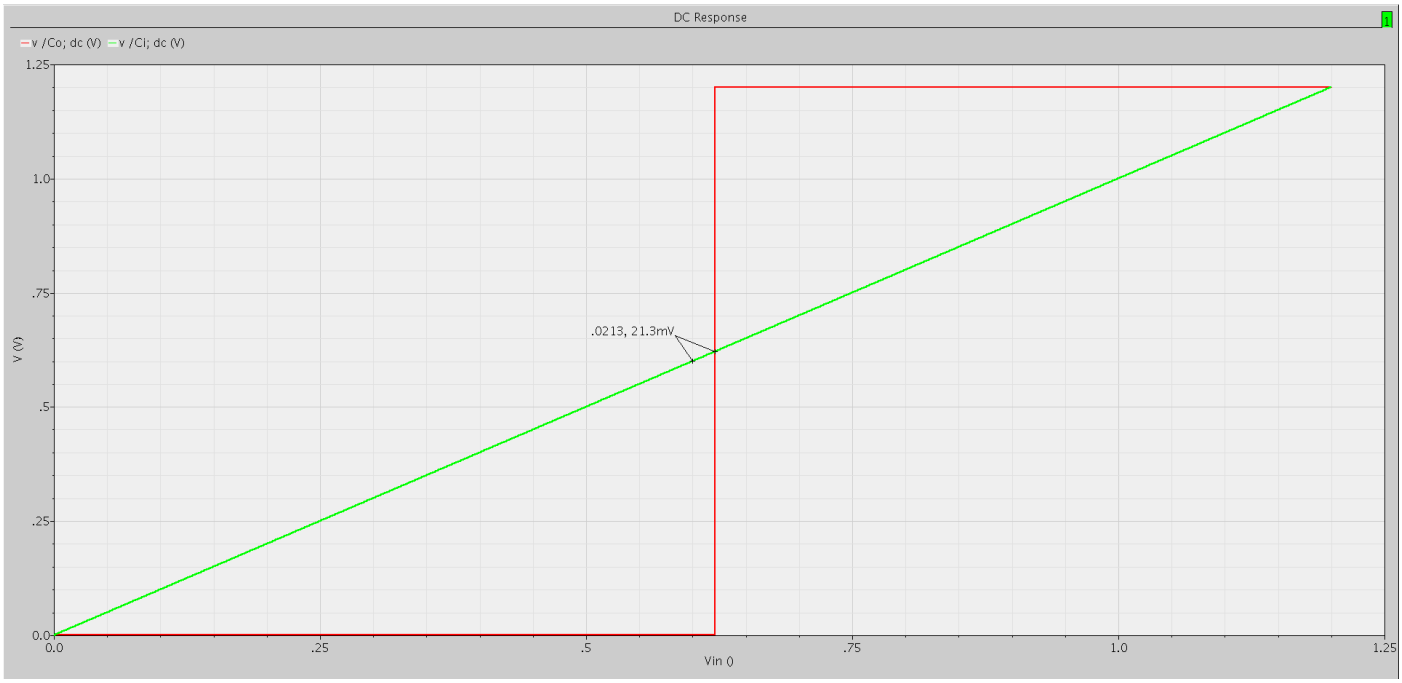


Names	Value
frequency(VT("/Co"))	5.0E8

500 MHz output Carry

Approximate Power Consumption at 500 MHz Switching

pwr	373.2u



Input/Output Transfer Characteristics for Ci to Co

CONCLUSION

Transistor Sizing for a single bit FA:

- 2 Inverters each one with PMOS (1105n/130n) and NMOS (250n/130n)

- 3 Stacked PMOS transistors with (3*1105n/130n)

- 3 Stacked NMOS transistors with (3*250n/130n)

- 9 transistors for the rest of PUN (Pull Up Network) with (2*1105n/130n)

- 9 transistors for the rest of PDN (Pull Down Network) with (2*250n/130n)

With total number of 28 Transistors for a single cell.

Area Estimation:

PMOS: (9*2 + 3*3 + 2*1) * 1105n * 130n = 4.1658 um^2 without routing

NMOS: (9*2 + 3*3 + 2*1) * 250n * 130n = 0.9425 um^2 without routing

Approximate area could be = 1.5 * (4.1658 + 0.9425) = 7.6625 um^2 for a single 1 bit FA

Total approximate area = 4 * 7.6625 = 30.65 um^2

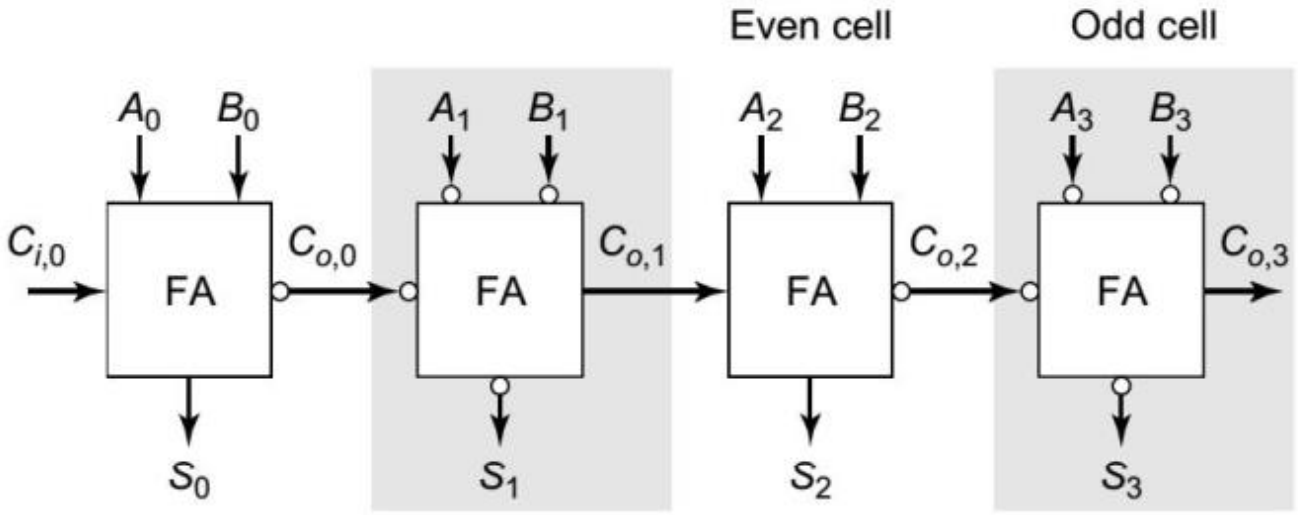
Propagation Delay: 662.5 pS

Power Consumption: 373.2 uW

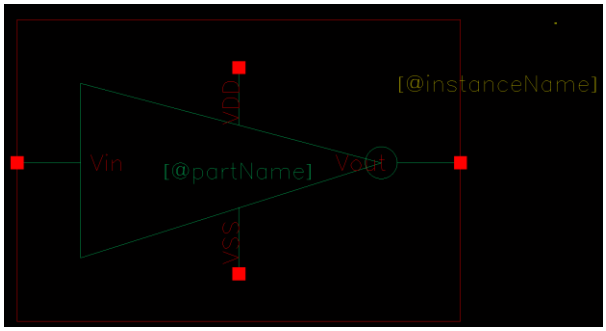
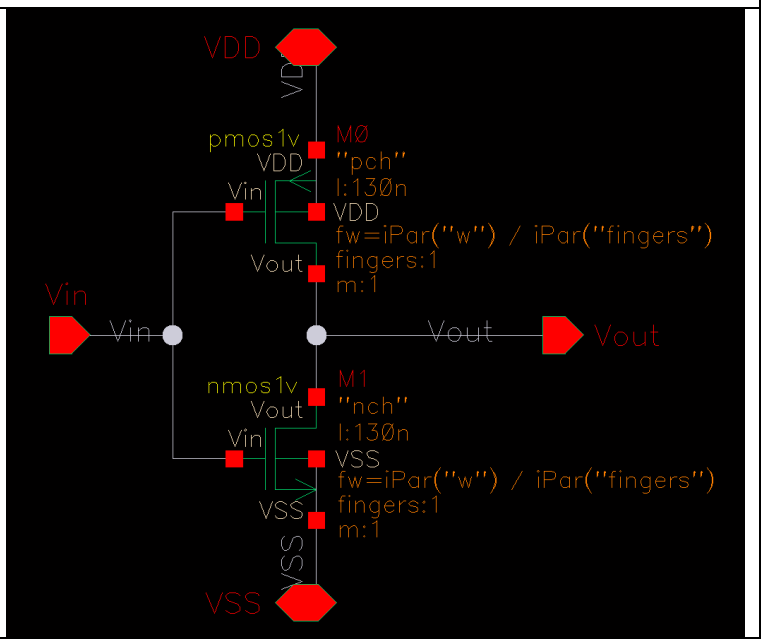
Technology: 130 nm (min Length), 150 nm (min Width)

Following We will exploit the inverting property where “Inverting all the inputs of a full-adder cell also inverts all the outputs”. This should exclude the extra inverters we added in the odd cells.

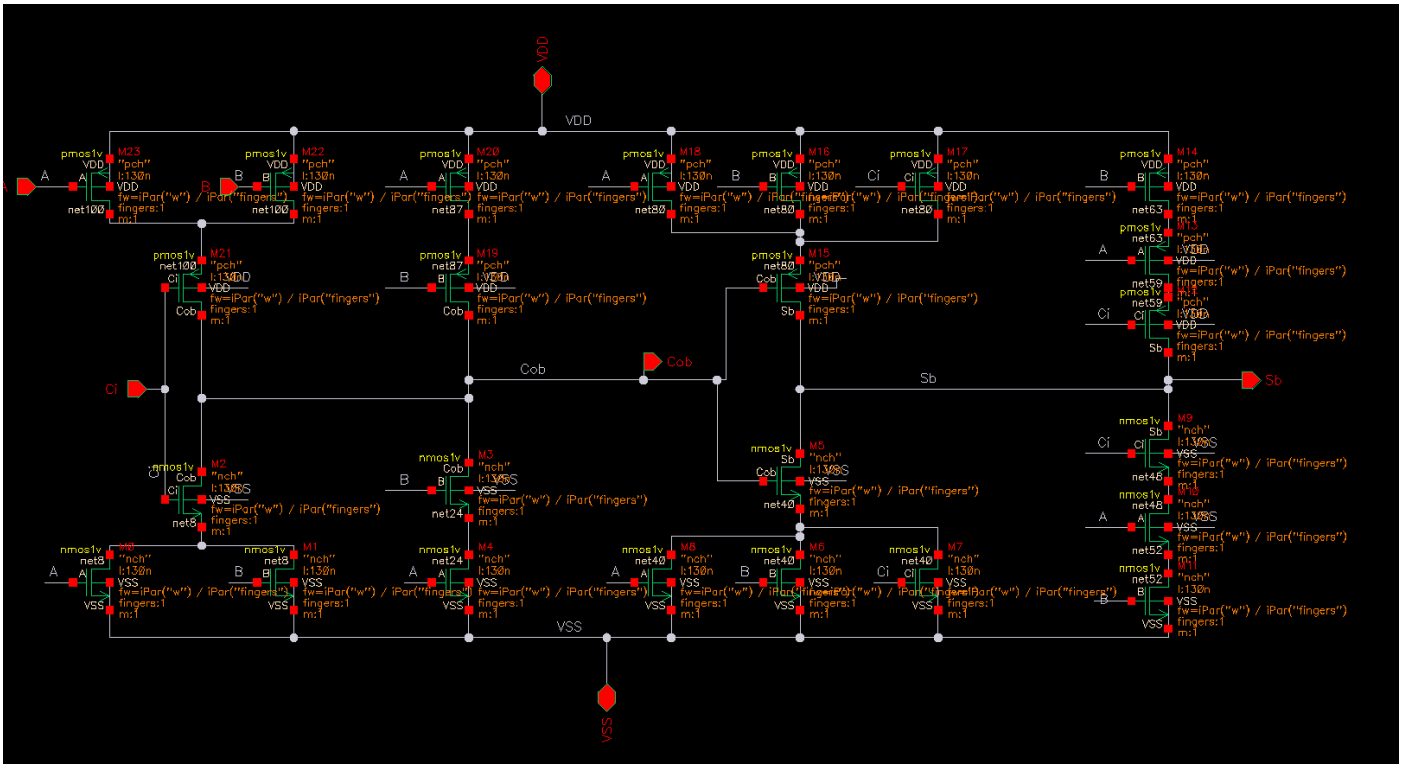
$$\overline{A'.B' + C_i'(A' + B')} \rightarrow \text{solves to} \rightarrow A.B + C_i(A + B) = C_o$$



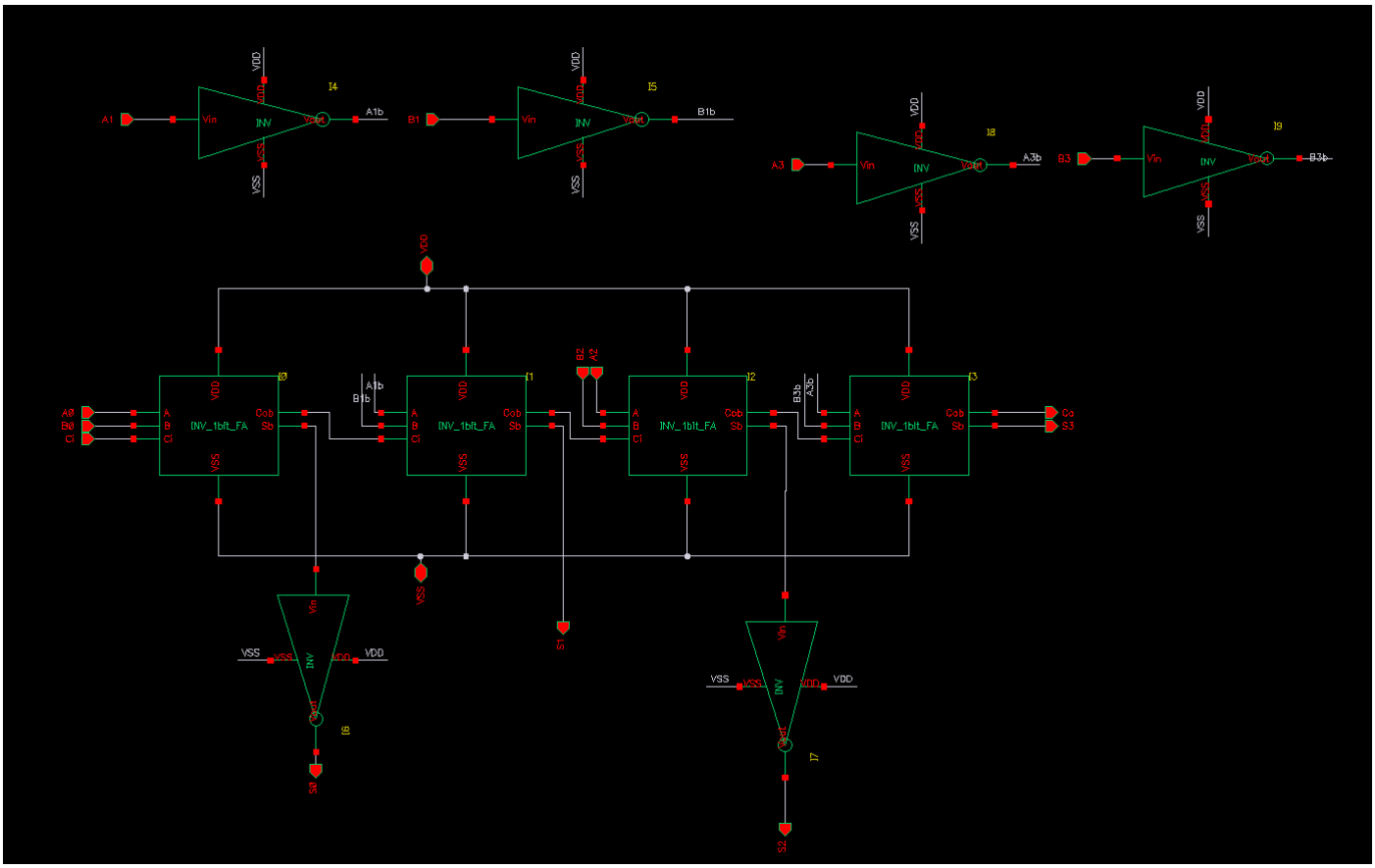
4-bit ripple carry adder

Inverter Symbol	Inverter Schematic
	

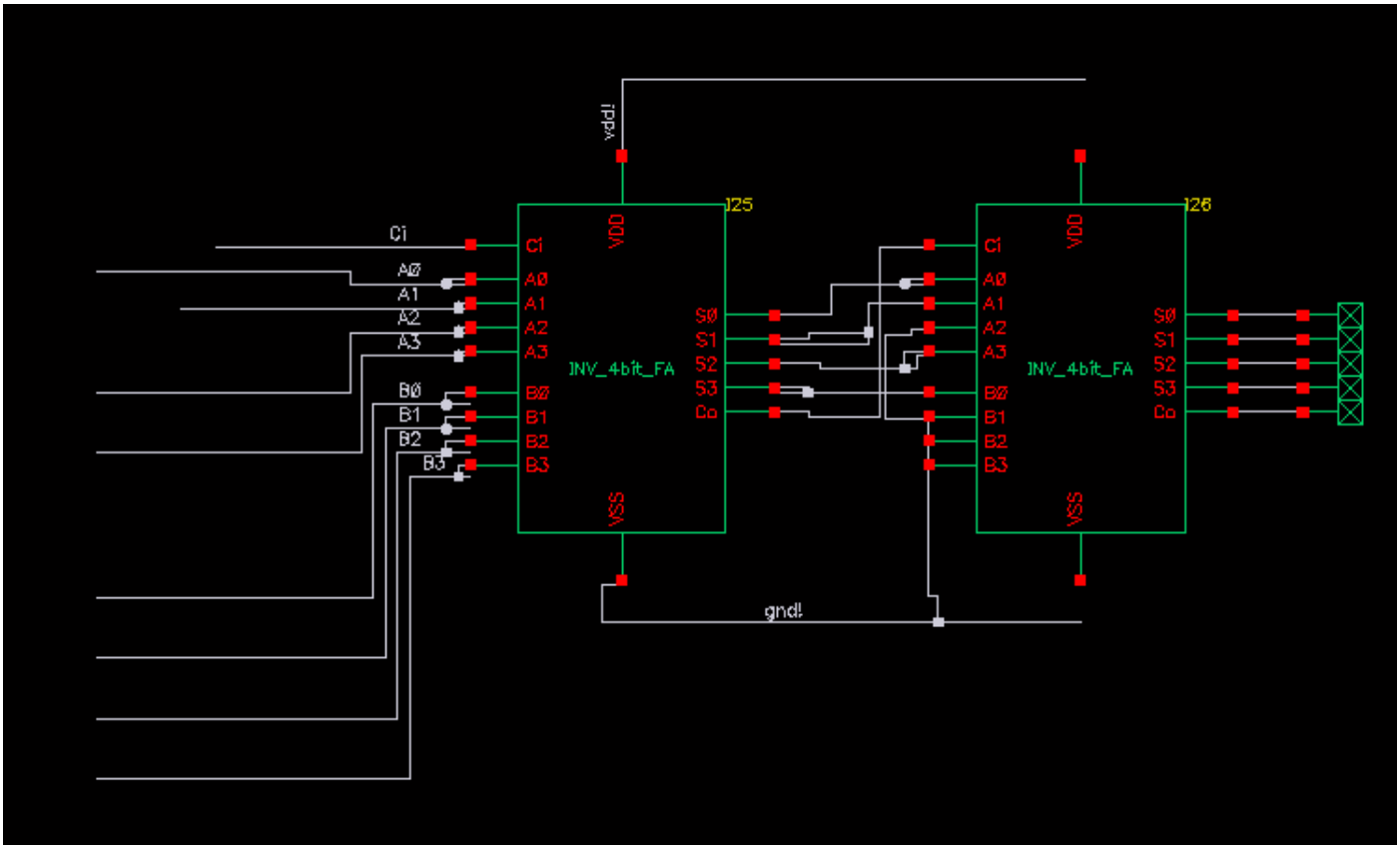
Wp = 1105n, Wn = 250n



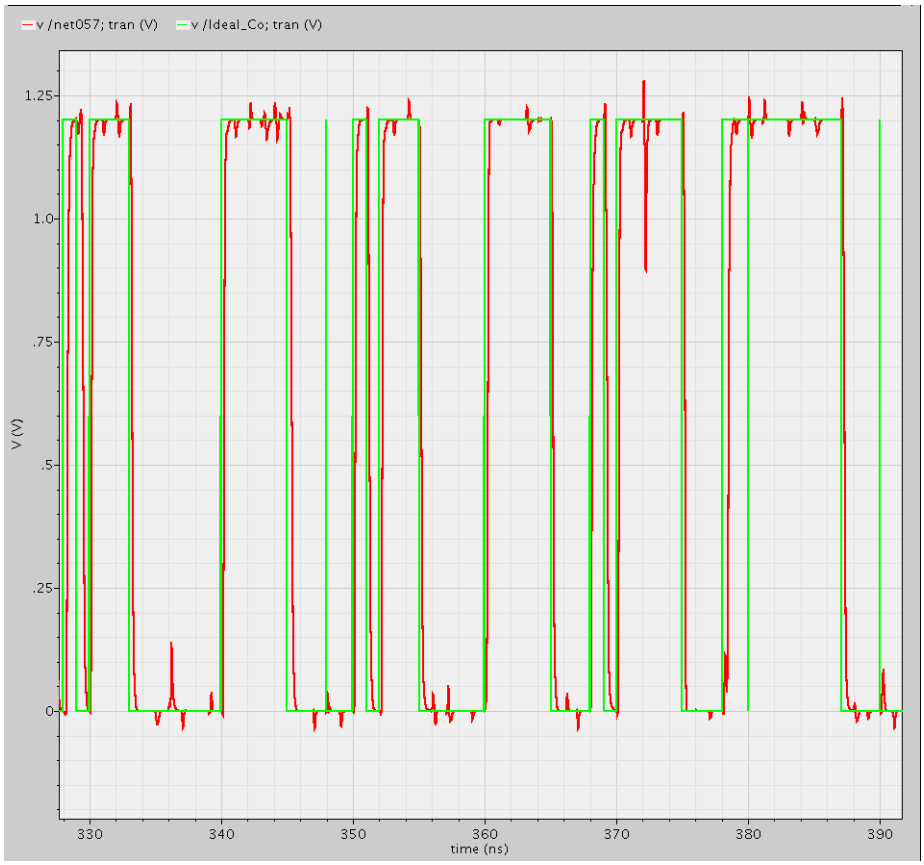
New Schematic for the single FA cell with inverted outputs without extra inverters



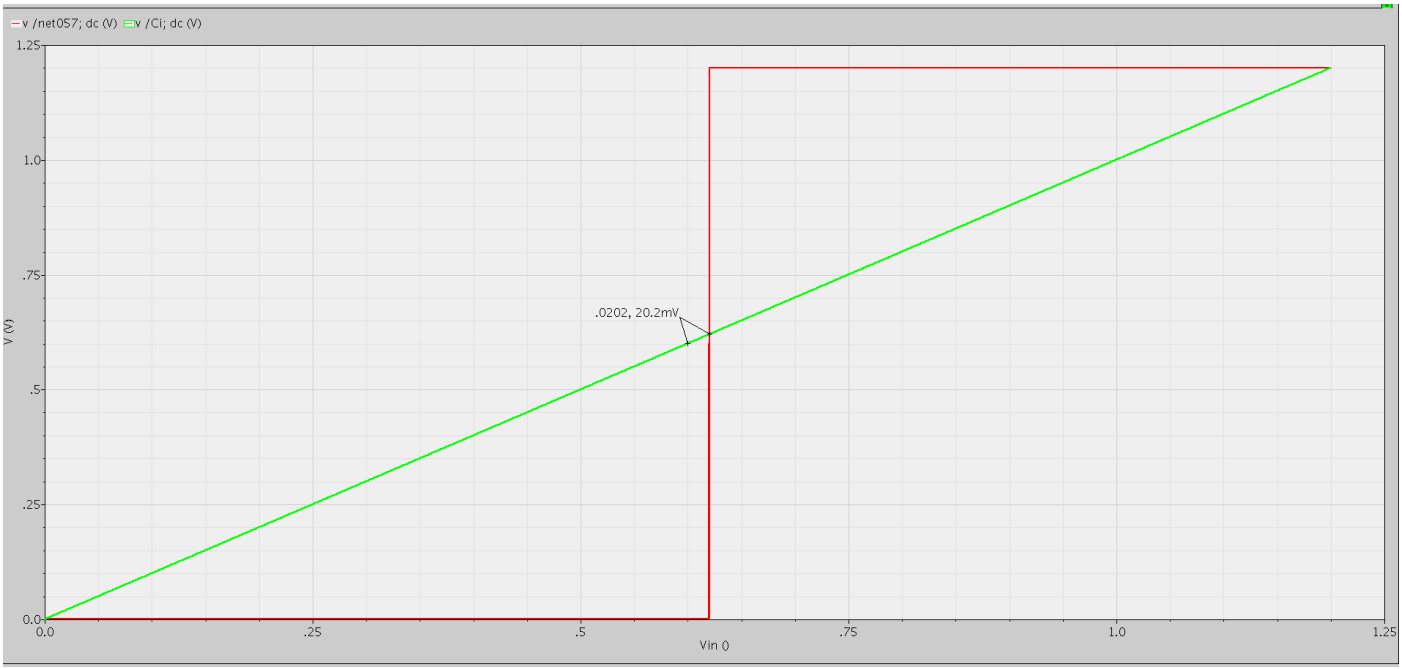
The Connections of the inverters, reducing the total inverter count by two and reducing the inverters at the critical path by 4.



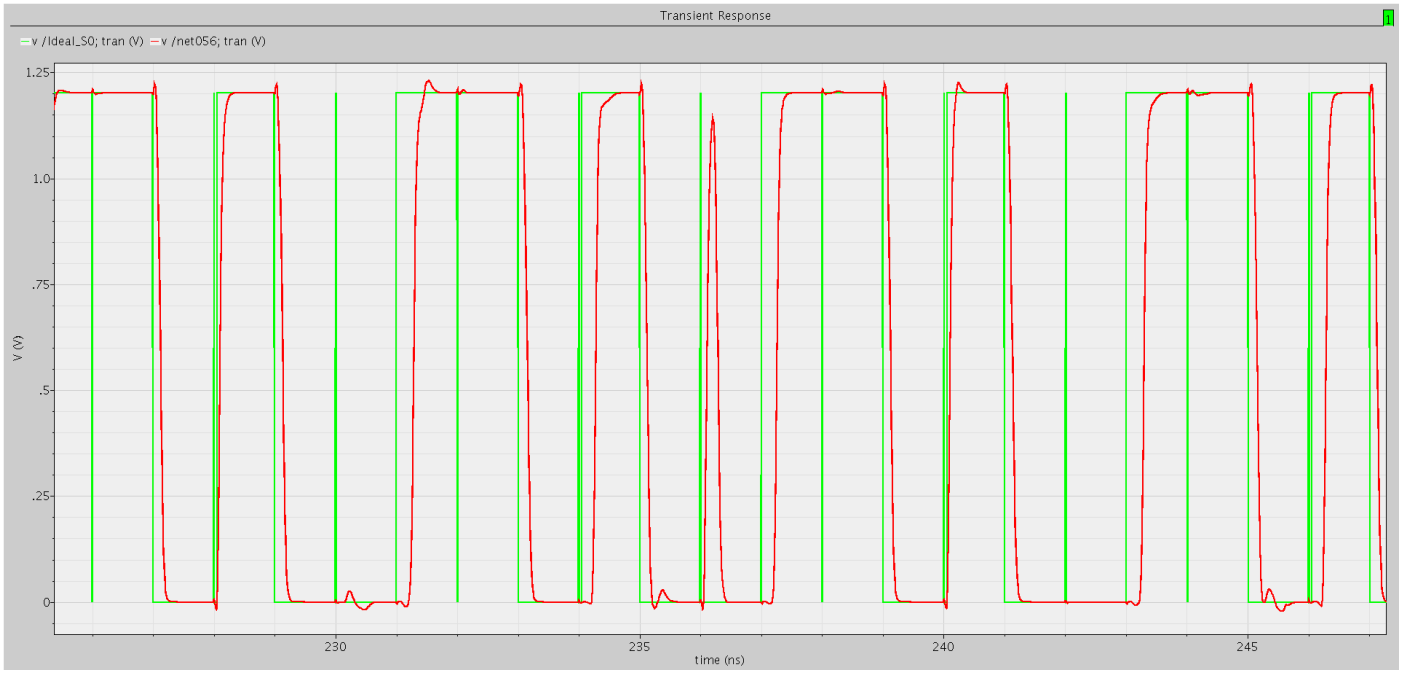
The New Design Test Bench



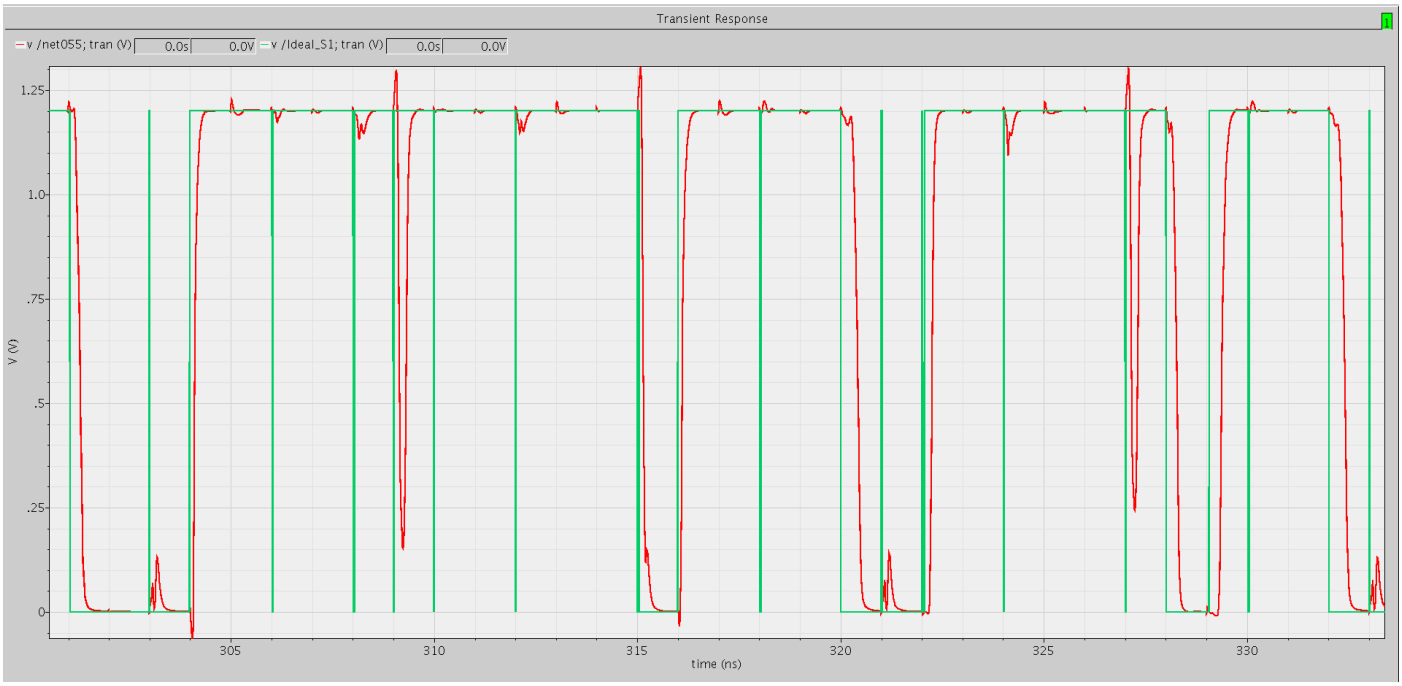
Ideal and Practical “Co” signals



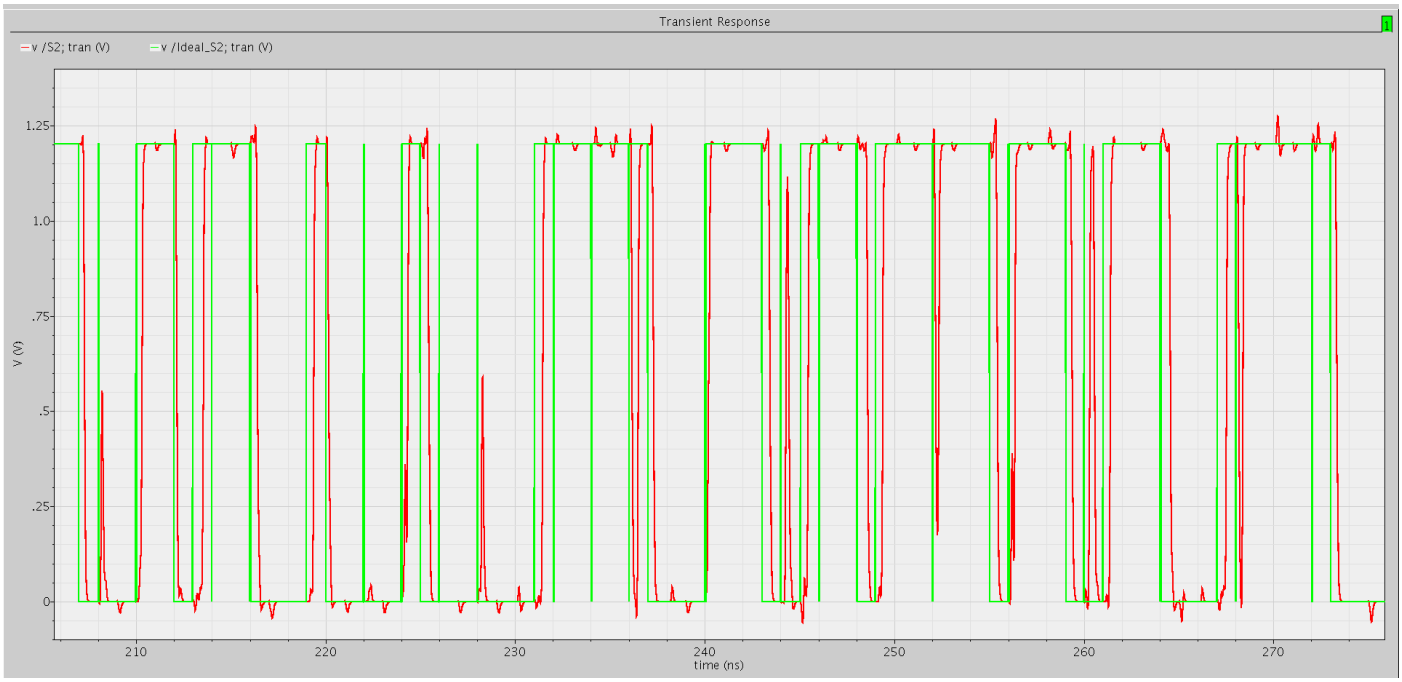
Voltage Transfer Characteristics



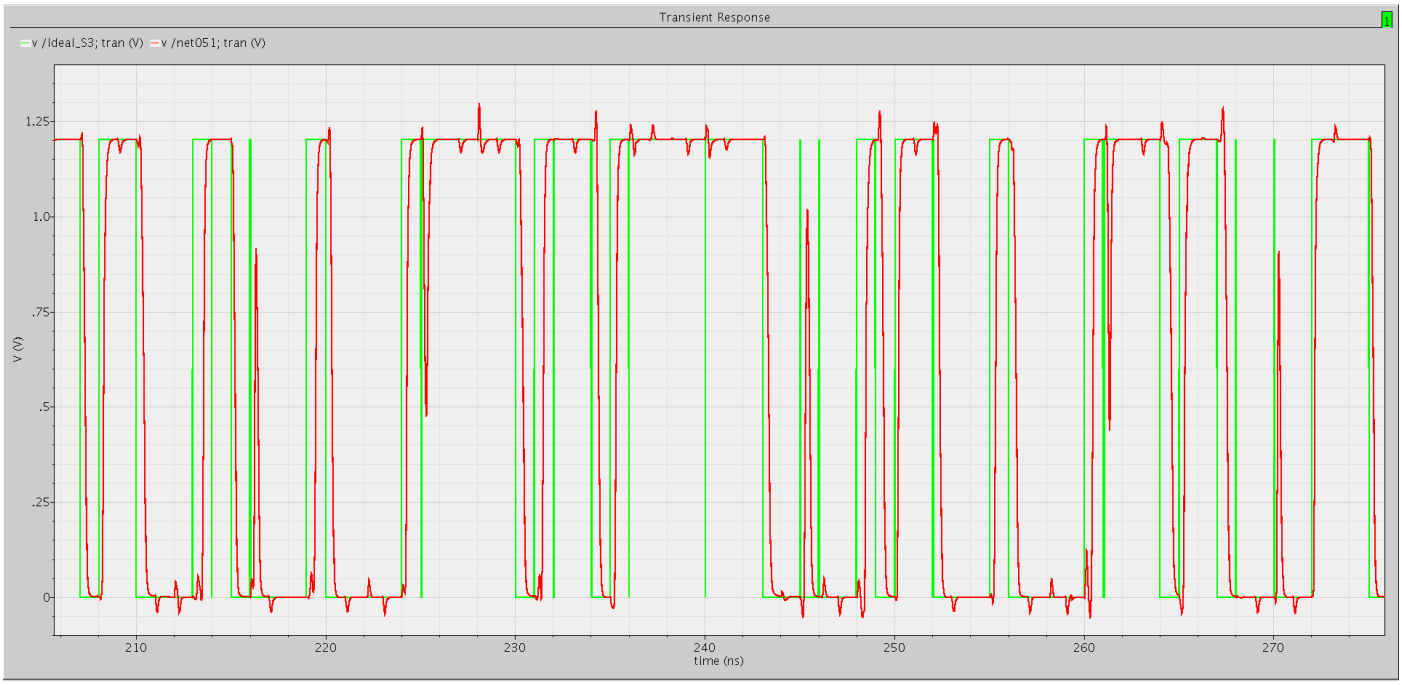
Ideal and Practical “S0” signals



Ideal and Practical “S1” signals



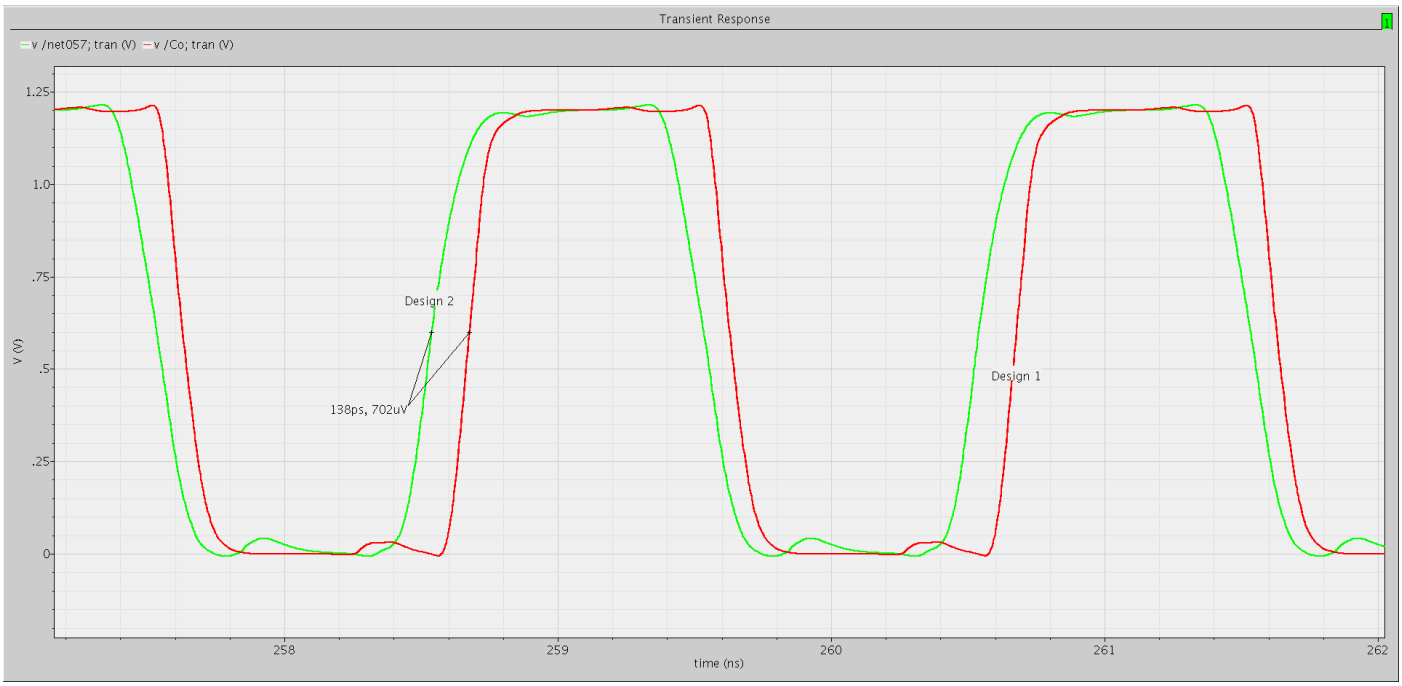
Ideal and Practical “S2” signals



Ideal and Practical “S3” signals

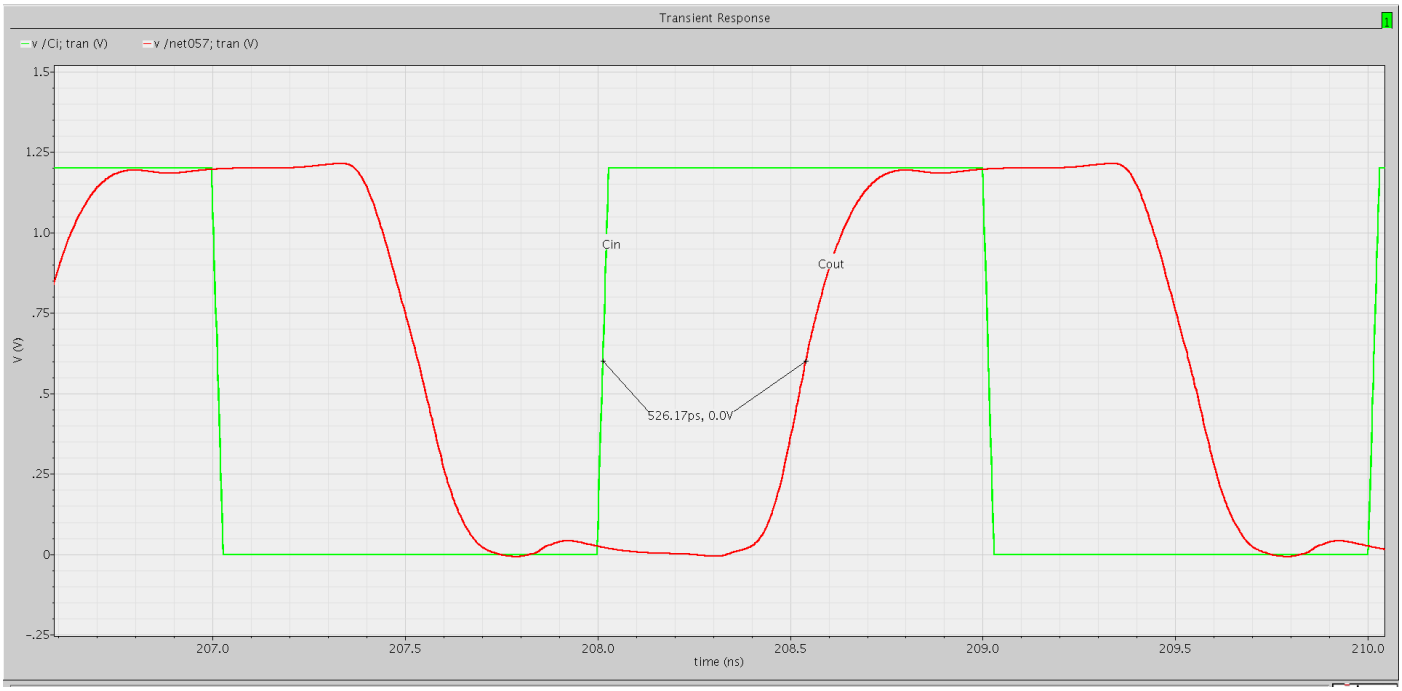
```
pwr                    304.2u
```

Power consumption for the second design = 304.2 uW




```
difference_Delay       138.3p
```

The delay Difference between the two designs of 4-bit ripple carry adder = 138.3 pS



The propagation delay of the second design = 526.17 pS

CONCLUSION

Transistor Sizing for a single bit FA:

- 3 Stacked PMOS transistors with (3*1105n/130n)

- 3 Stacked NMOS transistors with (3*250n/130n)

- 9 transistors for the rest of PUN (Pull Up Network) with (2*1105n/130n)

- 9 transistors for the rest of PDN (Pull Down Network) with (2*250n/130n)

With total number of 24 Transistors for a single cell.

In addition to another 6 Inverters for connections each one with PMOS (1105n/130n) and NMOS (250n/130n)

Area Estimation:

PMOS: (9*2 + 3*3) * 1105n * 130n = 3.87855 um^2 without routing

NMOS: (9*2 + 3*3) * 250n * 130n = 0.8775 um^2 without routing

Approximate area could be = 1.5 * (3.87855 + 0.8775) = 7.134 um^2 for a single 1 bit FA

Total approximate area = 4 * 7.134 + 6*(1.105+0.250)*0.130*1.5= 30.12 um^2

Propagation Delay: 526.17 pS

Power Consumption: 304.2 uW

Technology: 130 nm (min Length), 150 nm (min Width)