Introduction to Silicon Process and VLSI

CND121

Project #4

Delay Locked Loop (DLL)

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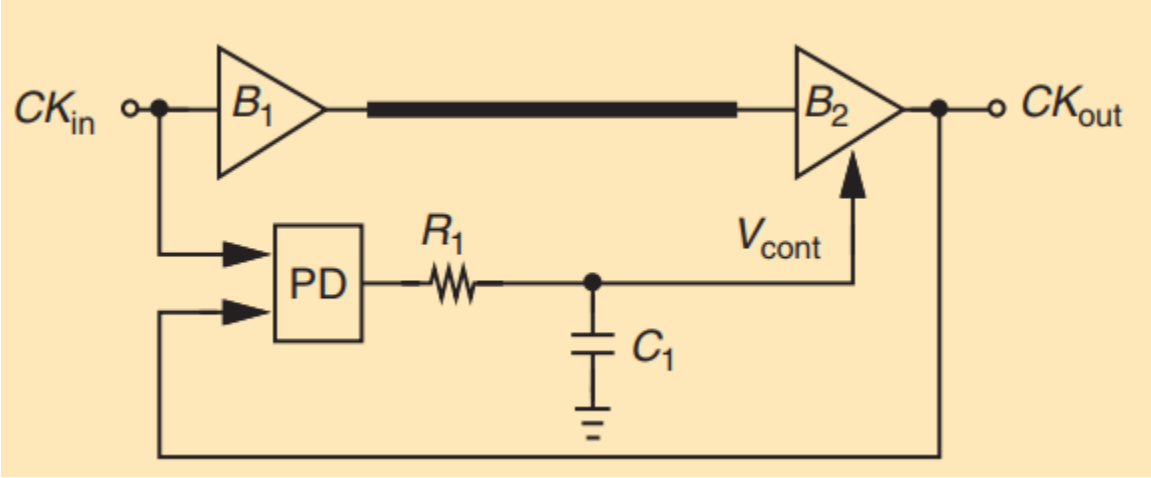
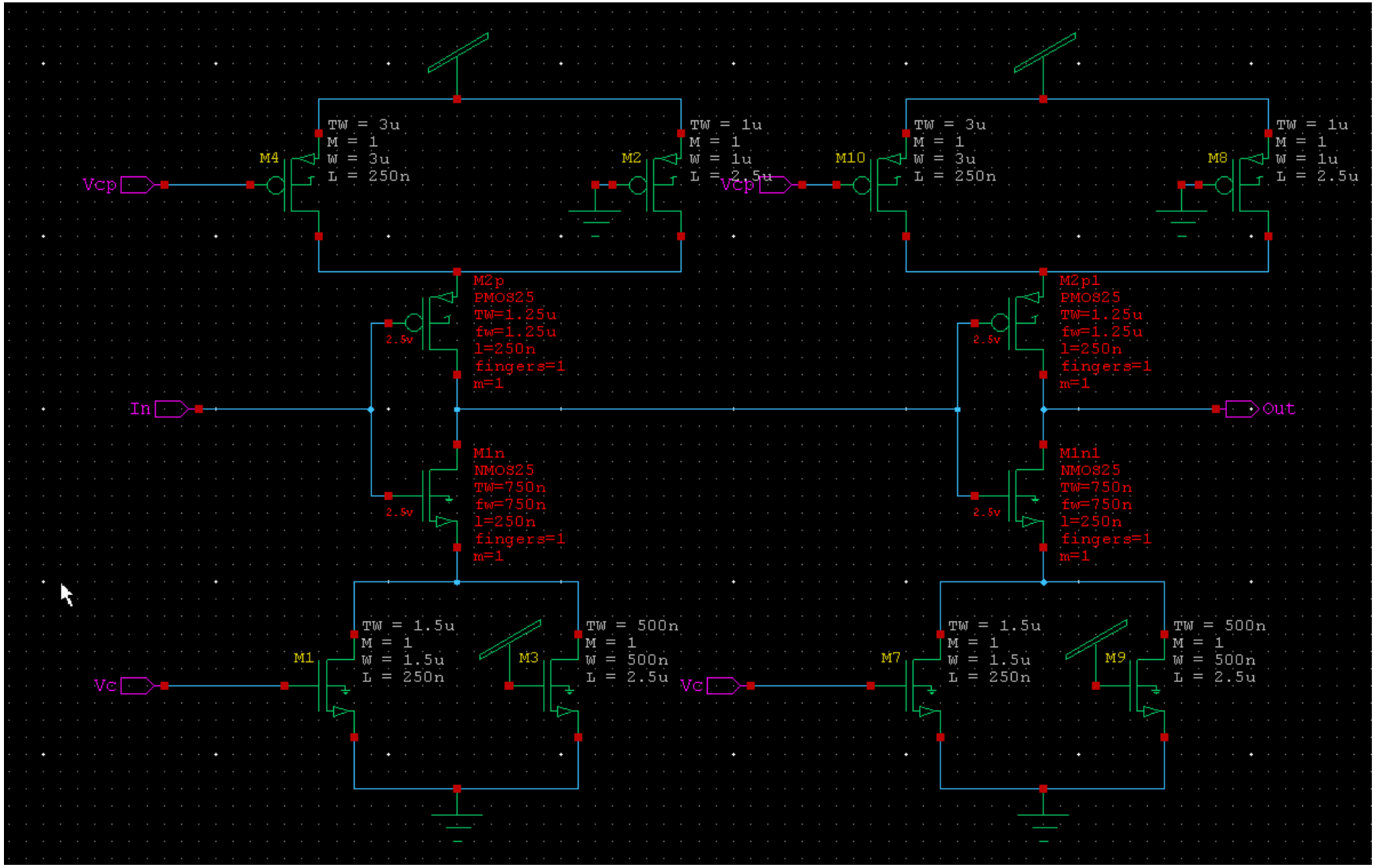
Introduction

Delay-locked loops (DLLs) can be considered as feedback circuits that phase lock an output to an input without the use of an oscillator. In some applications, DLLs are necessary or preferable over phase-locked loops (PLLs), with their advantages including lower sensitivity to supply noise and lower phase noise. This article deals with fundamental DLL design concepts.

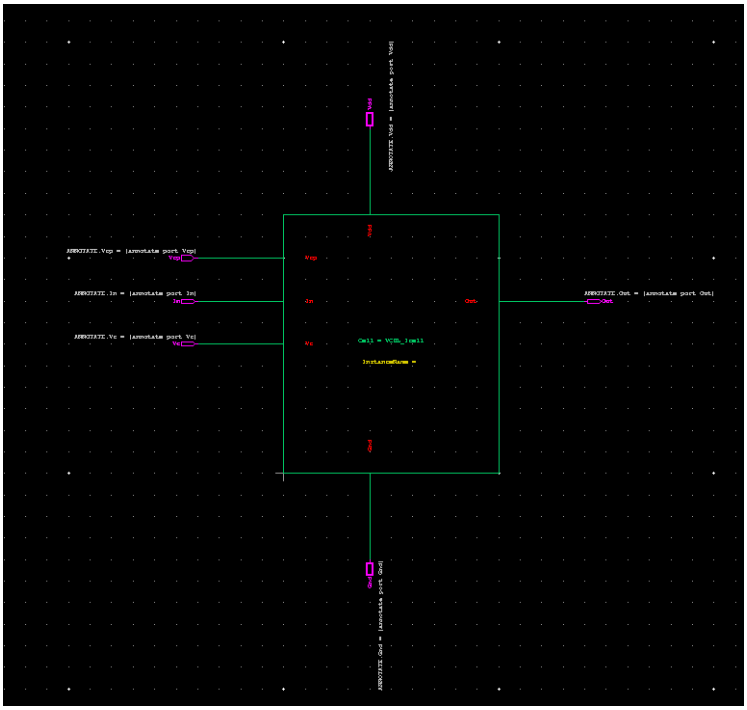
The origins of DLLs can be traced to a paper published in 1961. The authors present the topology shown in Figure 1 as a “delay-lock discriminator” operating on random signals. The feedback loop consists of a controlled delay line, a multiplier acting as a phase detector (PD), and a lowpass filter. The use of DLLs in modern CMOS design evidently began with the work by Bazes in 1985 and Johnson and Hudson in 1988.



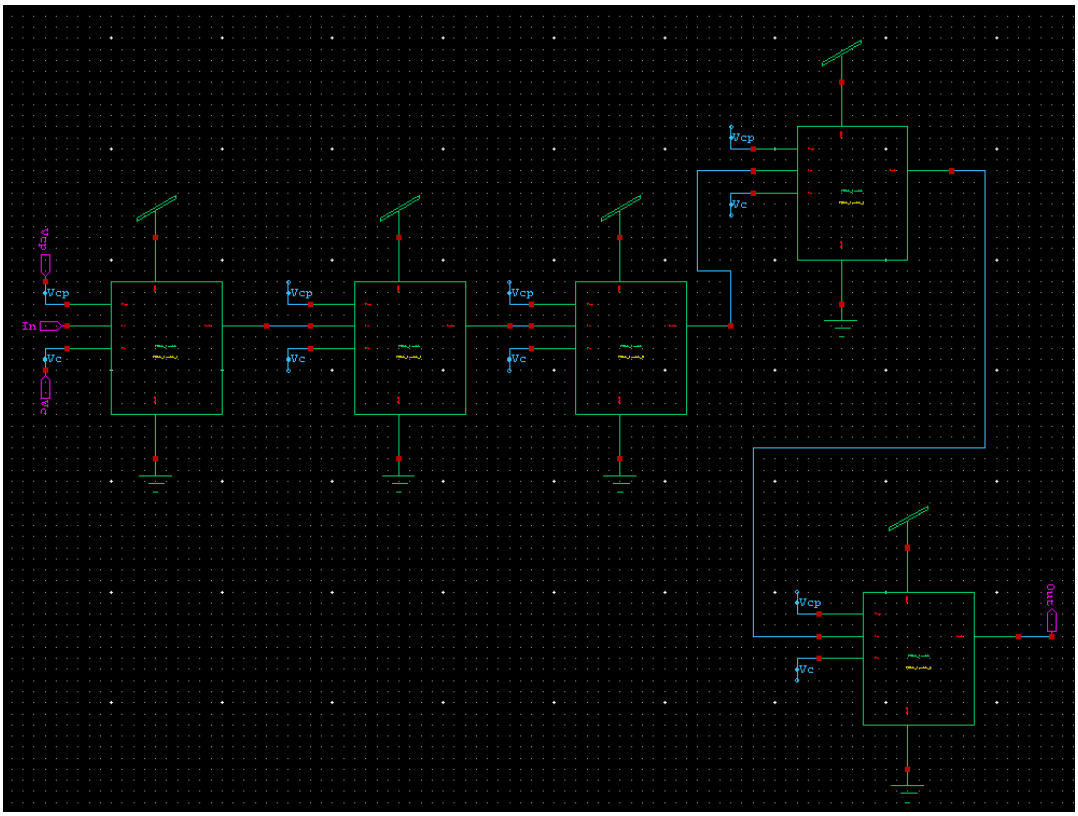
Main Cell Schematic



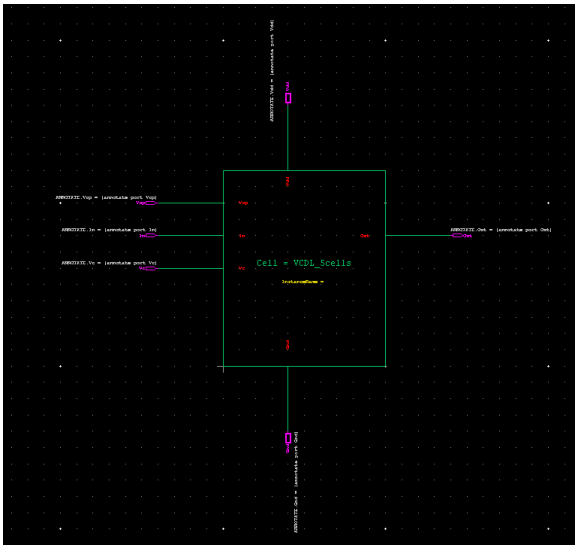
1 Cell Symbol



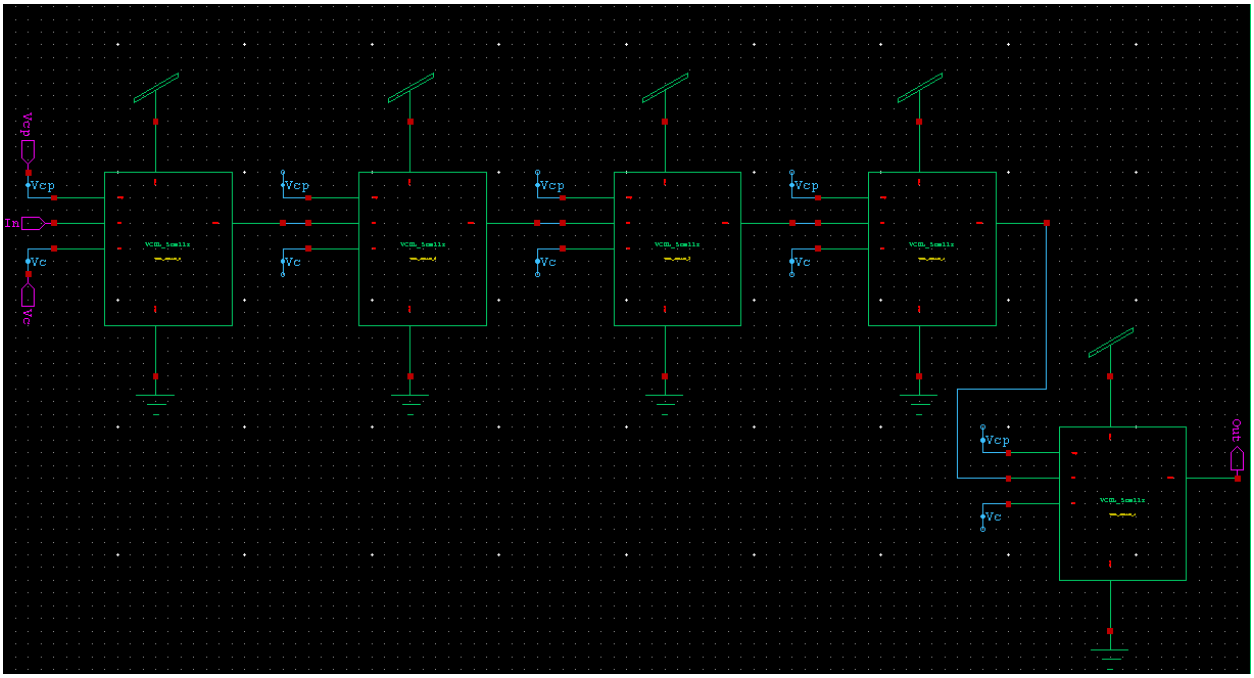
5 Cells Schematic:



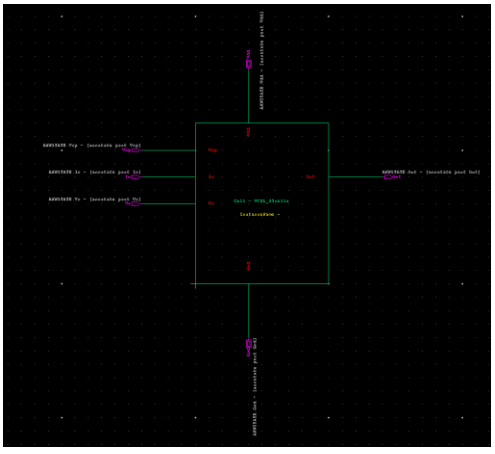
5 Cells Symbol



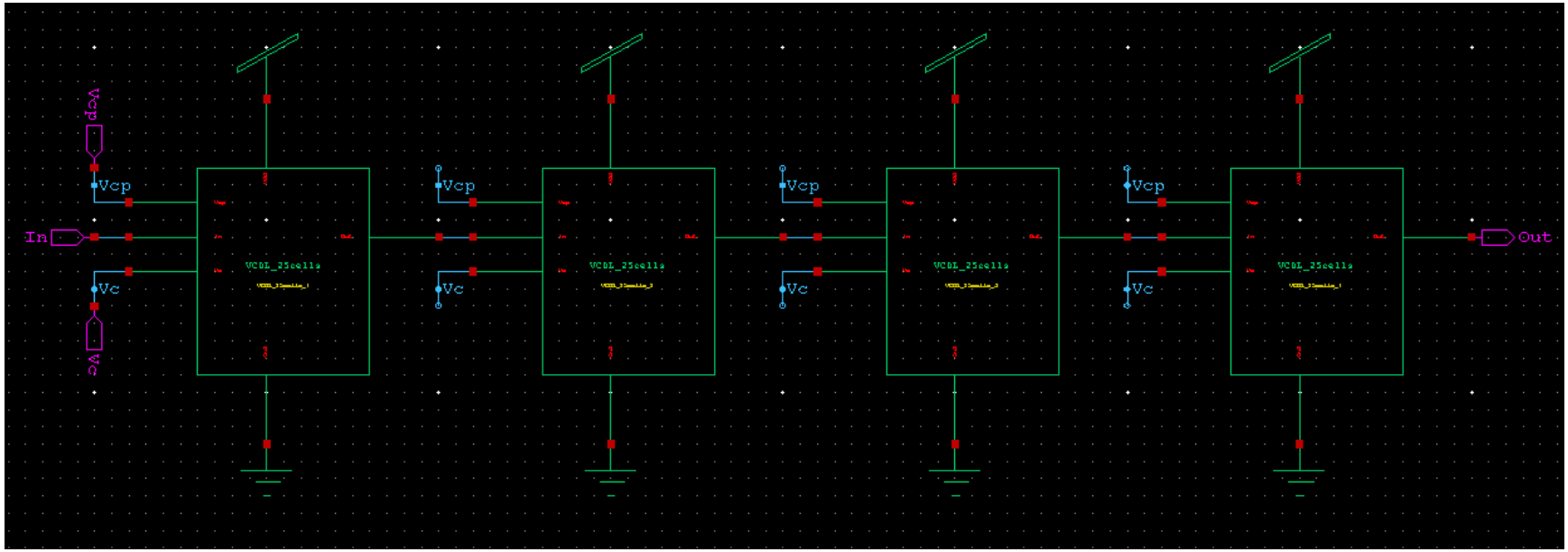
25 Cells Schematic:



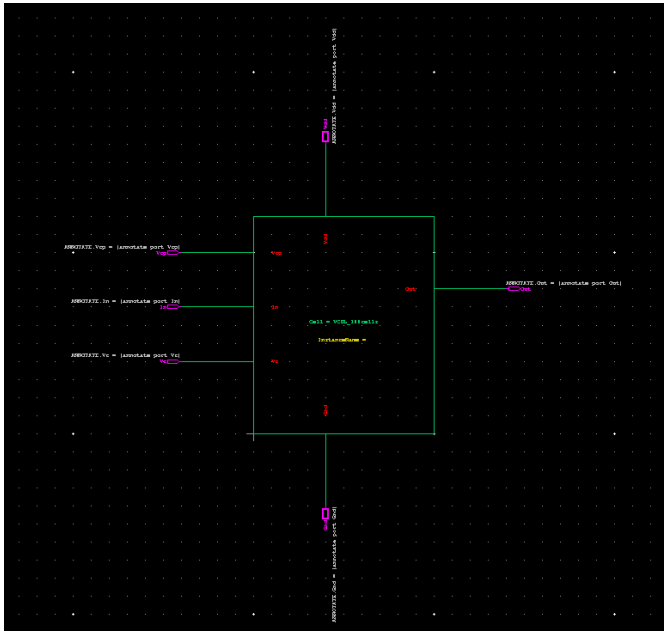
25 Cells Symbol:



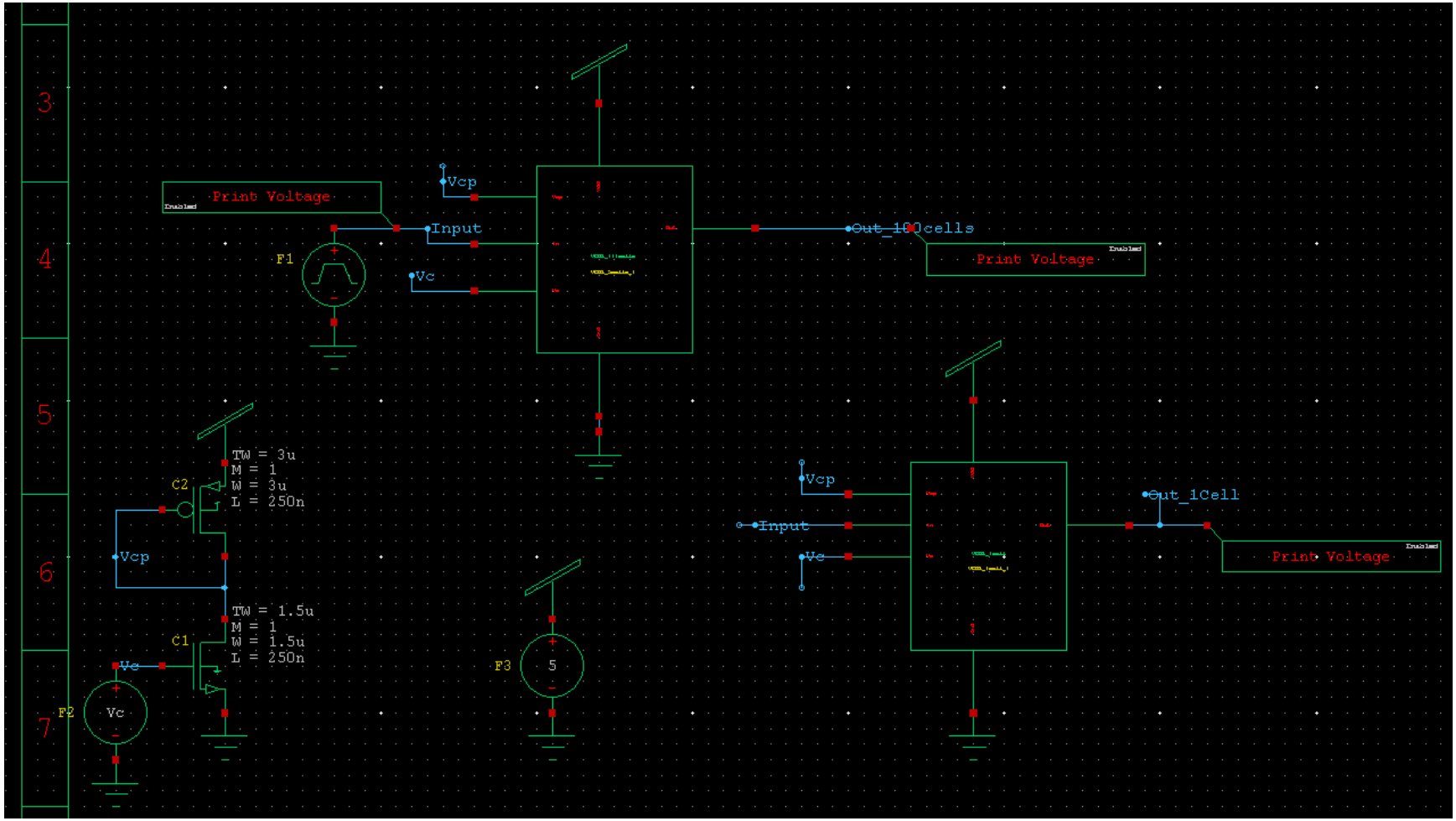
100 Cells Schematic:



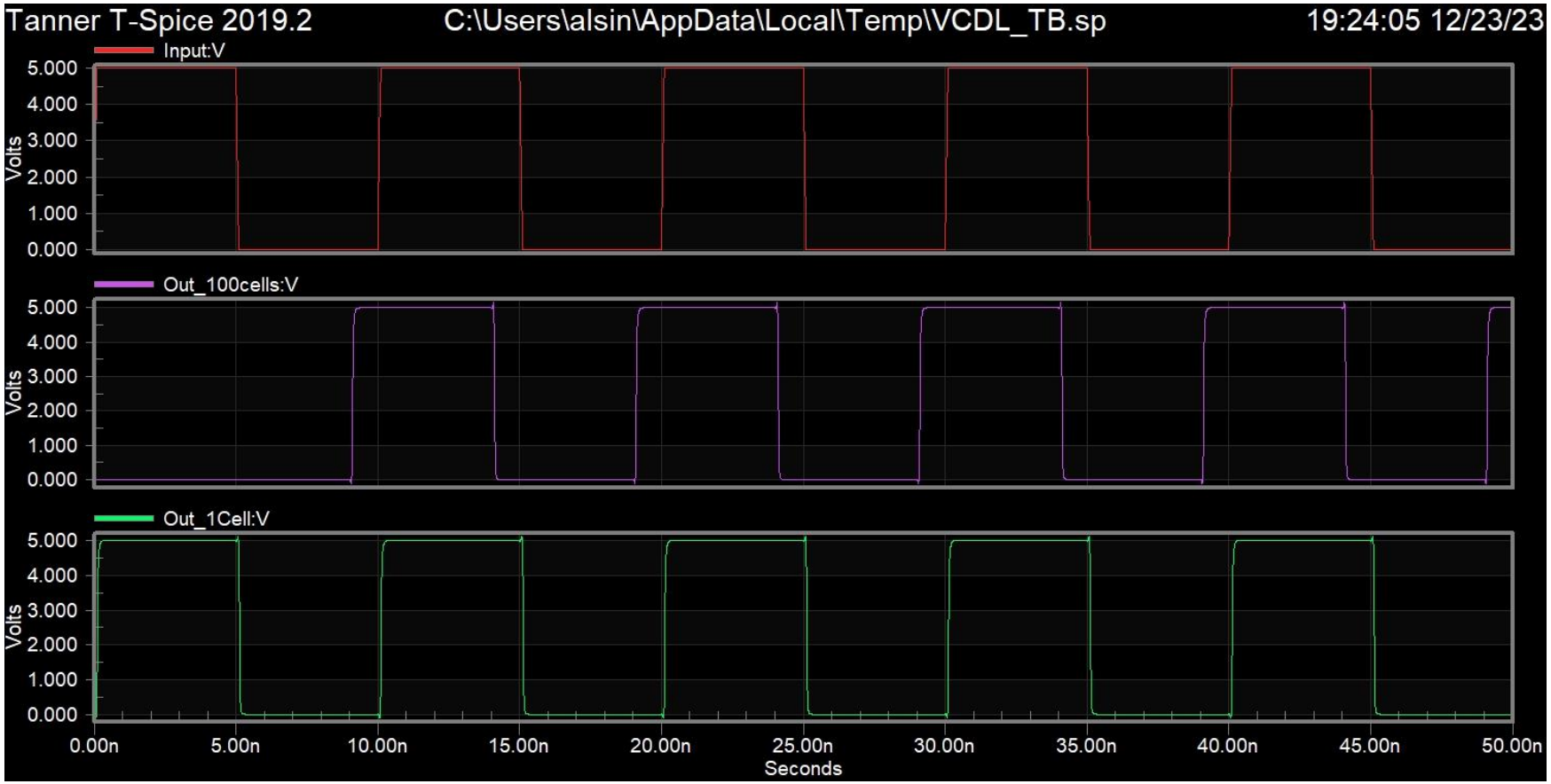
100 Cells Symbol:



Test Bench Schematic:

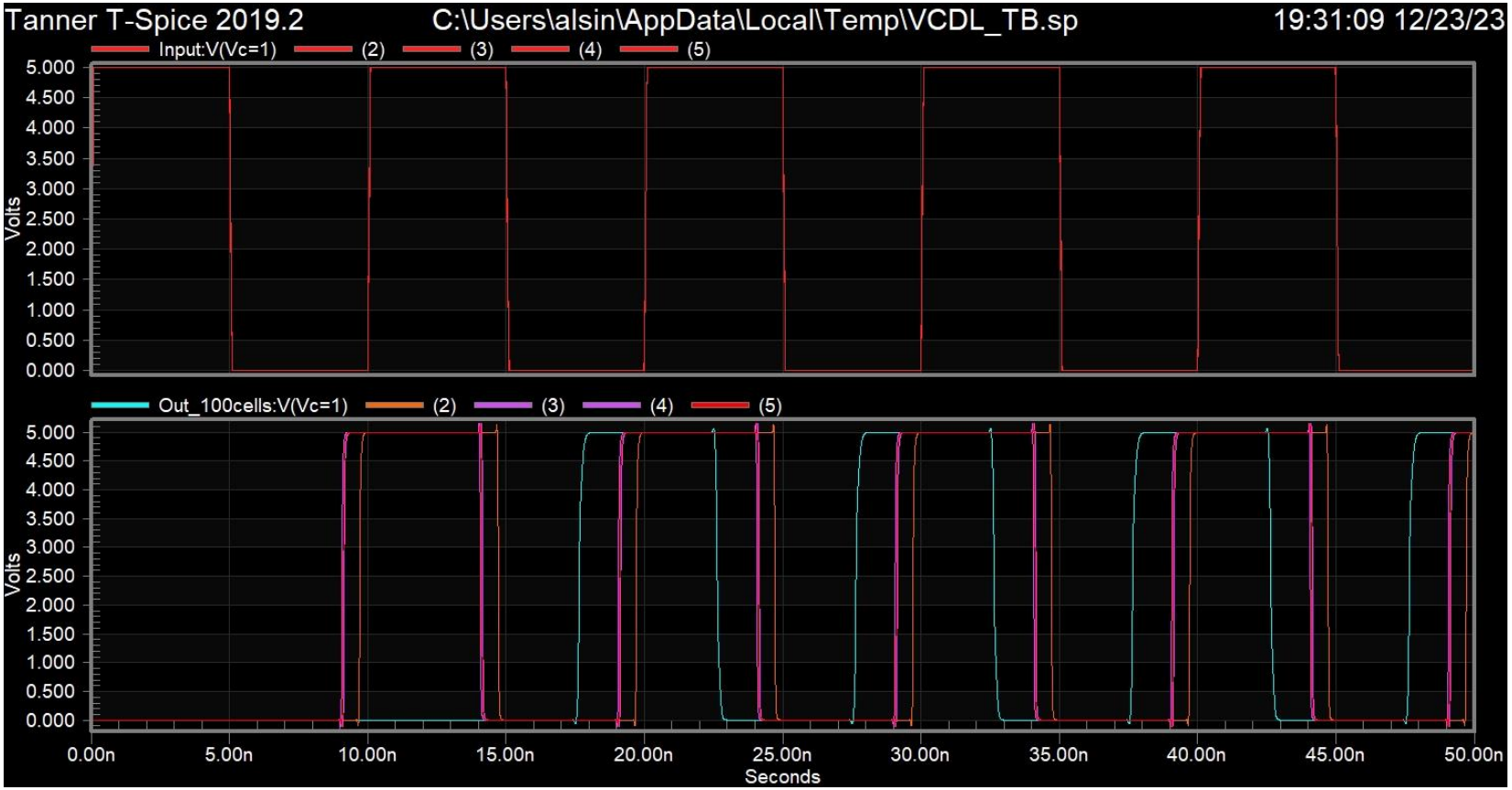


Voltage Controlled Delay Line Testing

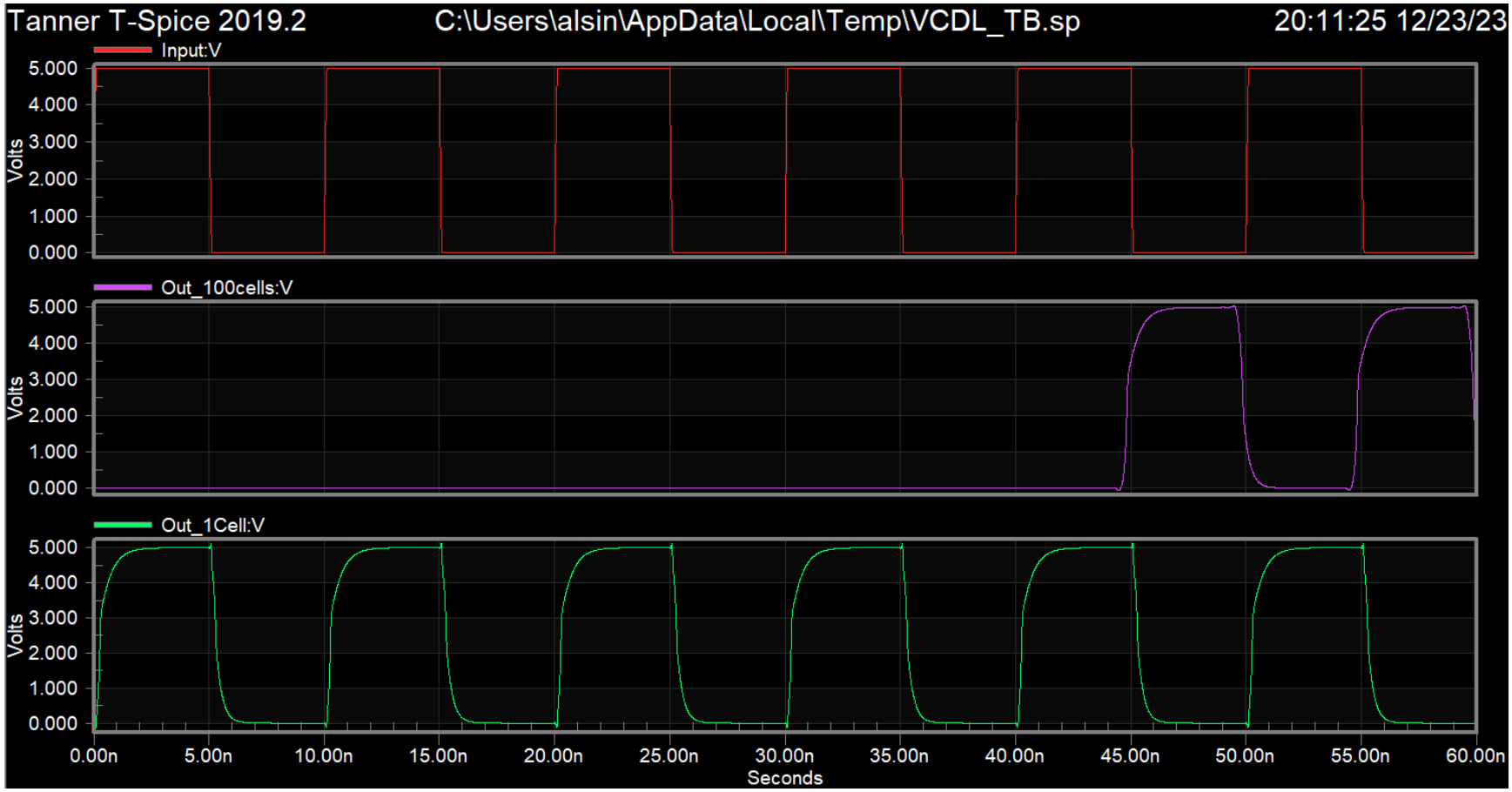


Input Frequency: 100MHz

VCDL Transient Analysis for different Control Voltages

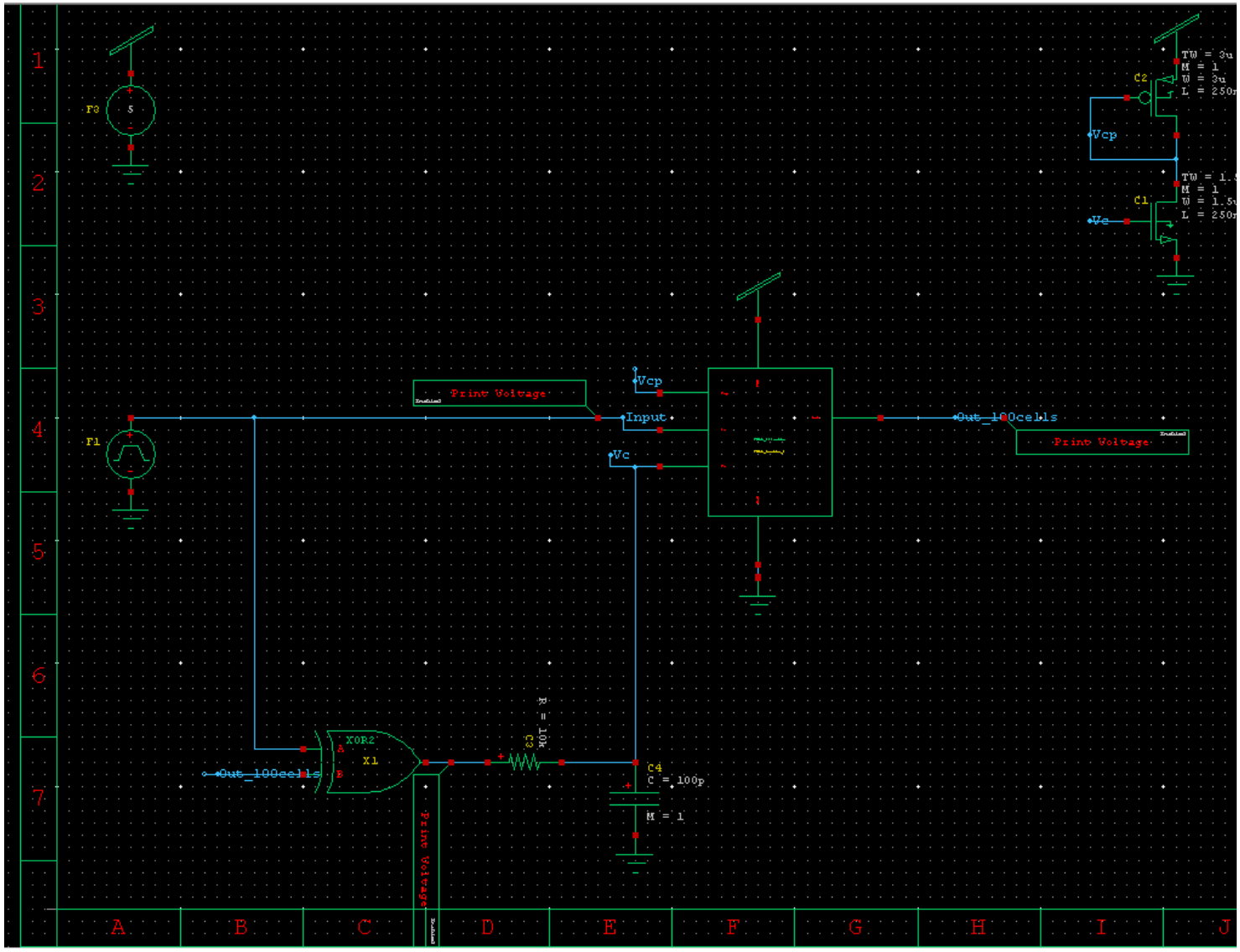


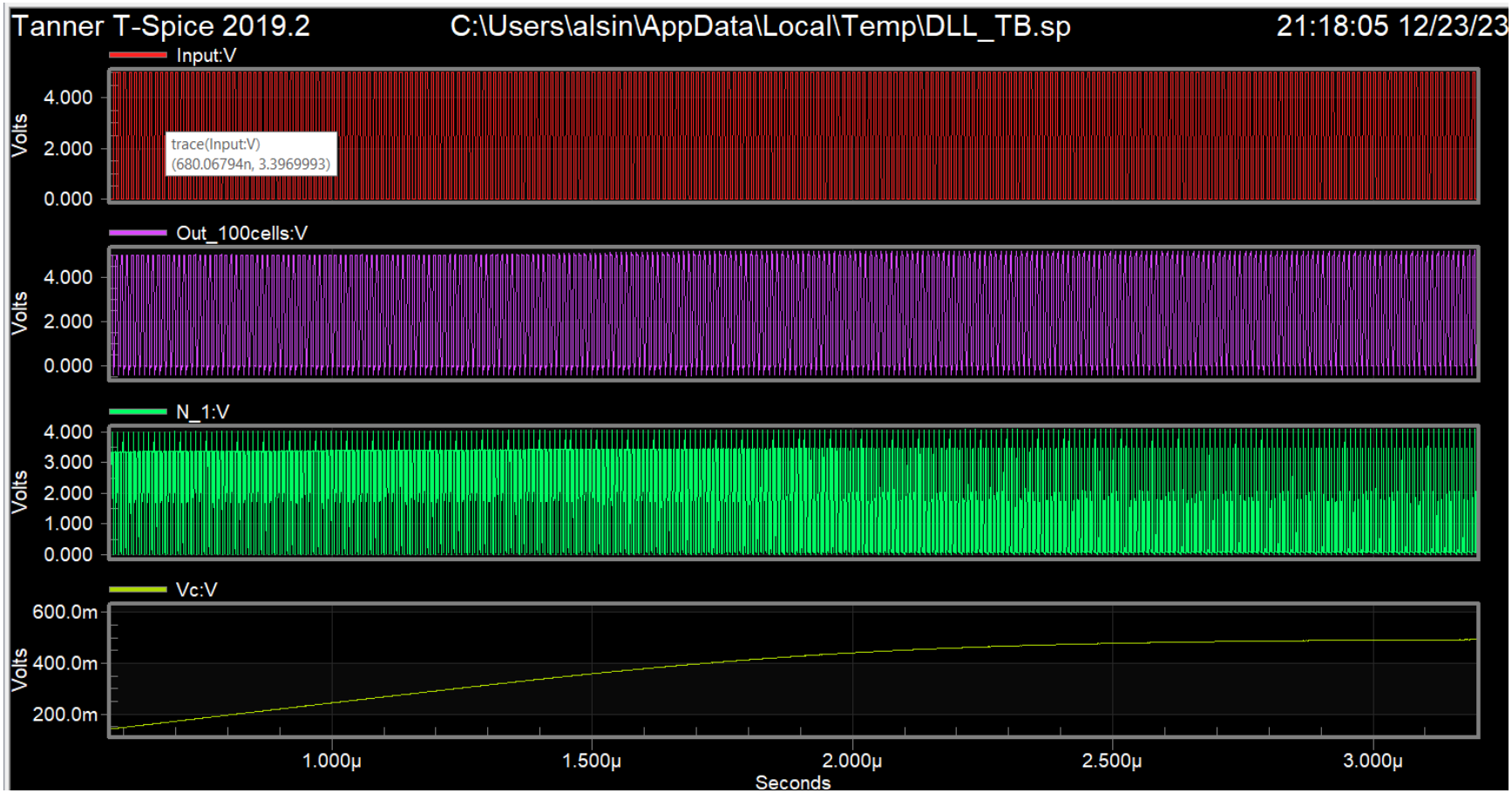
Maximum Delay for 1V, and Minimum Delay For 5V



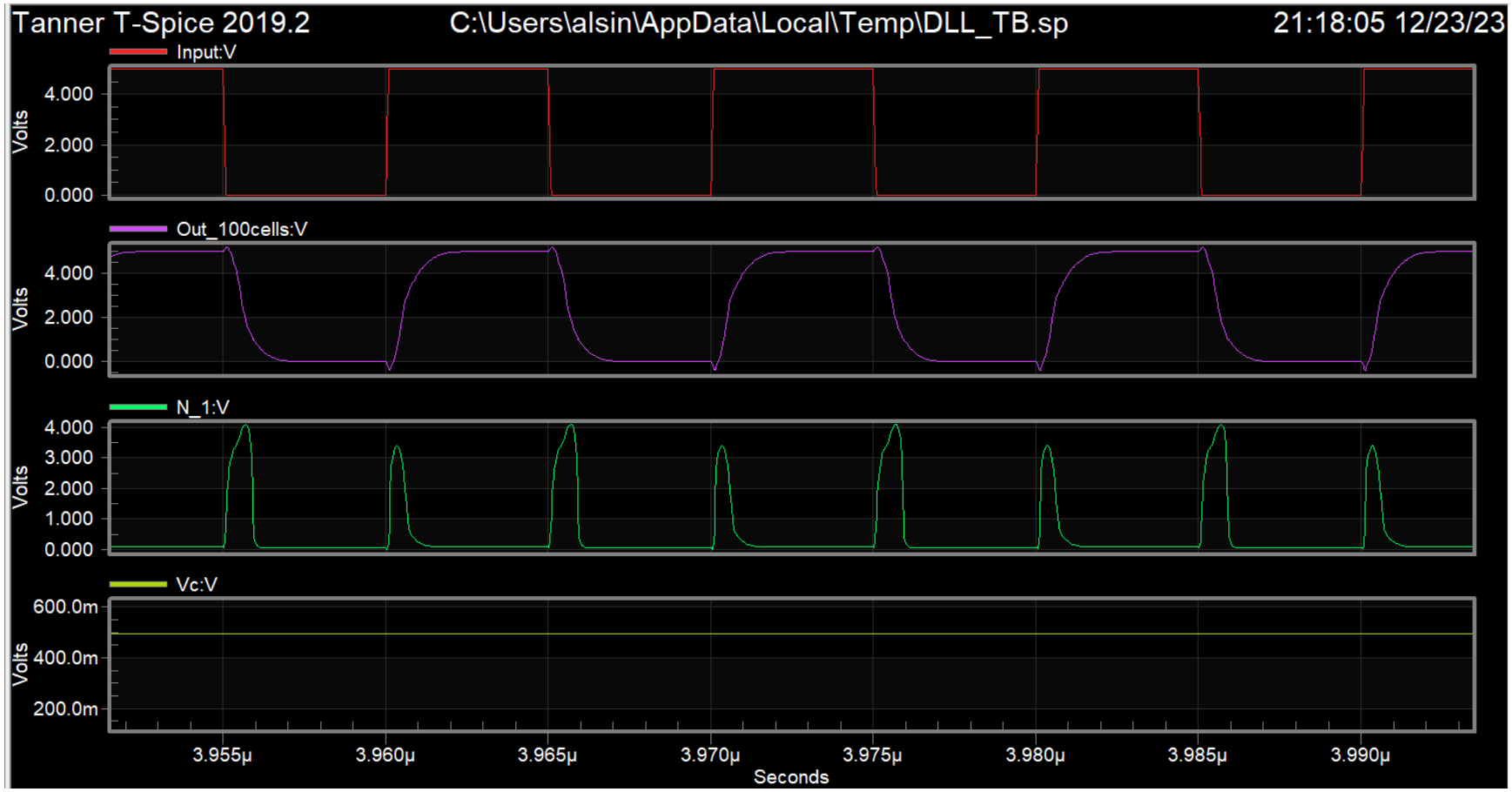
4.5 Delay Periods for Vc = 0V, for 100 Cells Delay Line

DLL Schematic

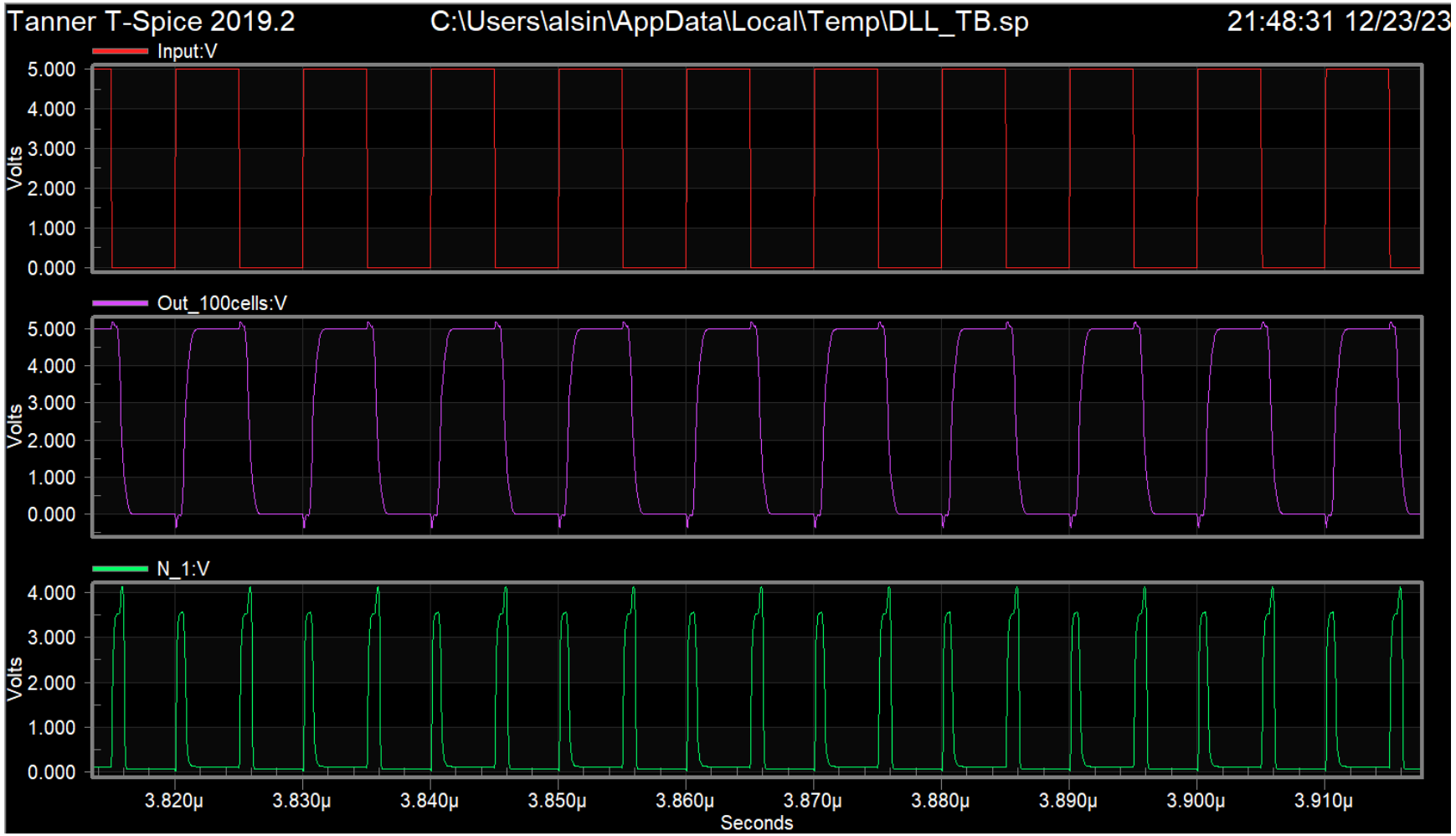




Lock condition occurs with control volt = 500mV



Using 75 Delay Cells



Lock Condition for 100 Cells used