**Introduction to Silicon Process and VLSI**

CND121

Project #4

Delay Locked Loop (DLL)

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**Introduction**

Delay-locked loops (DLLs) can be considered as feedback circuits that phase lock an output to an input without the use of an oscillator. In some applications, DLLs are necessary or preferable over phase-locked loops (PLLs), with their advantages including lower sensitivity to supply noise and lower phase noise. This article deals with fundamental DLL design concepts.

The origins of DLLs can be traced to a paper published in 1961. The authors present the topology shown in Figure 1 as a “delay-lock discriminator” operating on random signals. The feedback loop consists of a controlled delay line, a multiplier acting as a phase detector (PD), and a lowpass filter. The use of DLLs in modern CMOS design evidently began with the work by Bazes in 1985 and Johnson and Hudson in 1988.

A diagram of a circuit

Description automatically generated

Main Cell Schematic

A computer screen shot of a computer

Description automatically generated

1 Cell Symbol

A screen shot of a computer screen

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5 Cells Schematic:

A computer screen shot of a diagram

Description automatically generated

5 Cells Symbol

A screenshot of a computer

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25 Cells Schematic:

A screenshot of a computer screen

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A screenshot of a computer screen

Description automatically generated

25 Cells Symbol:

100 Cells Schematic:

A screenshot of a computer screen

Description automatically generated

A screen shot of a computer screen

Description automatically generated100 Cells Symbol:

Test Bench Schematic:

A computer screen shot of a computer screen

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Voltage Controlled Delay Line Testing

A screen shot of a graph

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Input Frequency: 100MHz

VCDL Transient Analysis for different Control Voltages

A screen shot of a graph

Description automatically generated

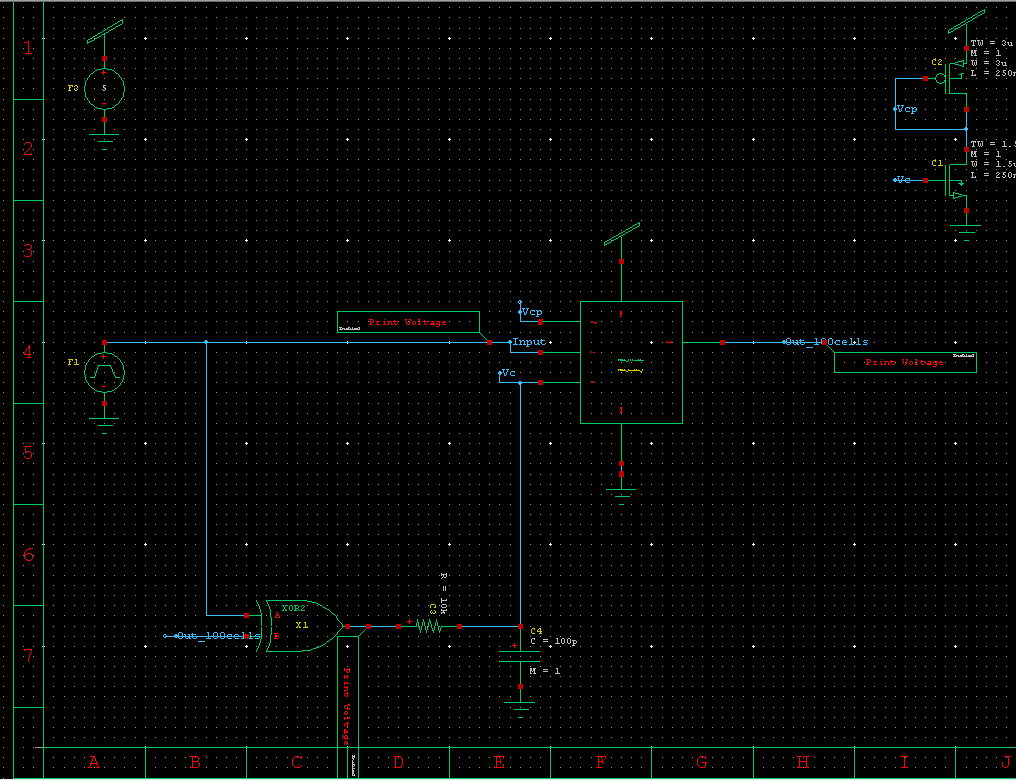
Maximum Delay for 1V, and Minimum Delay For 5V

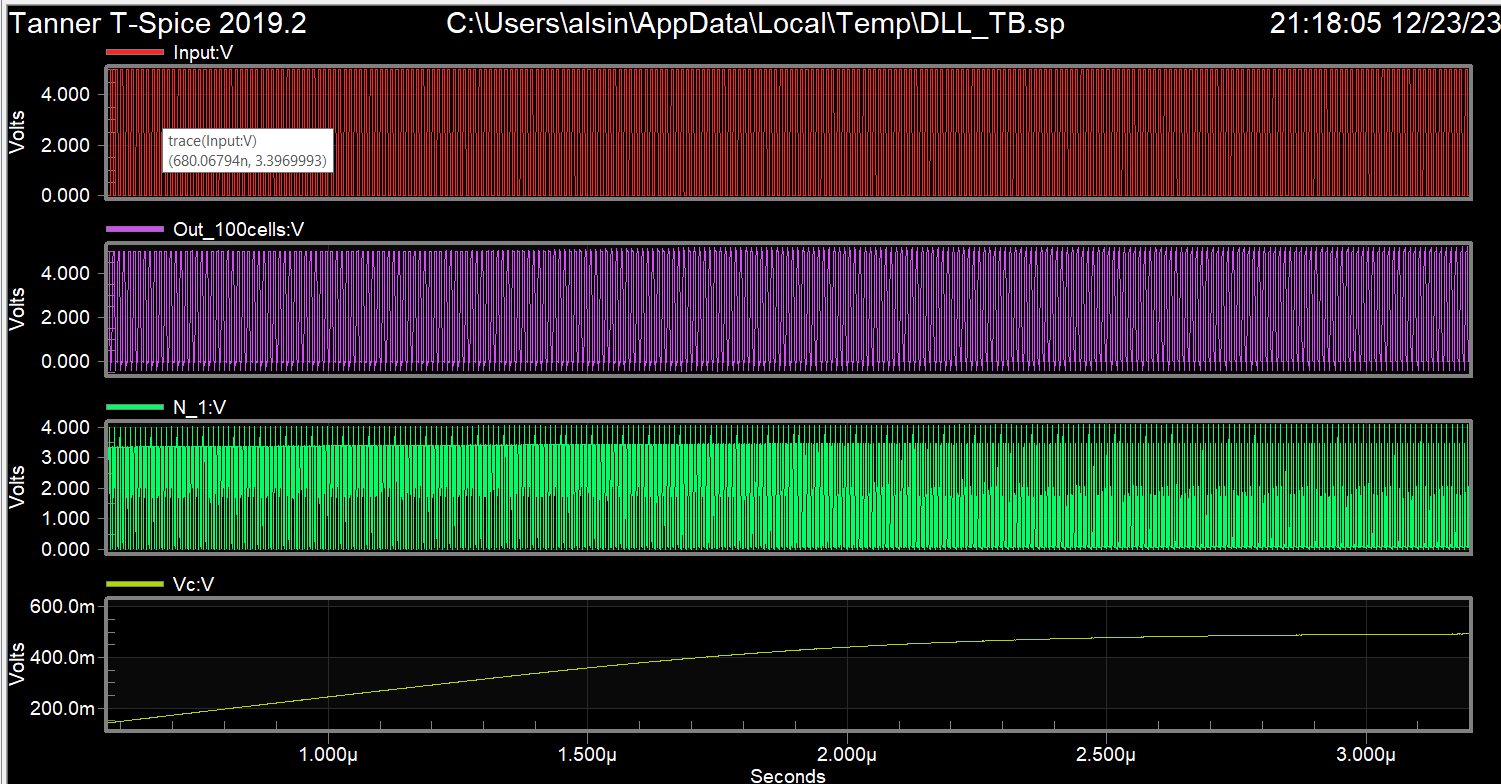
A screenshot of a computer

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4.5 Delay Periods for Vc = 0V, for 100 Cells Delay Line

DLL Schematic





Lock condition occurs with control volt = 500mV

A screenshot of a computer screen

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Using 75 Delay Cells

A screenshot of a computer screen

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Lock Condition for 100 Cells used