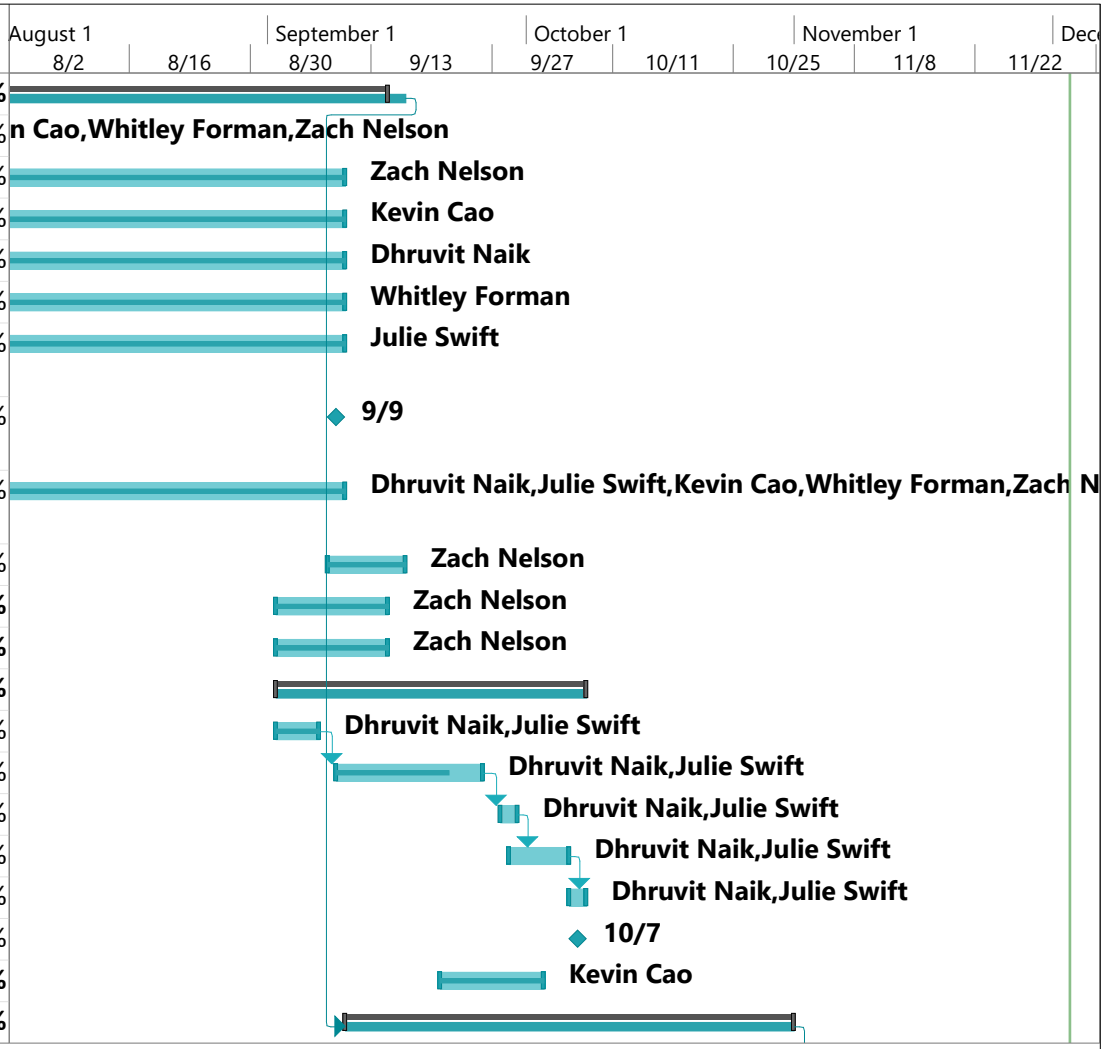
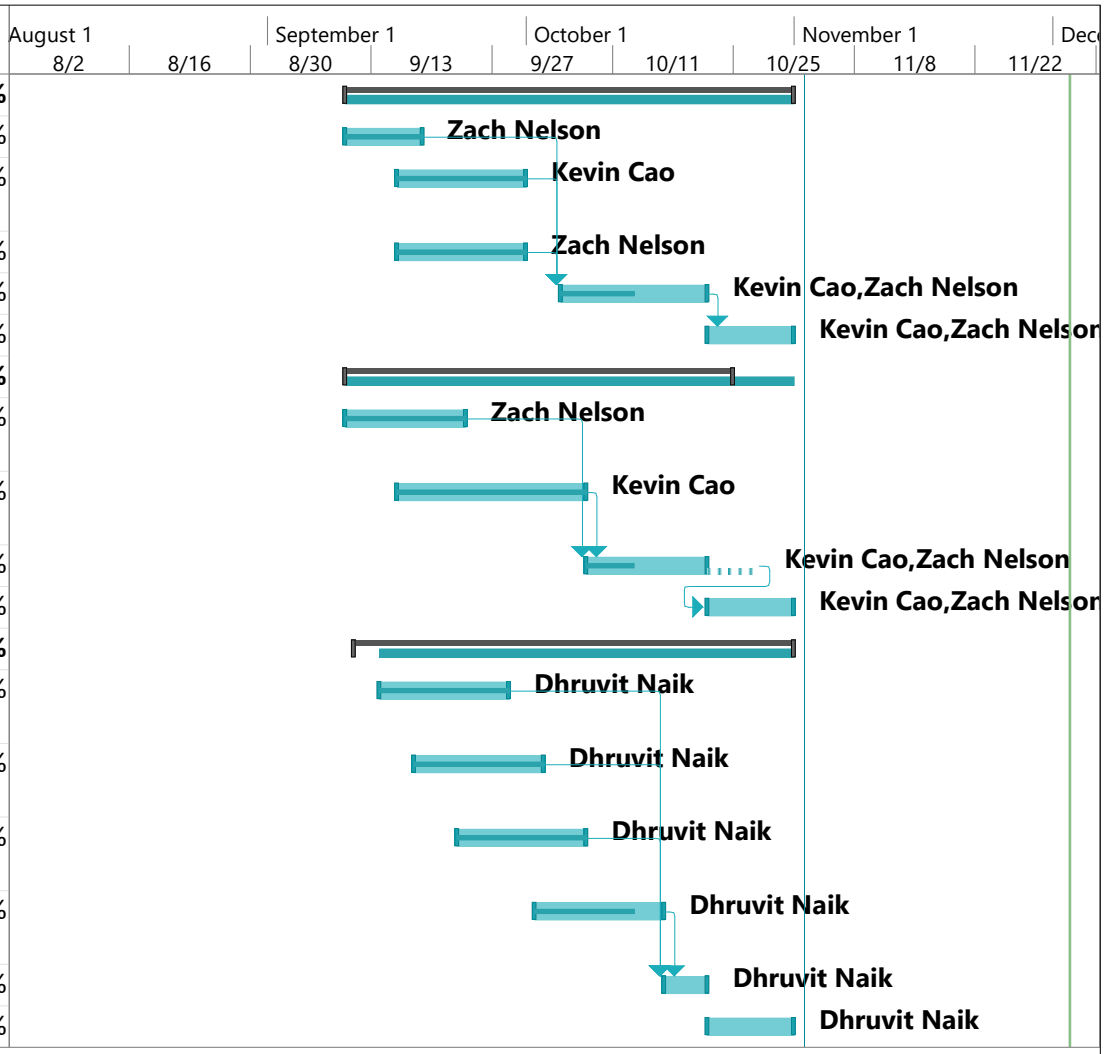
ID	Task Name	% Complete
1	**System Design**	**100%**
2	General Planning	100%
3	Complete I2S In Document	100%
4	Complete I2S Out Document	100%
5	Complete Filter Document	100%
6	Complete I2C Document	100%
7	Complete Register Document	100%
8	Finish System Design	100%
9	Document System in CORE	100%
10	RTS/RTR and XFC Protocols	100%
11	**Create a Detailed Schedule**	**100%**
12	**Install Microsoft Project**	**100%**
13	**Install EDA Tools**	**50%**
14	Determine EDA Requriments	100%
15	Install OS	69%
16	Install EDA Tool	0%
17	Create a Simple Test Case	0%
18	Place and Route Test	0%
19	Finish EDA Installation	0%
20	**Create Web Page**	**100%**
21	**RTL Design and Testing**	**70%**



Project: Chip Design.mpp
Date: Thu 12/3/15

Task	Inactive Summary	External Tasks
Split	Manual Task	External Milestone
Milestone	Duration-only	Deadline
Summary	Manual Summary Rollup	Progress
Project Summary	Manual Summary	Manual Progress
Inactive Task	Start-only	
Inactive Milestone	Finish-only	

ID	Task Name	% Complete
22	**Create i2si.v**	**71%**
23	Create and Test i2si_fifo.v	100%
24	Create and Test i2si_deserializer.v	100%
25	Create and Test i2si_bist.v	100%
26	Create i2si.v Top-Level	50%
27	Test i2si.v	0%
28	**Create i2so.v**	**67%**
29	Create and Test i2so_fifo.v	100%
30	Create and Test i2so_serializer.v	100%
31	Create i2so.v Top-Level	35%
32	Test i2so.v	0%
33	**Create filter.v**	**72%**
34	Create and Test filter_convolution.v	100%
35	Create and Test filter_accumulator.v	100%
36	Create and Test filter_fifo.v	100%
37	Create and Test filter_round_shift_clip.v	68%
38	Create filter.v Top-Level	0%
39	Test filter.v	0%



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Milestone	Duration-only	Deadline
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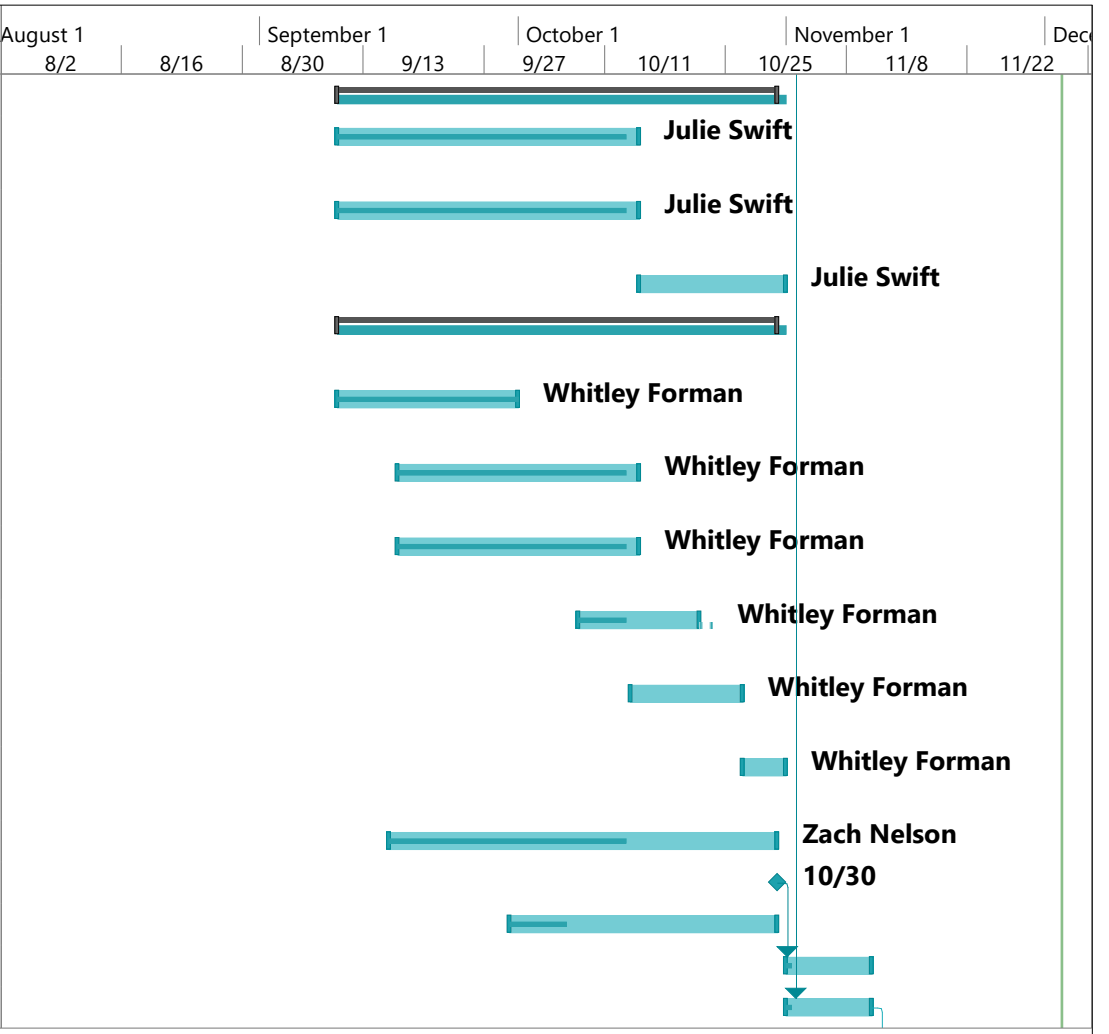
Project Summary	Manual Summary	Manual Progress
Inactive Task	Start-only	
Inactive Milestone	Finish-only	

ID	Task Name	% Complete
40	**Create register.v**	**75%**
41	Create and Test register_trig_gen.v	94%
42	Create register.v Top-Level	94%
43	Test register.v	0%
44	**Create i2c_slave.v**	**70%**
45	Create and Test i2c_slave_deserializer.v	100%
46	Create and Test i2c_slave_sequencer.v	93%
47	Create and Test i2c_slave_writetoreg.v	93%
48	Create and Test i2c_slave_serializer.v	35%
49	Create i2c_slave.v Top Level	0%
50	Test i2c_slave.v	0%
51	**Create chip.v**	59%
52	**Finish RTL Design**	0%
53	**Create Text Fixtures**	**20%**
54	**Integration Testing**	**10%**
55	**Logic Synthesis**	**10%**



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Milestone	Duration-only	Deadline
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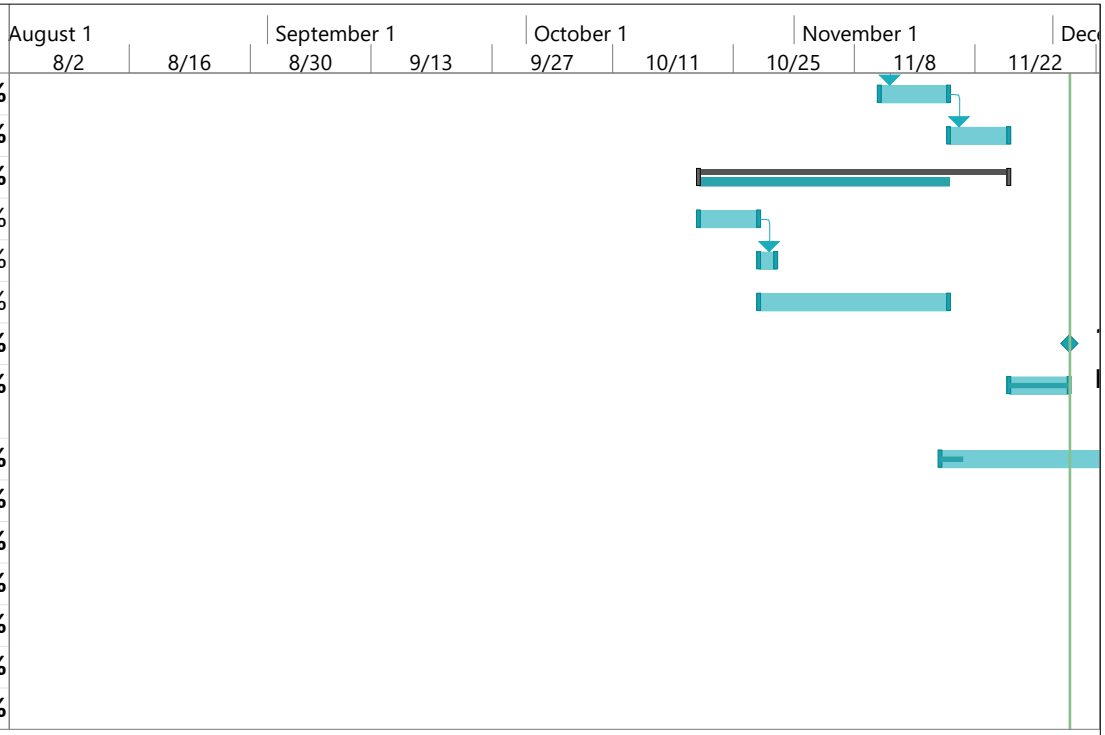
Project Summary	Manual Summary	Manual Progress
Inactive Task	Start-only	
Inactive Milestone	Finish-only	

ID	Task Name	% Complete
56	**Floor Planning**	**0%**
57	**Place and Route Gates**	**0%**
58	**Board Design**	**0%**
59	Research FPGA's	0%
60	Purchase FPGA	0%
61	Write Microcontroller Code	0%
62	**Have a Functional FPGA**	**0%**
63	**Write Final Report and Presentation**	**100%**
64	**PSoC for I2S Stream**	**5%**
65	**Verification**	**0%**
66	**Prepare for Fabrication**	**0%**
67	**MOSIS Fabrication Deadline**	**0%**
68	**Additional FPGA Testing**	**0%**
69	**Final Documentation**	**0%**
70	**Final Presentation and Report II**	**0%**



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