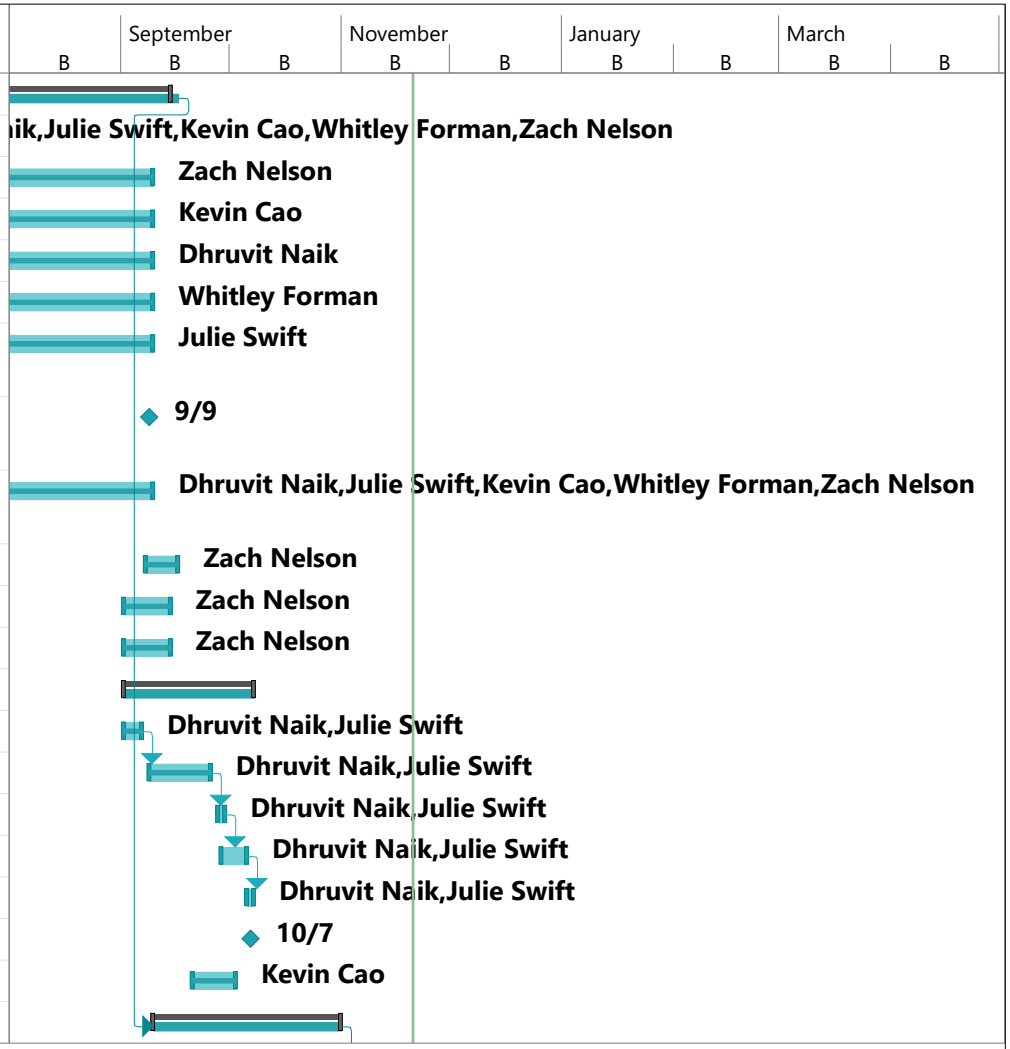
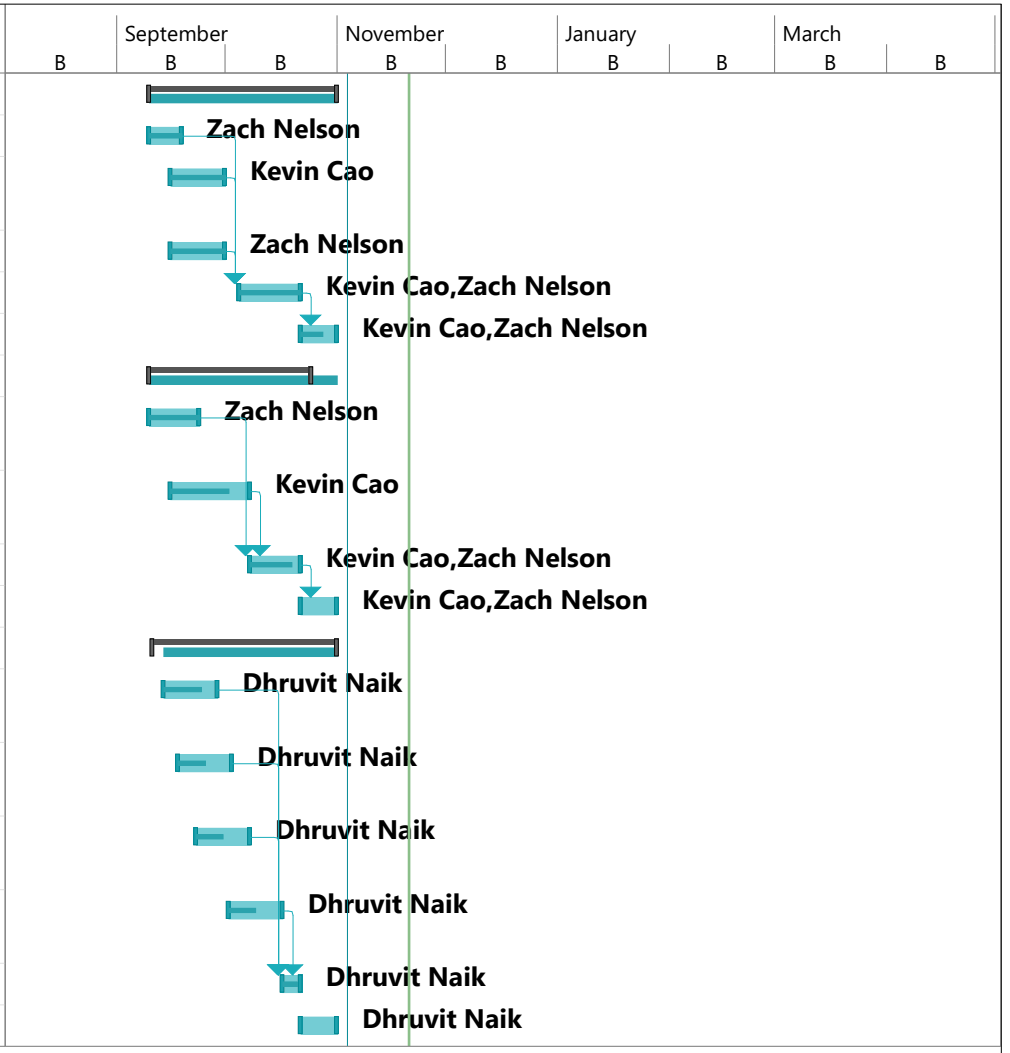
ID	Task Name	Finish	Duration
1	**System Design**	**Mon 9/14/15**	**88 days**
2	General Planning	Thu 6/18/15	26 days
3	Complete I2S In Document	Wed 9/9/15	60 days
4	Complete I2S Out Document	Wed 9/9/15	44 days
5	Complete Filter Document	Wed 9/9/15	60 days
6	Complete I2C Document	Wed 9/9/15	60 days
7	Complete Register Document	Wed 9/9/15	60 days
8	Finish System Design	Wed 9/9/15	0 days
9	Document System in CORE	Wed 9/9/15	60 days
10	RTS/RTR and XFC Protocols	Wed 9/16/15	7 days
11	**Create a Detailed Schedule**	**Mon 9/14/15**	**9 days**
12	**Install Microsoft Project**	**Mon 9/14/15**	**9 days**
13	**Install EDA Tools**	**Wed 10/7/15**	**26 days**
14	Determine EDA Requriments	Sun 9/6/15	4 days
15	Install OS	Fri 9/25/15	13 days
16	Install EDA Tool	Tue 9/29/15	2 days
17	Create a Simple Test Case	Mon 10/5/15	5 days
18	Place and Route Test	Wed 10/7/15	2 days
19	Finish EDA Installation	Wed 10/7/15	0 days
20	**Create Web Page**	**Fri 10/2/15**	**10 days**
21	**RTL Design and Testing**	**Sat 10/31/15**	**38 days**



Project: Chip Design.mpp
Date: Sat 11/21/15

Task	Inactive Summary	External Tasks
Split	Manual Task	External Milestone
Milestone	Duration-only	Deadline
Summary	Manual Summary Rollup	Progress
Project Summary	Manual Summary	Manual Progress
Inactive Task	Start-only	
Inactive Milestone	Finish-only	

ID	Task Name	Finish	Duration
22	**Create i2si.v**	**Sat 10/31/15**	**38 days**
23	Create and Test i2si_fifo.v	Fri 9/18/15	7 days
24	Create and Test i2si_deserializer.v	Wed 9/30/15	11 days
25	Create and Test i2si_bist.v	Wed 9/30/15	11 days
26	Create i2si.v Top-Level	Wed 10/21/15	13 days
27	Test i2si.v	Sat 10/31/15	8 days
28	**Create i2so.v**	**Sat 10/24/15**	**33 days**
29	Create and Test i2so_fifo.v	Wed 9/23/15	10 days
30	Create and Test i2so_serializer.v	Wed 10/7/15	16 days
31	Create i2so.v Top-Level	Wed 10/21/15	10 days
32	Test i2so.v	Sat 10/31/15	8 days
33	**Create filter.v**	**Sat 10/31/15**	**37 days**
34	Create and Test filter_convolution.v	Mon 9/28/15	11 days
35	Create and Test filter_accumulator.v	Fri 10/2/15	11 days
36	Create and Test filter_fifo.v	Wed 10/7/15	11 days
37	Create and Test filter_round_shift_clip.v	Fri 10/16/15	11 days
38	Create filter.v Top-Level	Wed 10/21/15	4 days
39	Test filter.v	Sat 10/31/15	8 days



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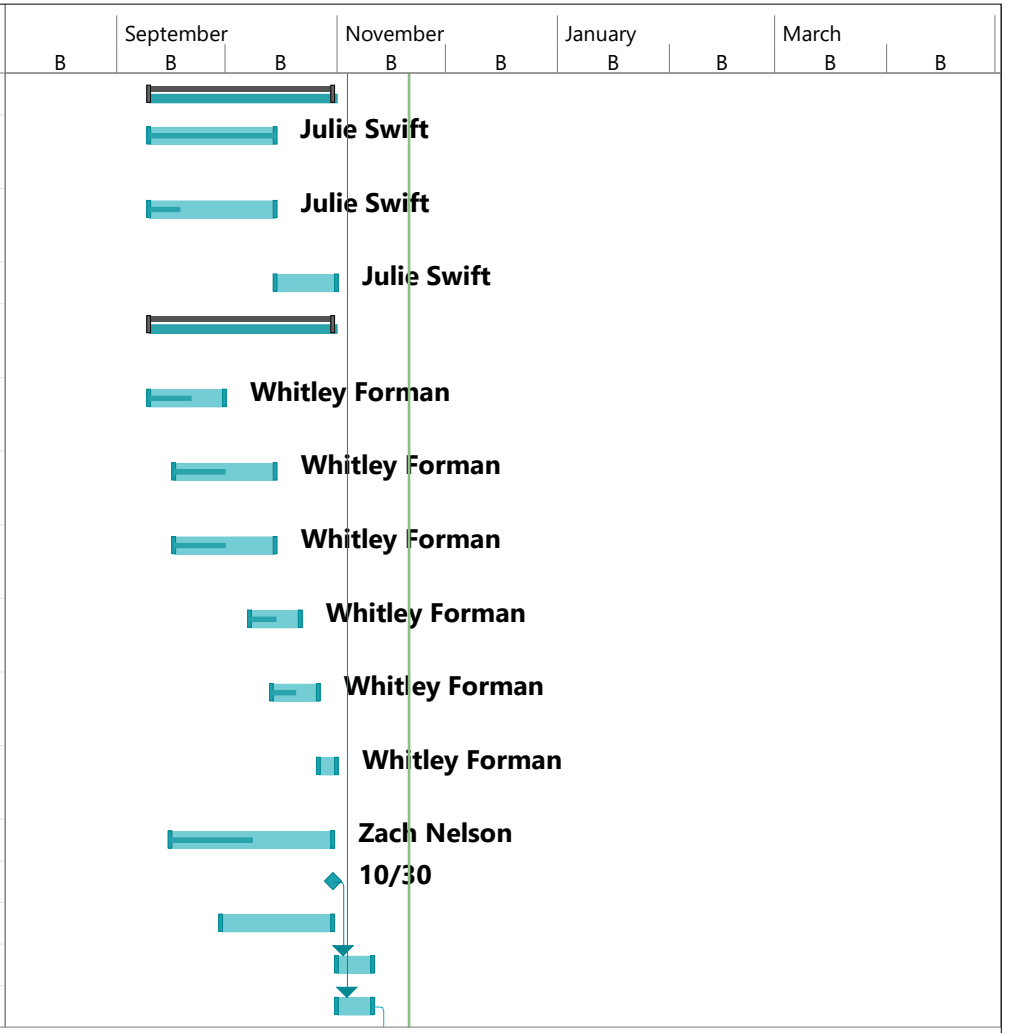
ID	Task Name	Finish	Duration
40	**Create register.v**	**Fri 10/30/15**	**37 days**
41	Create and Test register_trig_gen.v	Wed 10/14/15	25 days
42	Create register.v Top-Level	Wed 10/14/15	25 days
43	Test register.v	Sat 10/31/15	13 days
44	**Create i2c_slave.v**	**Fri 10/30/15**	**37 days**
45	Create and Test i2c_slave_deserializer.v	Wed 9/30/15	15 days
46	Create and Test i2c_slave_sequencer.v	Wed 10/14/15	20 days
47	Create and Test i2c_slave_writetoreg.v	Wed 10/14/15	20 days
48	Create and Test i2c_slave_serializer.v	Wed 10/21/15	10 days
49	Create i2c_slave.v Top Level	Mon 10/26/15	9 days
50	Test i2c_slave.v	Sat 10/31/15	5 days
51	**Create chip.v**	**Fri 10/30/15**	**33 days**
52	**Finish RTL Design**	**Fri 10/30/15**	**0 days**
53	**Create Text Fixtures**	**Fri 10/30/15**	**23 days**
54	**Integration Testing**	**Tue 11/10/15**	**8 days**
55	**Logic Synthesis**	**Tue 11/10/15**	**8 days**



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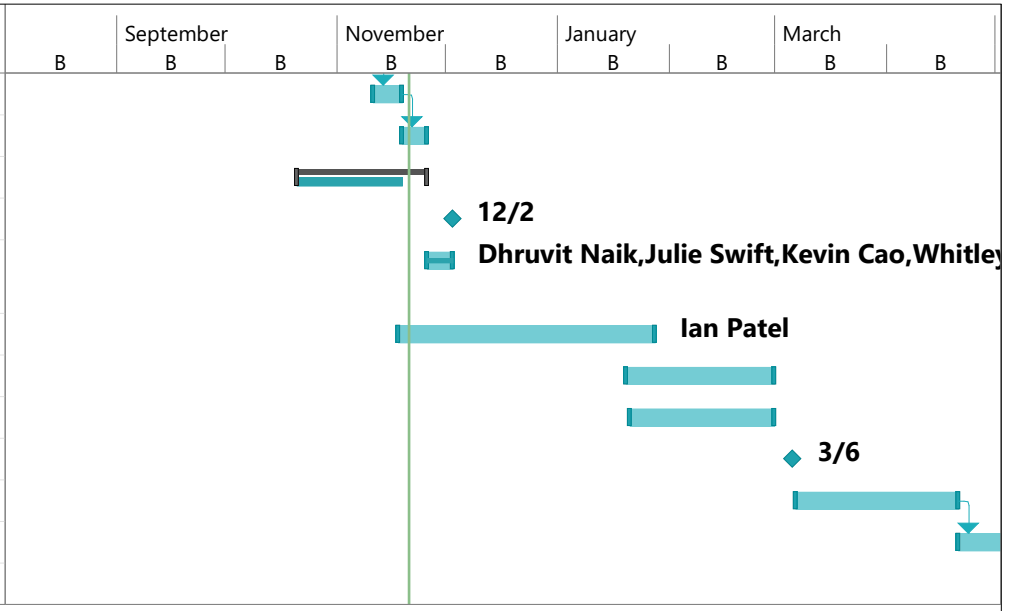
Inactive Milestone	Finish-only	

ID		Task Name	Finish	Duration
56		**Floor Planning**	**Wed 11/18/15**	**6 days**
57		**Place and Route Gates**	**Wed 11/25/15**	**5 days**
58		**Board Design**	**Wed 11/25/15**	**26 days**
62		**Have a Functional FPGA**	**Wed 12/2/15**	**0 days**
63	✓	**Write Final Report and Presentation**	**Wed 12/2/15**	**5 days**
64		**PSoC for I2S Stream**	**Wed 1/27/16**	**51 days**
65		**Verification**	**Mon 2/29/16**	**29 days**
66		**Prepare for Fabrication**	**Mon 2/29/16**	28 days
67		**MOSIS Fabrication Deadline**	**Sun 3/6/16**	**0 days**
68		**Additional FPGA Testing**	**Wed 4/20/16**	33 days
69		**Final Documentation**	**Tue 5/3/16**	9 days
70		**Final Presentation and Report II**	**Wed 5/4/16**	0 days



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