Chip Design Process Rough Outline

Orange = Whitley
Blue = Zach
Magenta = Kevin
Green = Dhruvit
Red = Julie
Black = Everybody

1. Requirements - Word
2. Architecture - Word / Visio
3. Verification
    - Write test plan (Word)
    - Develop RTL Test Environment (Verilog, C++)
    - Test Software (C++)
    - Test Vectors
    - Run and Debug RTL Tests
4. Install EDA (Electronic Design Automation) Tools (IT/students)
5. Design and Code RTL for Blocks
    - I^2C Slave Device (communication between system. Give us an address and write/read data
    - Register Set
    - I^2S Input Interfaces (streaming audio interfaces)
    - Core Functional Unit
6. Test Insertion (scan chain) (either replace DFF with scan flops, and add scan chain in gates, or modify RTL)
7. Logic Synthesis (to standard cell library) (either 180 or 500 nm library)
    - static timing analysis
8. Gate Level Simulation
    - Check for Clock Domain Crossing issues
    - Check for X propagation
9. Place and Route Gates
    - Post route timing (Static Timing Analysis)
10. Board Design
    - Hardware Test Fixture
    - microcontroller code written to
        - functional test
        - register test

Some other miscellaneous issues:

- PAD Design
- Chip Stuff (e.g. bond wires between package and IC)