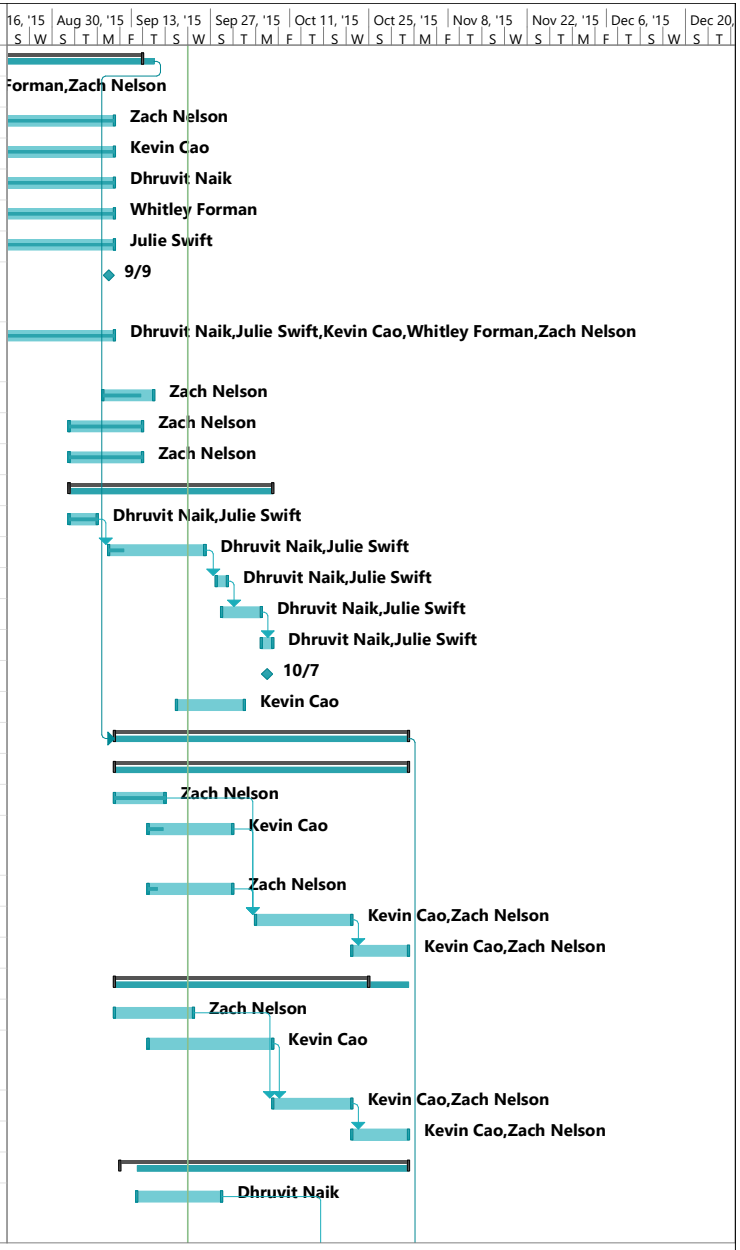
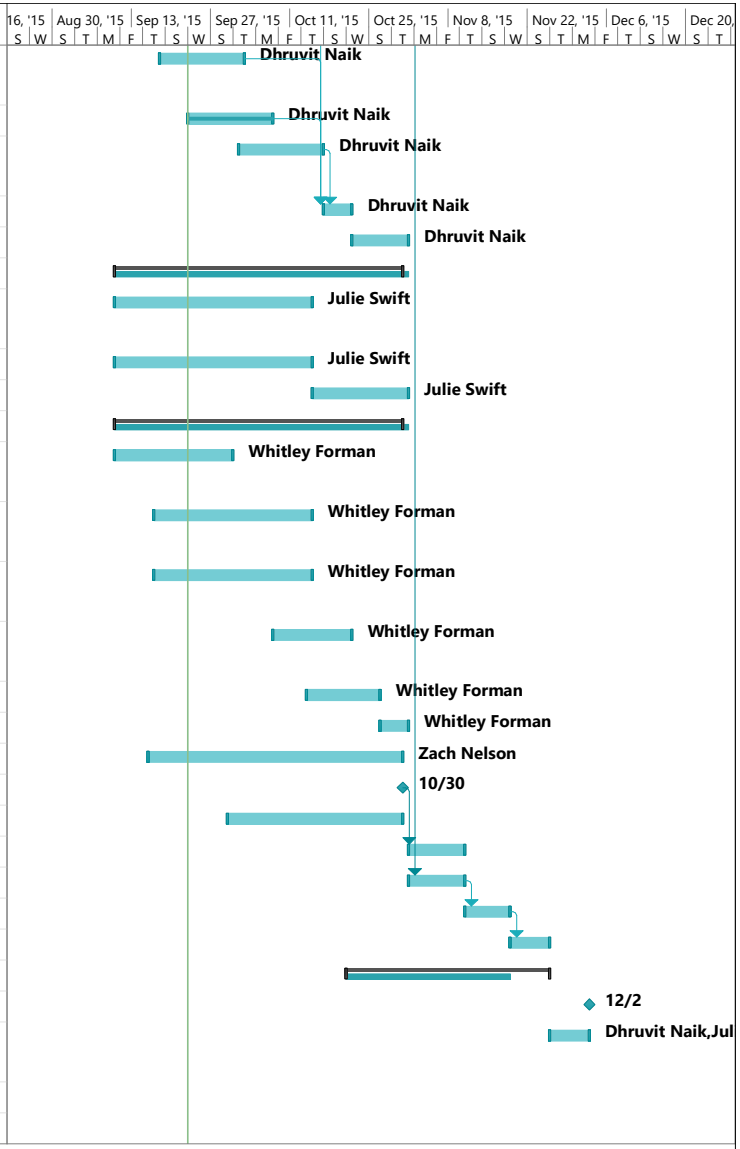
ID	Task Mode	Task Name	Duration	Start	Finish	Resource Names	Predecessors
1		**System Design**	**88 days**	**Thu 5/14/15**	**Mon 9/14/15**	**Dhruvit Naik,Julie Swift,Kevi**	
2		General Planning	26 days	Thu 5/14/15	Thu 6/18/15	Dhruvit Naik,Julie Swift,Kevir	
3		Complete I2S In Document	60 days	Thu 6/18/15	Wed 9/9/15	Zach Nelson	
4		Complete I2S Out Document	44 days	Sat 7/11/15	Wed 9/9/15	Kevin Cao	
5		Complete Filter Document	60 days	Thu 6/18/15	Wed 9/9/15	Dhruvit Naik	
6		Complete I2C Document	60 days	Thu 6/18/15	Wed 9/9/15	Whitley Forman	
7		Complete Register Document	60 days	Thu 6/18/15	Wed 9/9/15	Julie Swift	
8		Finish System Design	0 days	Wed 9/9/15	Wed 9/9/15	Dhruvit Naik,Julie Swift,Kevin Cao,Whitley	
9		Document System in CORE	60 days	Thu 6/18/15	Wed 9/9/15	Dhruvit Naik,Julie Swift,Kevin Cao,Whitley	
10		RTS/RTR and XFC Protocols	7 days	Tue 9/8/15	Wed 9/16/15	Zach Nelson	
11		**Create a Detailed Schedule**	**9 days**	**Wed 9/2/15**	**Mon 9/14/15**	**Zach Nelson**	
12		**Install Microsoft Project**	**9 days**	**Wed 9/2/15**	**Mon 9/14/15**	**Zach Nelson**	
13		**Install EDA Tools**	**26 days**	**Wed 9/2/15**	**Wed 10/7/15**	**Dhruvit Naik,Julie Swift**	
14		Determine EDA Requriments	4 days	Wed 9/2/15	Sun 9/6/15	Dhruvit Naik,Julie Swift	
15		Install OS	13 days	Wed 9/9/15	Fri 9/25/15	Dhruvit Naik,Julie Swift	14
16		Install EDA Tool	2 days	Mon 9/28/15	Tue 9/29/15	Dhruvit Naik,Julie Swift	15
17		Create a Simple Test Case	5 days	Tue 9/29/15	Mon 10/5/15	Dhruvit Naik,Julie Swift	16
18		Place and Route Test	2 days	Tue 10/6/15	Wed 10/7/15	Dhruvit Naik,Julie Swift	17
19		Finish EDA Installation	0 days	Wed 10/7/15	Wed 10/7/15	Dhruvit Naik,Julie Swift	
20		**Create Web Page**	**10 days**	**Mon 9/21/15**	**Fri 10/2/15**	**Kevin Cao**	
21		**RTL Design and Testing**	**38 days**	**Thu 9/10/15**	**Sat 10/31/15**	**Dhruvit Naik,Julie Swift,Kevi**	**1**
22		**Create i2si.v**	**38 days**	**Thu 9/10/15**	**Sat 10/31/15**	**Kevin Cao,Zach Nelson**	
23		Create and Test i2si_fifo.v	7 days	Thu 9/10/15	Fri 9/18/15	Zach Nelson	
24		Create and Test i2si_deserializer.v	11 days	Wed 9/16/15	Wed 9/30/15	Kevin Cao	
25		Create and Test i2si_bist.v	11 days	Wed 9/16/15	Wed 9/30/15	Zach Nelson	
26		Create i2si.v Top-Level	13 days	Mon 10/5/15	Wed 10/21/15	Kevin Cao,Zach Nelson	23,24,25
27		Test i2si.v	8 days	Thu 10/22/15	Sat 10/31/15	Kevin Cao,Zach Nelson	26
28		**Create i2so.v**	**33 days**	**Thu 9/10/15**	**Sat 10/24/15**	**Kevin Cao,Zach Nelson**	
29		Create and Test i2so_fifo.v	10 days	Thu 9/10/15	Wed 9/23/15	Zach Nelson	
30		Create and Test i2so_serializer.v	16 days	Wed 9/16/15	Wed 10/7/15	Kevin Cao	
31		Create i2so.v Top-Level	10 days	Thu 10/8/15	Wed 10/21/15	Kevin Cao,Zach Nelson	29,30
32		Test i2so.v	8 days	Thu 10/22/15	Sat 10/31/15	Kevin Cao,Zach Nelson	31
33		**Create filter.v**	**37 days**	**Fri 9/11/15**	**Sat 10/31/15**	**Dhruvit Naik**	
34		Create and Test filter_convolution.v	11 days	Mon 9/14/15	Mon 9/28/15	Dhruvit Naik	



Project: Chip Design
Date: Wed 9/23/15

Task	Project Summary	Manual Task	Start-only	Deadline
Split	Inactive Task	Duration-only	Finish-only	Progress
Milestone	Inactive Milestone	Manual Summary Rollup	External Tasks	Manual Progress
Summary	Inactive Summary	Manual Summary	External Milestone	

ID	Task Mode	Task Name	Duration	Start	Finish	Resource Names	Predecessors
35		Create and Test filter_accumulator.v	11 days	Fri 9/18/15	Fri 10/2/15	Dhruvit Naik	
36		Create and Test filter_fifo.v	11 days	Wed 9/23/15	Wed 10/7/15	Dhruvit Naik	
37		Create and Test filter_round_shift_clip.v	11 days	Fri 10/2/15	Fri 10/16/15	Dhruvit Naik	
38		Create filter.v Top-Level	4 days	Sat 10/17/15	Wed 10/21/15	Dhruvit Naik	34,35,36,37
39		Test filter.v	8 days	Thu 10/22/15	Sat 10/31/15	Dhruvit Naik	
40		**Create register.v**	**37 days**	**Thu 9/10/15**	**Fri 10/30/15**	**Julie Swift**	
41		Create and Test register_trig_gen.v	25 days	Thu 9/10/15	Wed 10/14/15	Julie Swift	
42		Create register.v Top-Level	25 days	Thu 9/10/15	Wed 10/14/15	Julie Swift	
43		Test register.v	13 days	Thu 10/15/15	Sat 10/31/15	Julie Swift	
44		**Create i2c_slave.v**	**37 days**	**Thu 9/10/15**	**Fri 10/30/15**	**Whitley Forman**	
45		Create and Test i2c_slave_deserializer.v	15 days	Thu 9/10/15	Wed 9/30/15	Whitley Forman	
46		Create and Test i2c_slave_sequencer.v	20 days	Thu 9/17/15	Wed 10/14/15	Whitley Forman	
47		Create and Test i2c_slave_writetoreg.v	20 days	Thu 9/17/15	Wed 10/14/15	Whitley Forman	
48		Create and Test i2c_slave_serializer.v	10 days	Thu 10/8/15	Wed 10/21/15	Whitley Forman	
49		Create i2c_slave.v Top Level	9 days	Wed 10/14/15	Mon 10/26/15	Whitley Forman	
50		Test i2c_slave.v	5 days	Tue 10/27/15	Sat 10/31/15	Whitley Forman	
51		**Create chip.v**	**33 days**	**Wed 9/16/15**	**Fri 10/30/15**	Zach Nelson	
52		**Finish RTL Design**	**0 days**	**Fri 10/30/15**	**Fri 10/30/15**	Dhruvit Naik,Julie Swift,Kevir	
53		**Create Text Fixtures**	**23 days**	**Wed 9/30/15**	**Fri 10/30/15**		
54		**Integration Testing**	**8 days**	**Sun 11/1/15**	**Tue 11/10/15**		52
55		**Logic Synthesis**	**8 days**	**Sun 11/1/15**	**Tue 11/10/15**		**21**
56		**Floor Planning**	**6 days**	**Wed 11/11/15**	**Wed 11/18/15**		**55**
57		**Place and Route Gates**	**5 days**	**Thu 11/19/15**	**Wed 11/25/15**		**56**
58		**Board Design**	**26 days**	**Wed 10/21/15**	**Wed 11/25/15**		
62		**Have a Functional FPGA**	**0 days**	**Wed 12/2/15**	**Wed 12/2/15**		
63		**Write Final Report and Presentation**	**5 days**	**Thu 11/26/15**	**Wed 12/2/15**	Dhruvit Naik,Julie Swift,Kevin Cao,Whitley Forman,Zach Nelson	
64		**Verification**	**1 day**	**Fri 5/6/16**	**Fri 5/6/16**		
65		**MOSIS Fabrication Deadline**	**0 days**	**Sun 3/6/16**	**Sun 3/6/16**	Dhruvit Naik,Julie Swift,Kevir	



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