

TPS6273x Step-Down Converter With Bypass Mode for Ultra Low-Power Wireless Applications

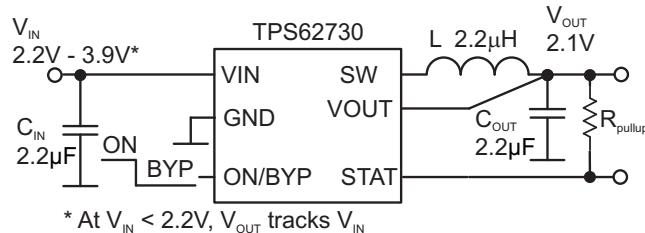
1 Features

- Input Voltage Range V_{IN} From 1.9 V to 3.9 V
- Typ. 30-nA Ultra Low-Power Bypass Mode
- Typ. 25- μ A DC-DC Quiescent Current
- Internal Feedback Divider Disconnect
- Typical 2.1- Ω Bypass Switch Between V_{IN} and V_{OUT}
- Automatic Transition from DC-DC to Bypass Mode
- Up to 3-MHz Switch Frequency
- Up to 95% DC-DC Efficiency
- Open-Drain Status Output STAT
- Output Peak Current up to 100 mA
- Fixed Output Voltages 1.9 V, 2.05 V, 2.1 V, 2.3 V
- Small External Output Filter Components 2.2 μ H and 2.2 μ F
- Optimized For Low Output Ripple Voltage
- Small $1 \times 1.5 \times 0.6\text{-mm}^3$ USON Package
- 12-mm 2 Minimum Solution Size

2 Applications

- CC2540 Bluetooth™ Low-Energy System-On-Chip Solution
- Low-Power Wireless Applications
- RF4CE, Metering

Typical Application



3 Description

The TPS62730 is a high frequency synchronous step-down DC-DC converter optimized for ultra low-power wireless applications. The device is optimized to supply TI's Low-Power Wireless sub 1-GHz and 2.4-GHz RF transceivers and System-On-Chip (SoC) solutions. The TPS62730 reduces the current consumption drawn from the battery during TX and RX mode by a high efficient step-down voltage conversion. The device provides an output current of up to 100 mA and allows the use of tiny and low-cost chip inductors and capacitors. With an input voltage range of 1.9 V to 3.9 V, the device supports Li-primary battery chemistries such as Li-SOCl₂, Li-SO₂, Li-MnO₂, and also two cell alkaline batteries.

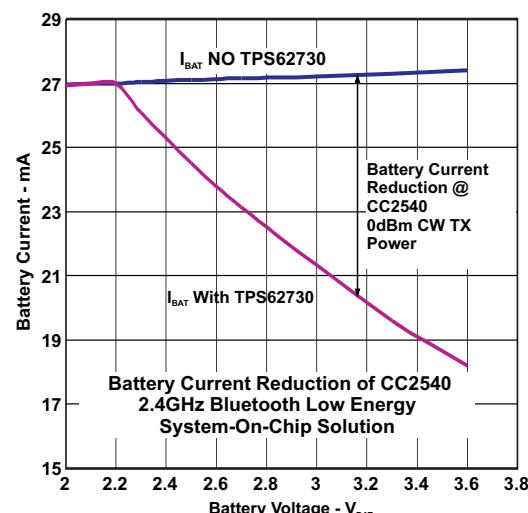
The TPS62730 features an Ultra Low-Power bypass mode with typical 30-nA current consumption to support sleep and low power modes of TI's CC2540 Bluetooth Low Energy and CC430 SoC solutions. In this bypass mode, the output capacitor of the DC-DC converter is connected through an integrated typical 2.1- Ω bypass switch to the battery.

Device Information⁽¹⁾

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS62730		
TPS62732	USON (6)	
TPS62733		1.45 mm x 1.00 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Battery Current Reduction Using TPS62730



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Table of Contents

1 Features	1	9.3 Feature Description.....	8
2 Applications	1	9.4 Device Functional Modes.....	10
3 Description	1	10 Application and Implementation.....	11
4 Revision History.....	2	10.1 Application Information.....	11
5 Description (Continued).....	3	10.2 Typical Application	11
6 Device Comparison Table.....	3	10.3 System Examples	18
7 Pin Configuration and Functions	3	11 Power Supply Recommendations	19
8 Specifications.....	4	12 Layout.....	19
8.1 Absolute Maximum Ratings	4	12.1 Layout Guidelines	19
8.2 ESD Ratings.....	4	12.2 Layout Example	19
8.3 Recommended Operating Conditions.....	4	13 Device and Documentation Support	20
8.4 Thermal Information	4	13.1 Device Support.....	20
8.5 Electrical Characteristics.....	5	13.2 Related Links	20
8.6 Typical Characteristics	7	13.3 Trademarks	20
9 Detailed Description	8	13.4 Electrostatic Discharge Caution	20
9.1 Overview	8	13.5 Glossary	20
9.2 Functional Block Diagram	8	14 Mechanical, Packaging, and Orderable Information	20

4 Revision History

Changes from Revision C (December 2012) to Revision D

Page

- Added *Pin Configuration and Functions* section, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section 1

5 Description (Continued)

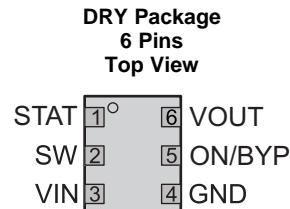
In DC-DC operation mode the device provides a fixed output voltage to the system. With a switch frequency up to 3 MHz, the TPS62730 features low output ripple voltage and low noise even with a small 2.2- μ F output capacitor. The automatic transition into bypass mode during DC-DC operation prevents an increase of output ripple voltage and noise once the DC-DC converter operates close to 100% duty cycle. The device automatically enters bypass mode once the battery voltage falls below the transition threshold $V_{IT\ BYP}$. The TPS62730 is available in a $1 \times 1.5\text{-mm}^2$ 6-pin USON package.

6 Device Comparison Table

T_A	PART NUMBER	OUTPUT VOLTAGE [V]	AUTOMATIC BYPASS MODE TRANSITION THRESHOLDS $V_{IT\ BYP}$		
			$V_{IT\ BYP}\ [V]$ RISING V_{IN}	$V_{IT\ BYP}\ [V]$ FALLING V_{IN}	$V_{IT\ BYP}\ [\text{mV}]$ HYSTERESIS
–40°C to 85°C	TPS62730	2.10	2.25	2.20	50
	TPS62731 ⁽¹⁾	2.05	2.2	2.15	50
	TPS62732	1.90	2.10	2.05	50
	TPS62733	2.3	2.48	2.41	70
	TPS62734 ⁽¹⁾	2.10	2.28	2.23	50
	TPS62735 ⁽¹⁾	2.10	2.33	2.23	100

(1) Device status is product preview. Contact TI for more details / samples.

7 Pin Configuration and Functions



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO		
VIN	3	PWR	V_{IN} power supply pin. Connect this pin close to the VIN terminal of the input capacitor. A ceramic capacitor of 2.2 μ F is required.
GND	4	PWR	GND supply pin. Connect this pin close to the GND terminal of the input and output capacitor.
ON/BYP	5	IN	This is the mode selection pin of the device. Pulling this pin to low forces the device into ultra low-power bypass mode. The output of the DC-DC converter is connected to VIN through an internal bypass switch. Pulling this pin to high enables the DC-DC converter operation. This pin must be terminated and is controlled by the system.
SW	2	OUT	This is the switch pin and is connected to the internal MOSFET switches. Connect the inductor to this terminal.
VOUT	6	IN	Feedback Pin for the internal feedback divider network and regulation loop. The internal bypass switch is connected between this pin and VIN. Connect this pin directly to the output capacitor with short trace.
STAT	1	OUT	This is the open-drain status output with active low level. An internal comparator drives this output. The pin is high impedance with ON/BYP = low. With ON/BYP set to high the device and the internal VOUT comparator becomes active. The active low STAT pin indicates if the DC-DC regulator is settled and the output voltage above the V_{TSTAT} threshold. If not used, this pin can be left open.

8 Specifications

8.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
Voltage ⁽²⁾	VIN, SW, VOUT	-0.3	4.2	V
	ON/BYP, STAT	-0.3	$V_{IN} + 0.3 \leq 4.2$	V
Operating junction temperature, T_J		-40	125	°C
Storage temperature, T_{stg}		-65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltages are with respect to network ground pin.

8.2 ESD Ratings

		VALUE	UNIT
V _(ESD)	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±2000	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	±1000	
	Machine model (MM), all pins	±150	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500-V HBM is possible with the necessary precautions.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 250-V CDM is possible with the necessary precautions.

8.3 Recommended Operating Conditions

Operating ambient temperature $T_A = -40$ to 85°C (unless otherwise noted)

	MIN	NOM	MAX	UNIT
Supply voltage V_{IN}	1.9		3.9	V
Effective inductance	1.5	2.2	3	μH
Effective output capacitance connected to V_{OUT}	1.0		10	μF
Operating junction temperature range, T_J	-40		125	°C
T_A Operating free air temperature range	-40		85	

8.4 Thermal Information

THERMAL METRIC ⁽¹⁾	TPS6273x	UNIT
	DRY	
	6 PINS	
θ_{JA}	293.8	°C/W
θ_{JCTop}	165.1	
θ_{JB}	160.8	
Ψ_{JT}	27.3	
Ψ_{JB}	159.6	
θ_{JCbot}	65.8	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).

8.5 Electrical Characteristics

$V_{IN} = 3.0 \text{ V}$, $V_{OUT} = 2.1 \text{ V}$, $\text{ON/BYP} = V_{IN}$, $T_A = -40^\circ\text{C}$ to 85°C typical values are at $T_A = 25^\circ\text{C}$ (unless otherwise noted), $C_{IN} = 2.2 \mu\text{F}$, $L = 2.2 \mu\text{H}$, $C_{OUT} = 2.2 \mu\text{F}$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT	
SUPPLY							
V_{IN}	Input voltage range		1.9	3.9		V	
I_Q	Operating quiescent current	ON/BYP = high, $I_{OUT} = 0 \text{ mA}$. $V_{IN} = 3 \text{ V}$ device not switching	25	40		μA	
		$I_{OUT} = 0 \text{ mA}$. device switching, $V_{IN} = 3.0 \text{ V}$, $V_{OUT} = 2.1 \text{ V}$	34				
		ON/BYP = high, Bypass switch active, $V_{IN} = V_{OUT} = 2.1 \text{ V}$	23				
I_{SD}	Shutdown current, Bypass Switch Activated ⁽¹⁾	ON/BYP = GND, leakage current into V_{IN}	30	550		nA	
		ON/BYP = GND, leakage current into V_{IN} , $T_A = 60^\circ\text{C}$	110				
ON/BYP							
$V_{IH\ TH}$	Threshold for detecting high ON/BYP	$1.9 \text{ V} \leq V_{IN} \leq 3.9 \text{ V}$, rising edge	0.8	1		V	
$V_{IL\ TH}$	Threshold for detecting low ON/BYP	$1.9 \text{ V} \leq V_{IN} \leq 3.9 \text{ V}$, falling edge	0.4	0.6		V	
I_{IN}	Input bias Current		0	50		nA	
POWER SWITCH							
$R_{DS(ON)}$	High side MOSFET on-resistance	$V_{IN} = 3.0 \text{ V}$	600			$\text{m}\Omega$	
	Low Side MOSFET on-resistance		350				
I_{LIMF}	Forward current limit MOSFET high side	$V_{IN} = 3.0 \text{ V}$, open loop	410			mA	
	Forward current limit MOSFET low side		410				
BYPASS SWITCH							
$R_{DS(ON)}$	Bypass Switch on-resistance		$V_{IN} = 2.1 \text{ V}$, $I_{OUT} = 20 \text{ mA}$, $T_J\max = 85^\circ\text{C}$	2.9	3.8	Ω	
			$V_{IN} = 3 \text{ V}$	2.1			
$V_{IT\ BYP}$	Automatic Bypass Switch Transition Threshold (Activation / Deactivation)	$\text{ON/BYP} = \text{high}$	TPS62730 (2.1 V)	ON / falling V_{IN}	2.14	2.20	2.3
				OFF / rising V_{IN}	2.19	2.25	2.35
			TPS62731 (2.05 V)	ON / falling V_{IN}	2.15		
				OFF / rising V_{IN}	2.20		
			TPS62732 (1.9 V)	ON / falling V_{IN}	2.05		
				OFF / rising V_{IN}	2.10		
			TPS62733 (2.3 V)	ON / falling V_{IN}	2.41		
				OFF / rising V_{IN}	2.48		
			TPS62734 (2.1 V)	ON / falling V_{IN}	2.23		
				OFF / rising V_{IN}	2.28		
$V_{IT\ BYP}$			TPS62735 (2.3 V)	ON / falling V_{IN}	2.23		V
				OFF / rising V_{IN}	2.33		

(1) Shutdown current into V_{IN} pin, includes internal leakage

Electrical Characteristics (continued)

$V_{IN} = 3.0 \text{ V}$, $V_{OUT} = 2.1 \text{ V}$, $\text{ON/BYP} = V_{IN}$, $T_A = -40^\circ\text{C}$ to 85°C typical values are at $T_A = 25^\circ\text{C}$ (unless otherwise noted), $C_{IN} = 2.2 \mu\text{F}$, $L = 2.2 \mu\text{H}$, $C_{OUT} = 2.2 \mu\text{F}$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
STAT STATUS OUTPUT (OPEN DRAIN)					
V_{TSTAT}	Threshold level for STAT OUTPUT in % from V_{OUT} ON/BYP = high and regulator is ready, V_{IN} falling	95%	98%	0.4	V
	ON/BYP = high and regulator is ready, V_{IN} rising ⁽²⁾	98%			
V_{OL}	Output Low Voltage	Current into STAT pin $I = 500 \mu\text{A}$, $V_{IN} = 2.3 \text{ V}$		0.4	
V_{OH}	Output High Voltage	Open drain output, external pull up resistor			V_{IN}
I_{LKG}	Leakage into STAT pin	ON/BYP = GND, $V_{IN} = V_{OUT} = 3 \text{ V}$	0	50	nA
REGULATOR					
t_{ONmin}	Minimum ON time	$V_{IN} = 3.0 \text{ V}$, $V_{OUT} = 2.1 \text{ V}$, $I_{OUT} = 0 \text{ mA}$	180		ns
t_{OFFmin}	Minimum OFF time	$V_{IN} = 2.3 \text{ V}$	50		ns
t_{Start}	Regulator start up time from transition ON/BYP = high to STAT = low	$V_{IN} = 3.0 \text{ V}$, $V_{OUT} = 3.0 \text{ V}$	50		μs
OUTPUT					
V_{REF}	Internal Reference Voltage		0.70		V
V_{VOUT}	VOUT Feedback Voltage Comparator Threshold Accuracy	$V_{IN} = 3.0 \text{ V}$	$T_A = 25^\circ\text{C}$	-1.5%	0% 1.5%
	DC output voltage load regulation	$I_{OUT} = 1 \text{ mA}$ to 50 mA	$V_{IN} = 3.0 \text{ V}$, $V_{OUT} = 2.1 \text{ V}$	-2.5%	0% 2.5%
	DC output voltage line regulation	$I_{OUT} = 20 \text{ mA}$	$2.4 \text{ V} \leq V_{IN} \leq 3.9 \text{ V}$	-0.01	%/mA
I_{LK_SW}	Leakage current into SW pin	$V_{IN} = V_{OUT} = V_{SW} = 3.0 \text{ V}$, $\text{ON/Byp} = \text{GND}$ ⁽³⁾	0.01	0.0	100 nA

- (2) The STAT output comparator is enabled once the rising input voltage exceeds the minimum input voltage V_{IN} min of 1.9 V. In case of the 1.9 V output voltage option, the STAT output is active once the rising input voltage V_{IN} exceeds 1.9 V.
- (3) The internal resistor divider network is disconnected from VOUT pin.

8.6 Typical Characteristics

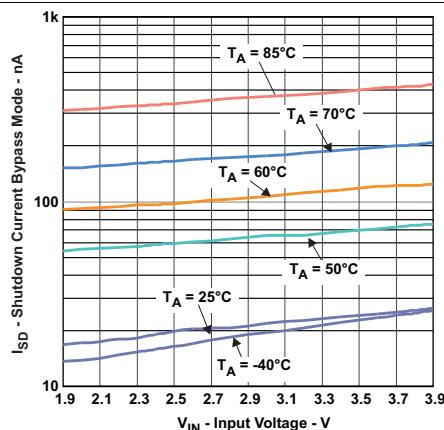


Figure 1. Shutdown Current Bypass Mode vs Input Voltage

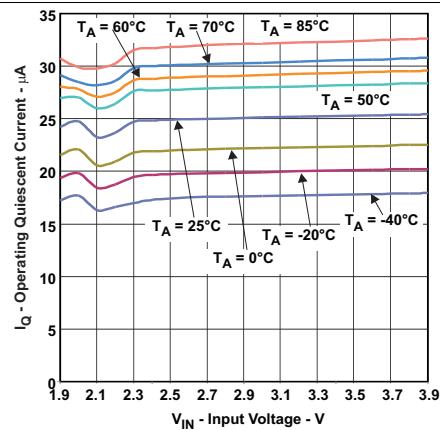


Figure 2. Operating Quiescent Current vs Input Voltage

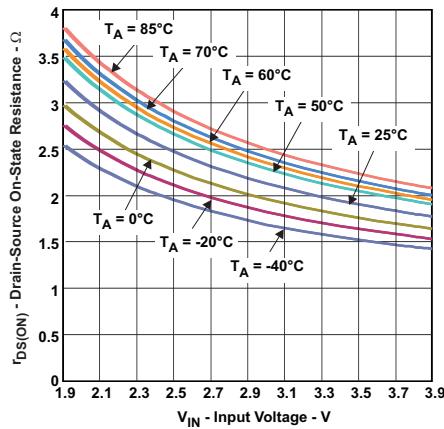


Figure 3. r_{DSON} Bypass vs Input Voltage

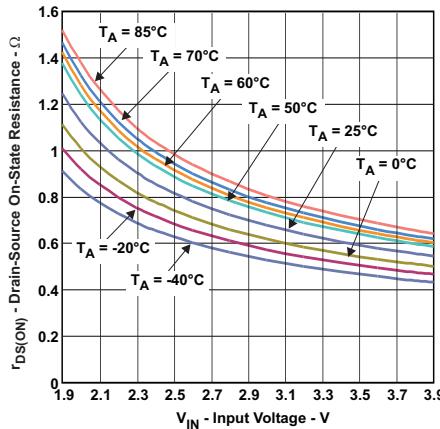


Figure 4. r_{DSON} PMOS vs Input Voltage

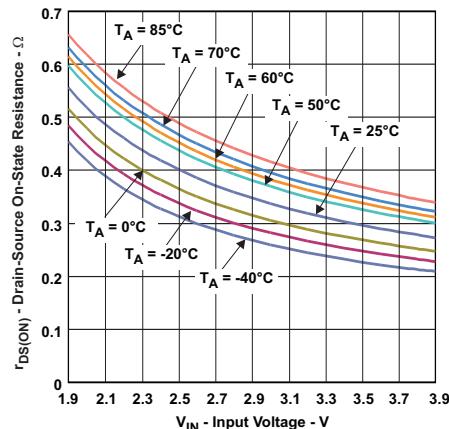


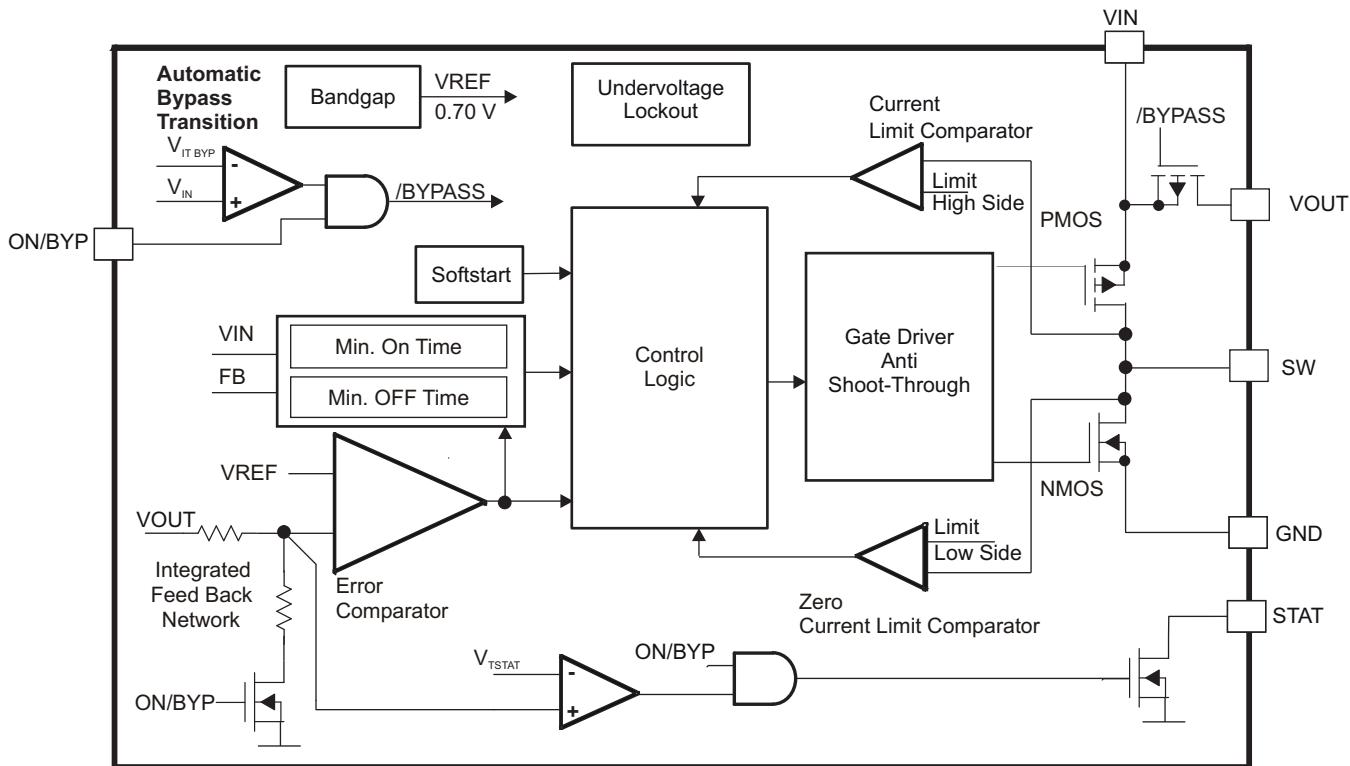
Figure 5. r_{DSON} NMOS vs Input Voltage

9 Detailed Description

9.1 Overview

The TPS62730 combines a synchronous buck converter for high efficient voltage conversion and an integrated ultra low power bypass switch to support low power modes of modern micro controllers and RF ICs.

9.2 Functional Block Diagram



9.3 Feature Description

9.3.1 DCS-Control™

The TPS62730 includes TI's DCS-Control, an advanced regulation topology, that combines the advantages of hysteretic and voltage mode control architectures. While a comparator stage provides excellent load transient response, an additional voltage feedback loop ensures high DC accuracy as well. The DCS-Control enables switch frequencies up to 3 MHz, excellent transient and AC load regulation as well as operation with small and cost-competitive external components. The TPS6273x devices offer fixed output voltage options featuring smallest solution size by using only three external components. Furthermore this step-down converter provides excellent low output voltage ripple over the entire load range which makes this part ideal for RF applications. In the ultra low-power bypass mode, the output of the device VOUT is directly connected to the input VIN through the internal bypass switch. In this mode, the buck converter is shut down and consumes only 30 nA typical input current. Once the device is turned from ultra low-power bypass mode into buck converter operation for an RF transmission, all the internal circuits of the regulator are activated within a start up time t_{Start} of typical 50 μ s. During this time the bypass switch is still turned on and maintains the output VOUT connected to the input VIN. Once the DC-DC converter is settled and ready to operate, the internal bypass switch is turned off and the system is supplied by the output capacitor and the other decoupling capacitors. The buck converter kicks in once the capacitors connected to VOUT are discharged to the level of the nominal buck converter output voltage. Once the output voltage falls below the threshold of the internal error comparator, a switch pulse is initiated, and the high side switch of the DC-DC converter is turned on. The high-side switch remains turned on until a minimum on time of t_{ONmin} expires and the output voltage trips the threshold of the error comparator or the inductor current reaches the high side switch current limit. Once the high side switch turns off, the low side switch

Feature Description (continued)

rectifier is turned on and the inductor current ramps down until the high side switch turns on again or the inductor current reaches zero. The converter operates in the PFM (pulse frequency modulation) mode during light loads, which maintains high efficiency over a wide load current range. In PFM mode, the device starts to skip switch pulses and generates only single pulses with the on time t_{ONmin} . The PFM mode of TPS62730 is optimized for low output ripple voltage if small external components are used.

The on time t_{ONmin} can be estimated to:

$$t_{ONmin} = \frac{V_{OUT}}{V_{IN}} \times 260 \text{ ns}$$

where

- t_{ONmin} : High side switch on time [ns]
 - V_{IN} : Input voltage [V]
 - V_{OUT} : Output voltage [V]
 -
- (1)

Therefore, the peak inductor current in PFM mode is approximately:

$$I_{LPFMpeak} = \frac{(V_{IN} - V_{OUT})}{L} \times t_{ONmin}$$

where

- V_{IN} : Input voltage [V]
 - V_{OUT} : Output voltage [V]
 - L : Inductance [μH]
 - $I_{LPFMpeak}$: PFM inductor peak current [mA]
- (2)

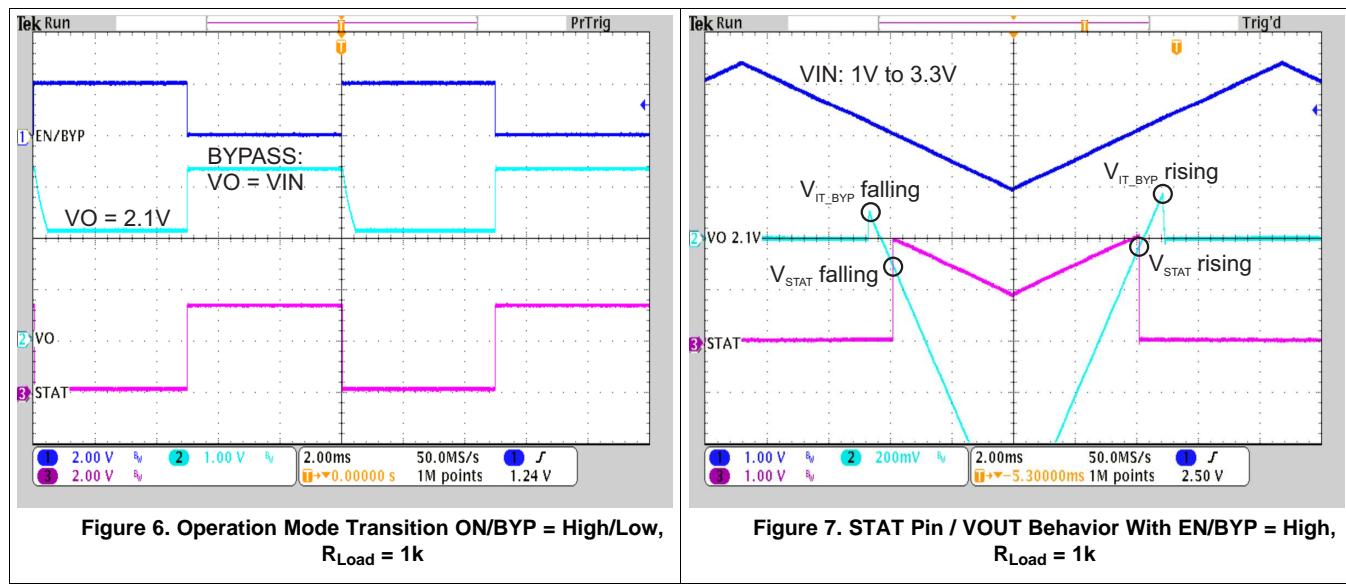
9.3.2 ON/BYP Mode Selection

The DC-DC converter is activated when ON/BYP is set high. For proper operation, the ON/BYP pin must be terminated and may not be left floating. This pin is controlled by the RF transceiver or micro controller for proper mode selection. Pulling the ON/BYP pin low activates the ultra low-power bypass mode with typical 30-nA current consumption. In this mode, the internal bypass switch is turned on and the output of the DC-DC converter is connected to the battery VIN. All other circuits like the entire internal-control circuitry, the High Side and Low Side MOSFETs of the DC-DC output stage are turned off as well the internal resistor feedback divider is disconnected. The ON/BYP must be controlled by a microcontroller for proper mode selection. In case of CC2540, connect this to the power down signal which is output on one of the P1.x ports (see CC2540 user guide).

9.3.3 STAT Open-Drain Output

The STAT output is active when the device is enabled (EN/BYP = high) and indicates the status of the output voltage. The STAT output is a open-drain output with active low level and needs a external pullup resistor to indicate a high level. It is driven by an internal comparator which monitors the output voltage V_{OUT} . The STAT pin is tied to low level, if the output voltage V_{OUT} is considered as valid and exceeding the threshold V_{TSTAT} (95% of V_{OUT} for falling V_{IN} and 98% of V_{OUT} for rising V_{IN}). The pin is high impedance with the ON/BYP pin set to low level or V_{OUT} is below the V_{TSTAT} threshold. If not used, the STAT pin can be left open. See [Figure 6](#) and [Figure 7](#).

Feature Description (continued)



9.4 Device Functional Modes

9.4.1 Start-Up

Once the device is supplied with a battery voltage, the bypass switch is activated. If the ON/BYP pin is set to high, the device operates in bypass mode until the DC-DC converter has settled and can kick in. During start-up, high peak currents can flow over the bypass switch to charge up the output capacitor and the additional decoupling capacitors in the system.

9.4.2 Automatic Transition from DC-DC to Bypass Operation

With the ON/BYP pin set to high, the TPS62730 is active and features an automatic transition between DC-DC and bypass mode to reduce the output ripple voltage to zero. Once the input voltage comes close to the output voltage of the DC-DC converter, the DC-DC converter operates close to 100% duty cycle operation. At this operating condition, the switch frequency would start to drop and would lead to increased output ripple voltage. The internal bypass switch is turned on once the battery voltage at VIN trips the Automatic Bypass Transition Threshold VIT BYP for falling VIN. The DC-DC regulator is turned off and therefore it generates no output ripple voltage. Due to the output is connected through the bypass switch to the input, the output voltage follows the input voltage minus the voltage drop across the internal bypass switch. In this mode the current consumption of the DC-DC converter is reduced to typically 23 μA . Once the input voltage increases and trips the bypass deactivation threshold VIT BYP for rising VIN, the DC-DC regulator turns on and the bypass switch is turned off. See [Figure 7](#) and [Figure 24](#).

9.4.3 Internal Current Limit

The TPS62730 integrates a High Side and Low Side MOSFET current limit to protect the device against heavy load or short circuit when the DC-DC converter is active. The current in the switches is monitored by current limit comparators. When the current in the High Side MOSFET reaches its current limit, the High Side MOSFET is turned off and the Low Side MOSFET is turned on to ramp down the current in the inductor. The High Side MOSFET switch can only turn on again, once the current in the Low Side MOSFET switch has fallen below the threshold of its current limit comparator. The bypass switch does not feature a current limit to support lowest current consumption.

10 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

The TPS62730 is a high-frequency synchronous step down DC-DC converter optimized for ultra low-power wireless applications. The device is optimized to supply TI's Low-Power Wireless sub 1-GHz and 2.4-GHz RF transceivers and system-on-chip (SoC) solutions.

10.2 Typical Application

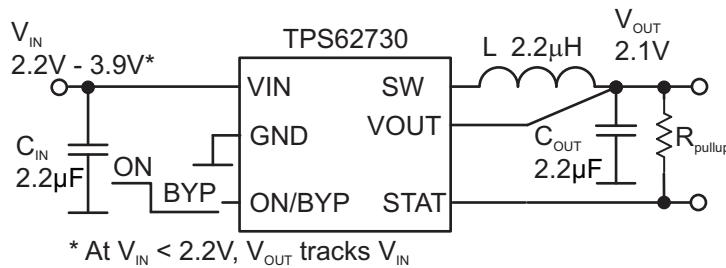


Figure 8. Typical Application

10.2.1 Design Requirements

The TPS6273x is a highly integrated DC-DC converter. The output voltage is internally fixed and does not require an external feedback divider network. For proper operation only a input- and output capacitor and an inductor is required. [Table 1](#) shows the components used for the application characteristic curves.

Table 1. List of Components

REFERENCE	DESCRIPTION	VALUE	MANUFACTURER	DIMENSIONS
TPS62730	Step-down converter with bypass mode		Texas Instruments	1.5 x 1.0 x 0.55 mm
CIN, COUT	Ceramic capacitor 0402 X5R 6.3V GRM155R60J225	2.2 μF	Murata	1.0 x 0.5 x 0.5 mm
L	Inductor MIPZ2012 2R2	2.2 μH	FDK	2.0 x 1.2 x 1.0 mm

10.2.2 Detailed Design Procedure

10.2.2.1 Output Filter Design (Inductor and Output Capacitor)

The TPS62730 is optimized to operate with effective inductance values in the range of 1.5 μH to 3 μH and with effective output capacitance in the range of 1.0 μF to 10 μF. The internal compensation is optimized to operate with an output filter of $L = 2.2 \mu H$ and $C_{OUT} = 2.2 \mu F$, which gives an LC output filter corner frequency of:

$$f_c = \frac{1}{2 \times \pi \times \sqrt{(2.2\mu H \times 2.2\mu F)}} = 72kHz \quad (3)$$

10.2.2.2 Inductor Selection

The inductor value affects its peak-to-peak ripple current, the PWM-to-PFM transition point, the output voltage ripple and the efficiency. The selected inductor must be rated for its DC resistance and saturation current. The inductor ripple current (ΔI_L) decreases with higher inductance and increases with higher V_{IN} or V_{OUT} . [Equation 4](#) calculates the maximum inductor current under static load conditions. The saturation current of the inductor should be rated higher than the maximum inductor current as calculated with [Equation 5](#).

$$\Delta I_L = V_{out} \times \frac{1 - \frac{V_{out}}{V_{in}}}{L \times f}$$

where

- f = Switching Frequency
 - L = Inductor Value
 - ΔI_L = Peak-to-Peak inductor ripple current
- (4)

$$I_{Lmax} = I_{outmax} + \frac{\Delta I_L}{2}$$

where

- ΔI_L = Peak-to-Peak inductor ripple current
 - I_{Lmax} = Maximum Inductor current
- (5)

In high-frequency converter applications, the efficiency is essentially affected by the inductor AC resistance (that is, quality factor) and to a smaller extent by the inductor DCR value. To achieve high efficiency operation, care should be taken in selecting inductors featuring a quality factor above 25 at the switching frequency. Increasing the inductor value produces lower RMS currents, but degrades transient response. For a given physical inductor size, increased inductance usually results in an inductor with lower saturation current.

The total losses of the coil consist of both the losses in the DC resistance, $R_{(DC)}$, and the following frequency-dependent components:

- The losses in the core material (magnetic hysteresis loss, especially at high switching frequencies)
- Additional losses in the conductor from the skin effect (current displacement at high frequencies)
- Magnetic field losses of the neighboring windings (proximity effect)
- Radiation losses

The following inductor series from different suppliers have been used with the TPS62730 converters.

Table 2. List of Inductors

INDUCTANCE [μ H]	DIMENSIONS [mm ³]	INDUCTOR TYPE	SUPPLIER
2.2	2.0 × 1.2 × 1.0	LQM21PN2R2NGC	Murata
2.2	2.0 × 1.2 × 1.0	MIPSZ2012	FDK

10.2.2.3 DC-DC Output Capacitor Selection

The DCS-Control scheme of the TPS62730 allows the use of tiny ceramic capacitors. Ceramic capacitors with low ESR values have the lowest output voltage ripple and are recommended. The output capacitor requires either an X7R or X5R dielectric. Y5V and Z5U dielectric capacitors, aside from their wide variation in capacitance over temperature, become resistive at high frequencies. At light load currents the converter operate in power save mode and the output voltage ripple is dependent on the output capacitor value and the PFM peak inductor current.

10.2.2.4 Additional Decoupling Capacitors

In addition to the output capacitor there are further decoupling capacitors connected to the output of the TPS62730. These decoupling capacitor are placed closely at the RF transmitter or micro controller. The total capacitance of these decoupling capacitors should be kept to a minimum and should not exceed the values given in the reference designs, see [Figure 31](#) and [Figure 32](#). During mode transition from DC-DC operation to bypass mode the capacitors on the output VOUT are charged up to the battery voltage VIN through the internal bypass

switch. During mode transition from bypass mode to DC-DC operation, these capacitors must be discharged by the system supply current to the nominal output voltage threshold until the DC-DC converter will kick in. The charge change in the output and decoupling capacitors can be calculated according to [Equation 6](#). The energy loss due to charge and discharge of the output and decoupling capacitors can be calculated according to [Equation 7](#).

$$dQ_{COUT_CDEC} = C_{COUT_CDEC} \times (V_{IN} - V_{OUT_DC_DC})$$

where

- dQ_{COUT_CDEC} : Charge change needed to charge up and discharge the output and decoupling capacitors from $V_{OUT_DC_DC}$ to V_{IN} and vice versa
 - C_{COUT_CDEC} : Total capacitance on the VOUT pin of the device, includes output and decoupling capacitors
 - V_{IN} : Input (battery) voltage
 - $V_{OUT_DC_DC}$: nominal DC-DC output voltage V_{OUT}
- (6)

$$E_{Charge_Loss} = \frac{1}{2} \times C_{COUT_CDEC} \times (V_{IN}^2 - V_{OUT_DC_DC}^2)$$

where

- C_{COUT_CDEC} : Total capacitance on the VOUT pin of the device, includes output and decoupling capacitors
 - V_{IN} : Input (battery) voltage
 - $V_{OUT_DC_DC}$: nominal DC-DC output voltage V_{OUT}
- (7)

10.2.2.5 Input Capacitor Selection

Because of the nature of the buck converter having a pulsating input current, a low ESR input capacitor is required for best input voltage filtering to ensure proper function of the device and to minimize input voltage spikes. For most applications a 2.2 μ F to 4.7 μ F ceramic capacitor is recommended. The input capacitor can be increased without any limit for better input voltage filtering.

[Table 3](#) shows a list of tested input/output capacitors.

10.2.2.5.1 Input Buffer Capacitor Selection

In addition to the small ceramic input capacitor a larger buffer capacitor C_{Buf} is recommended to reduce voltage drops and ripple voltage. When using battery chemistries like Li-SOCl₂, Li-SO₂, Li-MnO₂, the impedance of the battery must be considered. These battery types tend to increase their impedance depending on discharge status and often can support output currents of only a few mA. Therefore a buffer capacitor is recommended to stabilize the battery voltage during DC-DC operations (for example, for an RF transmission). A voltage drop on the input of the TPS62730 during DC-DC operation impacts the advantage of the step-down conversion for system power reduction. Furthermore the voltage drops can fall below the minimum recommended operating voltage of the device and leads to an early system cut off. Both impacts effects reduce the battery life time. To achieve best performance and to extract most energy out of the battery, a good procedure is to design the select the buffer capacitor value for an voltage drop below 50 mVpp during DC-DC operation. The capacitor value strongly depends on the used battery type, as well the current consumption during an RF transmission as well the duration of the transmission.

Table 3. List of Capacitor

CAPACITANCE [μ F]	SIZE	CAPACITOR TYPE	SUPPLIER
2.2	0402	GRM155R60J225	Murata

10.2.2.6 Checking Loop Stability

The first step of circuit and stability evaluation is to look from a steady-state perspective at the following signals:

- Switching node, SW
- Inductor current, I_L
- Output ripple voltage, $V_{OUT(AC)}$

Basic signals must be measured when evaluating a switching converter. When the switching waveform shows large duty cycle jitter or the output voltage or inductor current shows oscillations, the regulation loop may be unstable. This is often a result of board layout and/or L-C combination.

As a next step in the evaluation of the regulation loop, the load transient response is tested. The time between the application of the load transient and the turn on of the High Side MOSFET, the output capacitor must supply all of the current required by the load. V_{OUT} immediately shifts by an amount equal to $\Delta I_{(LOAD)} \times ESR$, where ESR is the effective series resistance of C_{OUT} . $\Delta I_{(LOAD)}$ begins to charge or discharge C_O generating a feedback error signal used by the regulator to return V_{OUT} to its steady-state value. The results are most easily interpreted when the device operates in PWM mode.

During this recovery time, V_{OUT} can be monitored for settling time, overshoot or ringing that helps judge the converter's stability. Without any ringing, the loop has usually more than 45° of phase margin.

Because the damping factor of the circuitry is directly related to several resistive parameters (for example, MOSFET $r_{DS(on)}$) that are temperature dependant, the loop stability analysis must be done over the input voltage range, load current range, and temperature range.

10.2.3 Application Curves

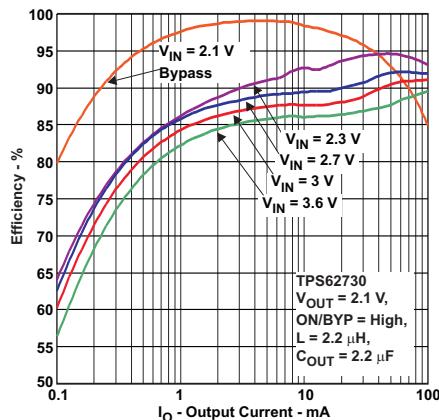


Figure 9. Efficiency vs Output Current

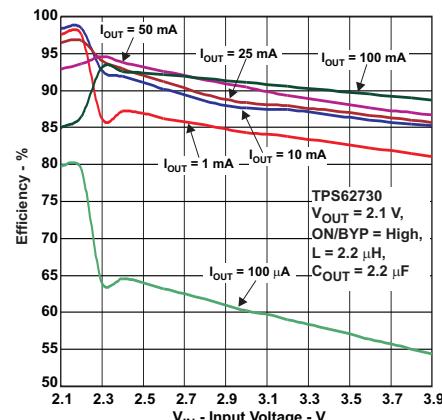


Figure 10. Efficiency vs Input Voltage

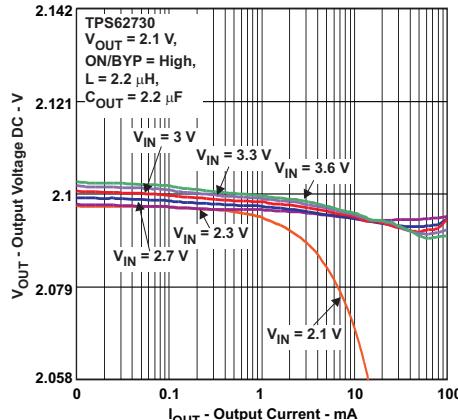


Figure 11. Output Voltage vs Output Current

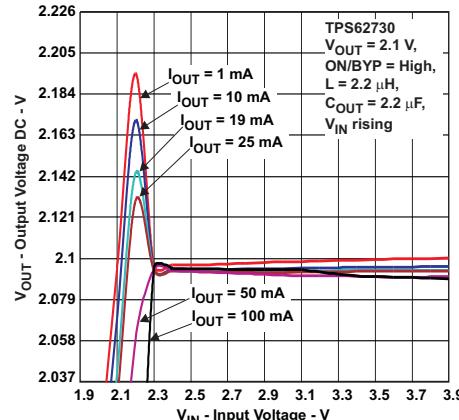
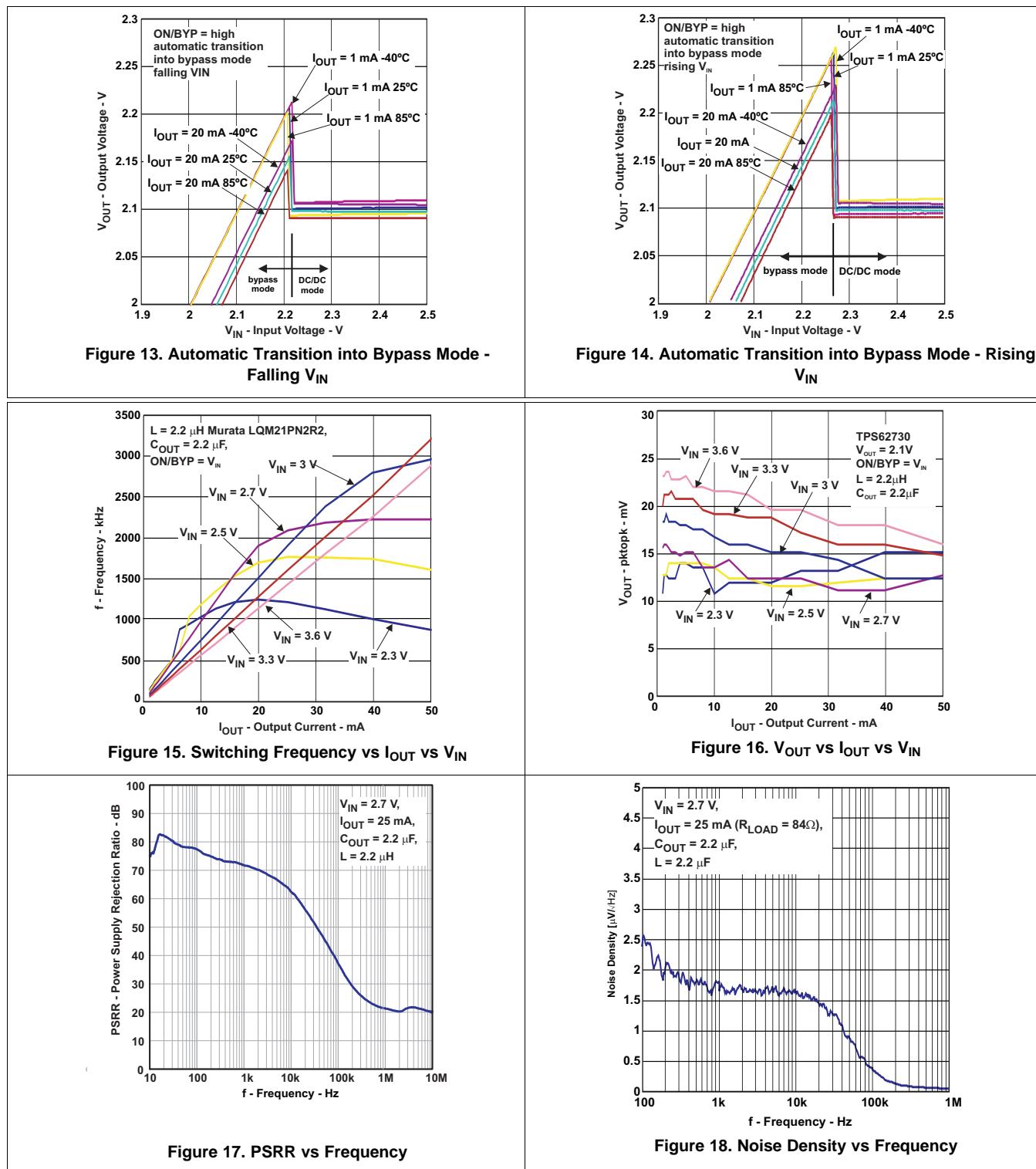


Figure 12. Output Voltage vs Input Voltage



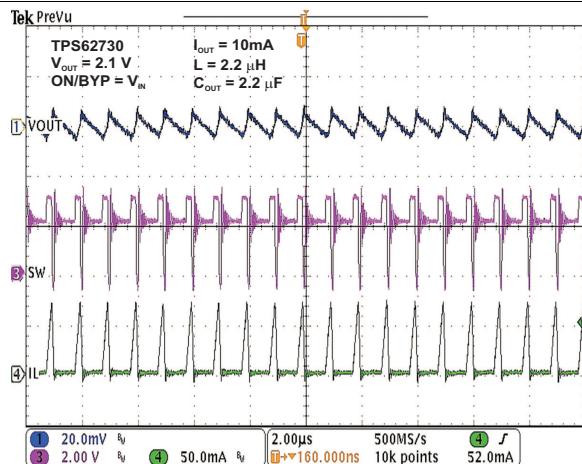
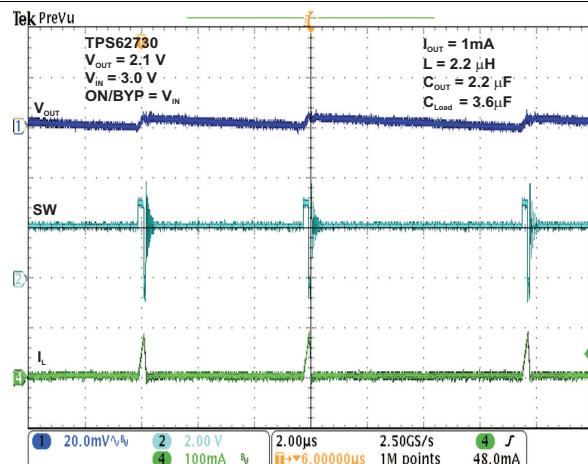
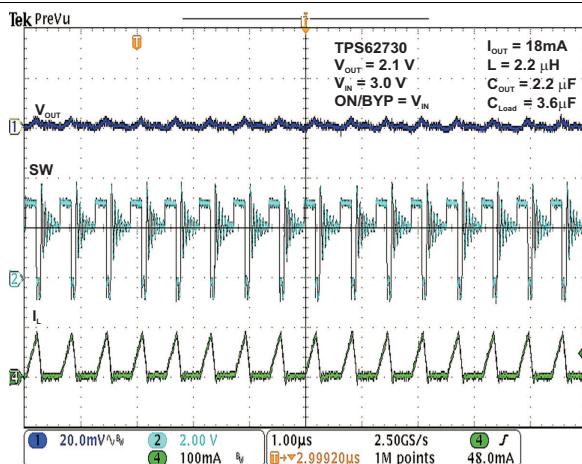
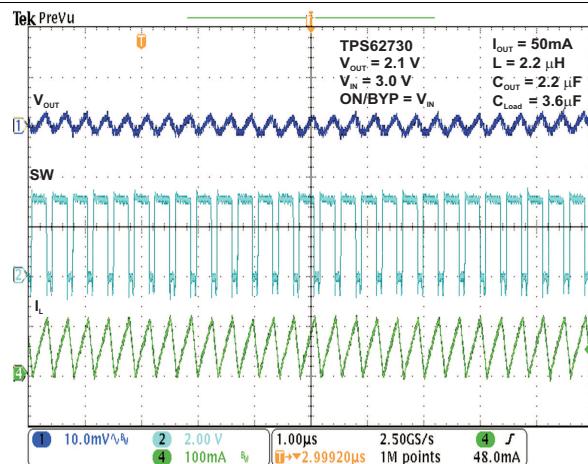
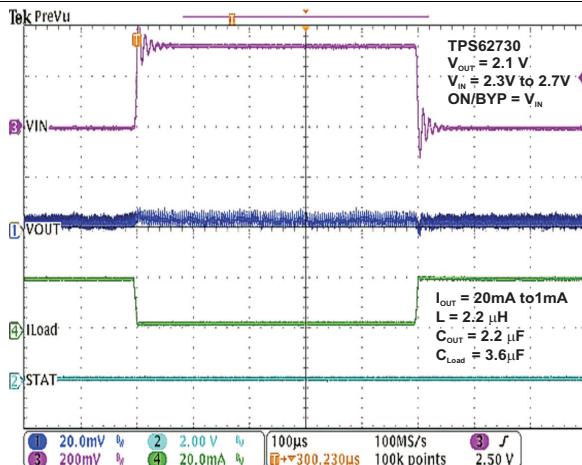
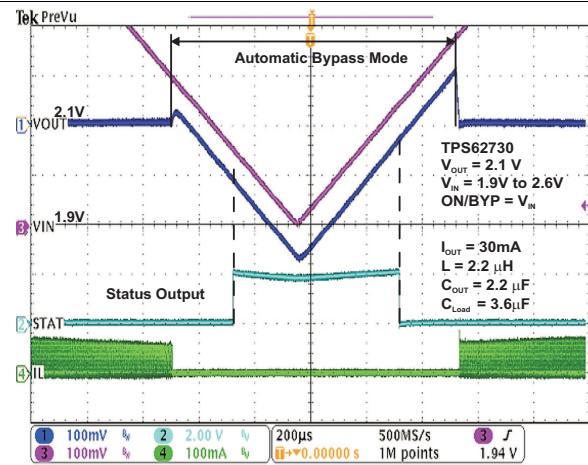
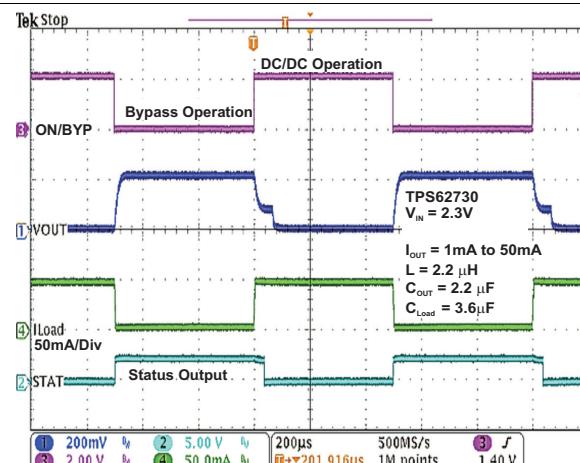
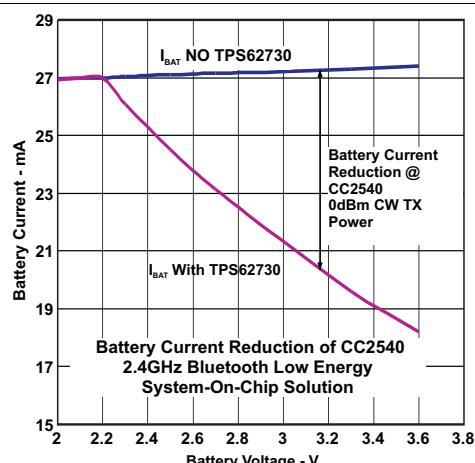
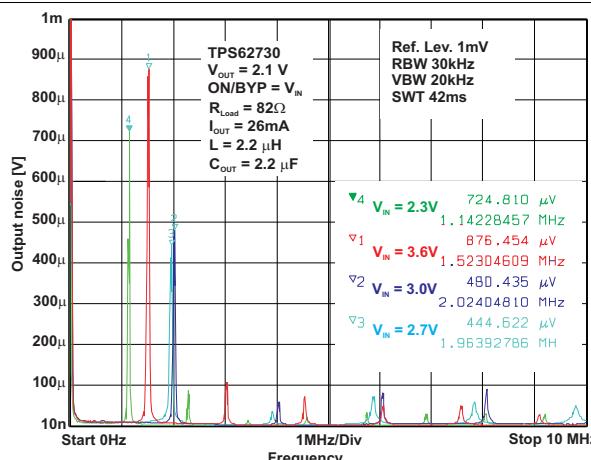
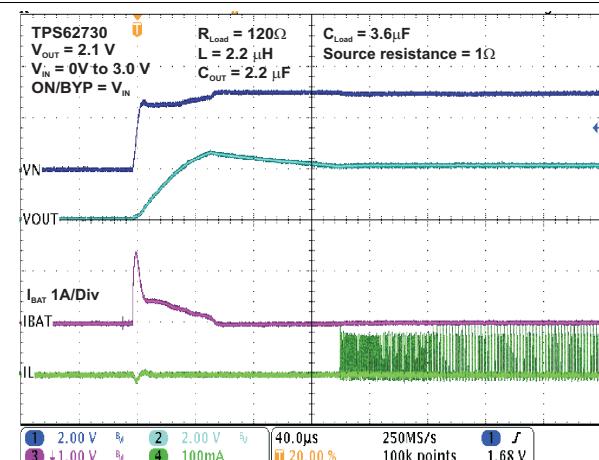
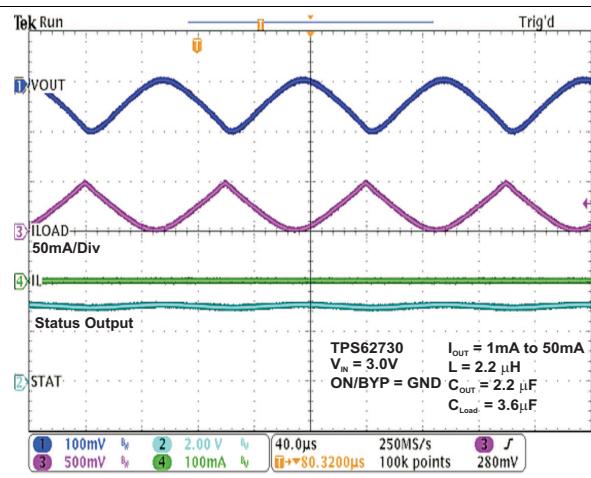
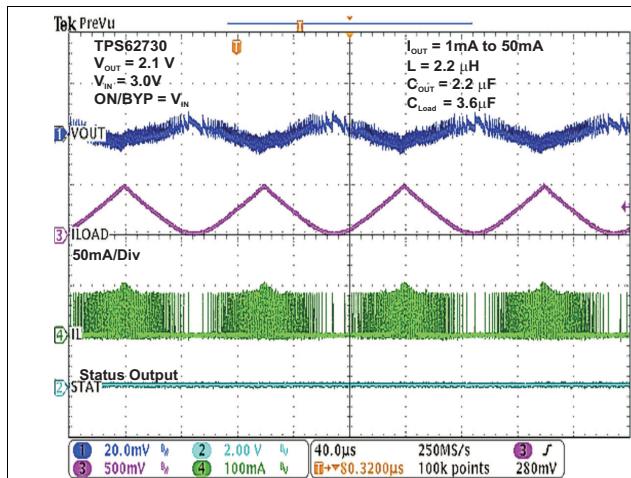

 Figure 19. DC-DC Mode Operation $I_{OUT} = 10 \text{ mA}$

 Figure 20. DC-DC Mode Operation $I_{OUT} = 1 \text{ mA}$

 Figure 21. DC-DC Mode Operation $I_{OUT} = 18 \text{ mA}$

 Figure 22. DC-DC Mode Operation $I_{OUT} = 50 \text{ mA}$


Figure 23. DC-DC Mode Operation Line and Load Transient Performance


 Figure 24. Automatic Bypass Transition with Falling / Rising Input Voltage V_{IN}



10.3 System Examples

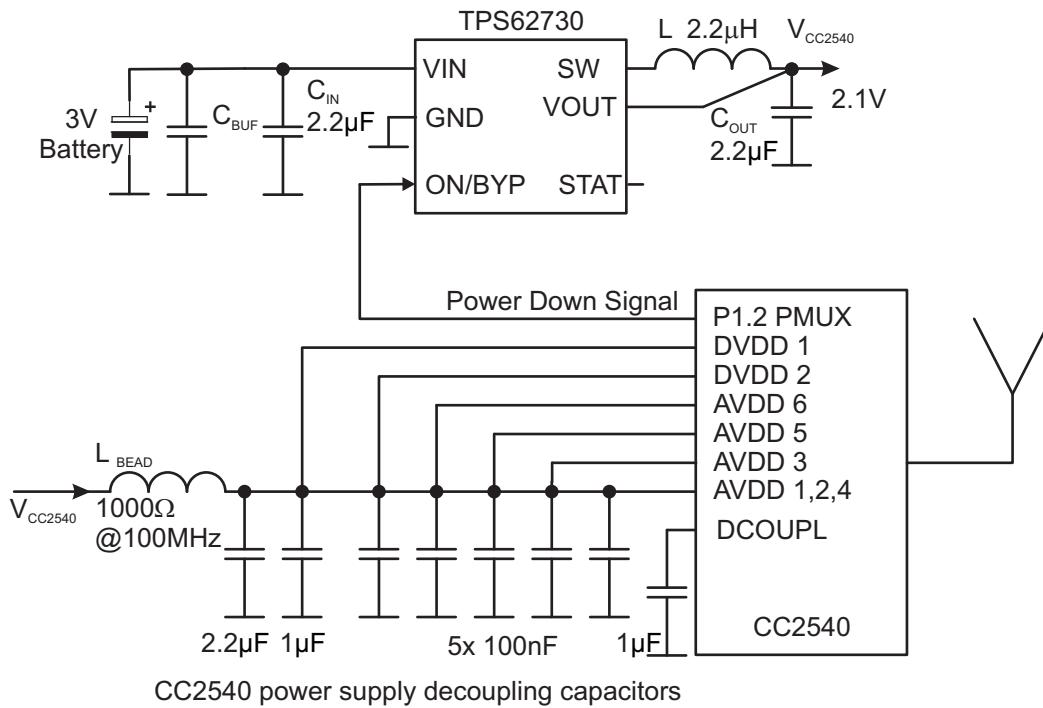


Figure 31. System Example CC2540

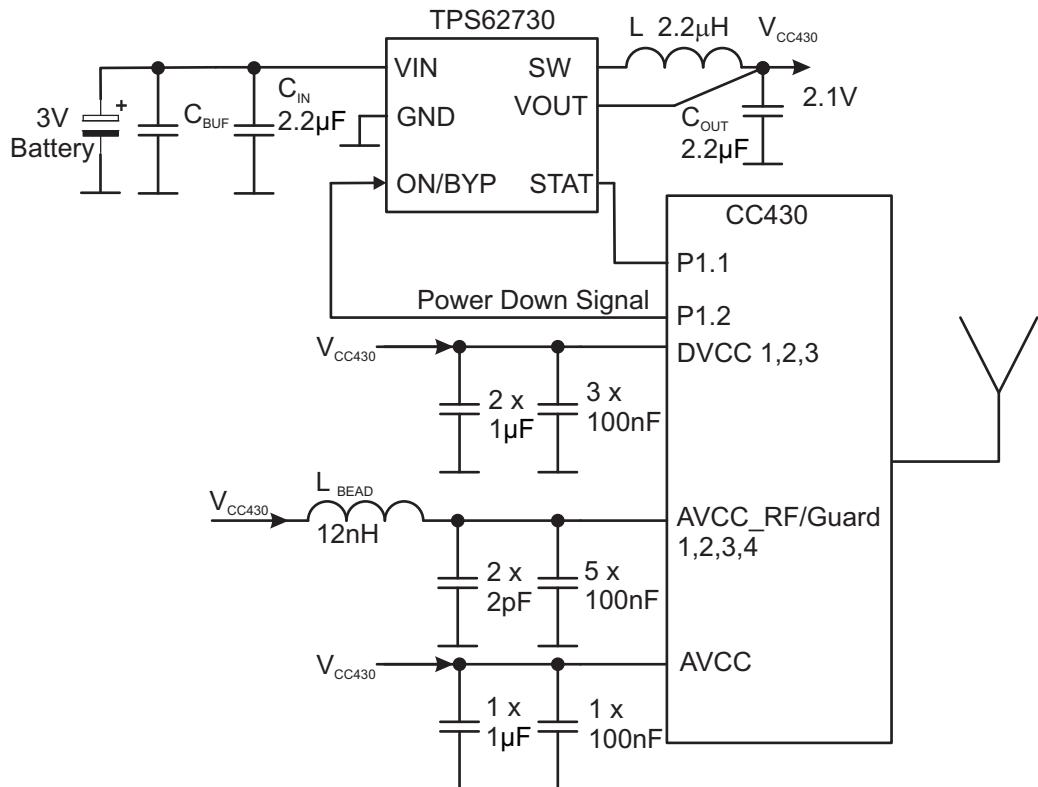


Figure 32. System Example CC430

11 Power Supply Recommendations

The power supply to the TPS62730 must have a current rating according to the supply voltage, output voltage and output current of the TPS62730.

12 Layout

12.1 Layout Guidelines

As for all switching power supplies, the layout is an important step in the design. Especially RF designs demand careful attention to the PCB layout. Care must be taken in board layout to get the specified performance. If the layout is not carefully done, the regulator could show poor line and/or load regulation, stability issues as well as EMI problems and interference with RF circuits. It is critical to provide a low inductance, impedance ground path. Therefore, use wide and short traces for the main current paths. The input capacitor should be placed as close as possible to the IC pins as well as the inductor and output capacitor. Use a common Power GND node and a different node for the Signal GND to minimize the effects of ground noise. Keep the common path to the GND PIN, which returns the small signal components and the high current of the output capacitors as short as possible to avoid ground noise. The V_{OUT} line should be connected to the output capacitor and routed away from noisy components and traces (for example, SW line).

12.2 Layout Example

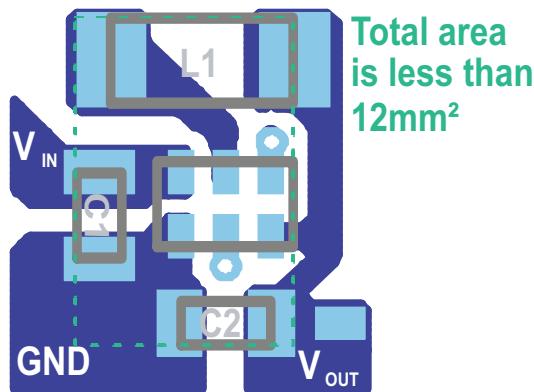


Figure 33. Recommended PCB Layout for TPS62730

13 Device and Documentation Support

13.1 Device Support

13.1.1 Third-Party Products Disclaimer

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13.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 4. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
TPS62730	Click here				
TPS62732	Click here				
TPS62733	Click here				

13.3 Trademarks

Bluetooth is a trademark of Bluetooth SIG.

All other trademarks are the property of their respective owners.

13.4 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

13.5 Glossary

[SLYZ022 — TI Glossary](#).

This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS62730DRYR	ACTIVE	SON	DRY	6	5000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	RP	Samples
TPS62730DRYT	ACTIVE	SON	DRY	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	RP	Samples
TPS62732DRYR	ACTIVE	SON	DRY	6	5000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	RR	Samples
TPS62732DRYT	ACTIVE	SON	DRY	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	RR	Samples
TPS62733DRYR	ACTIVE	SON	DRY	6	5000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	YA	Samples
TPS62733DRYT	ACTIVE	SON	DRY	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	YA	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.



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PACKAGE OPTION ADDENDUM

27-Jun-2014

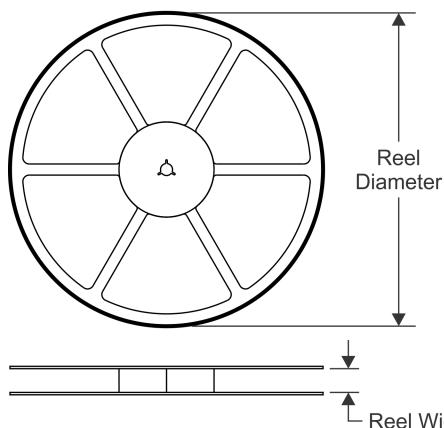
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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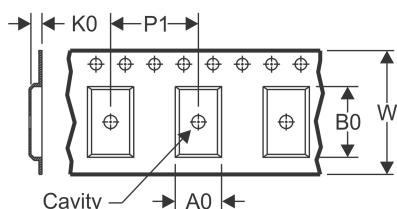
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

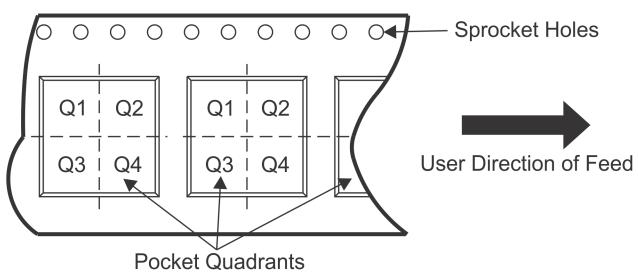


TAPE DIMENSIONS



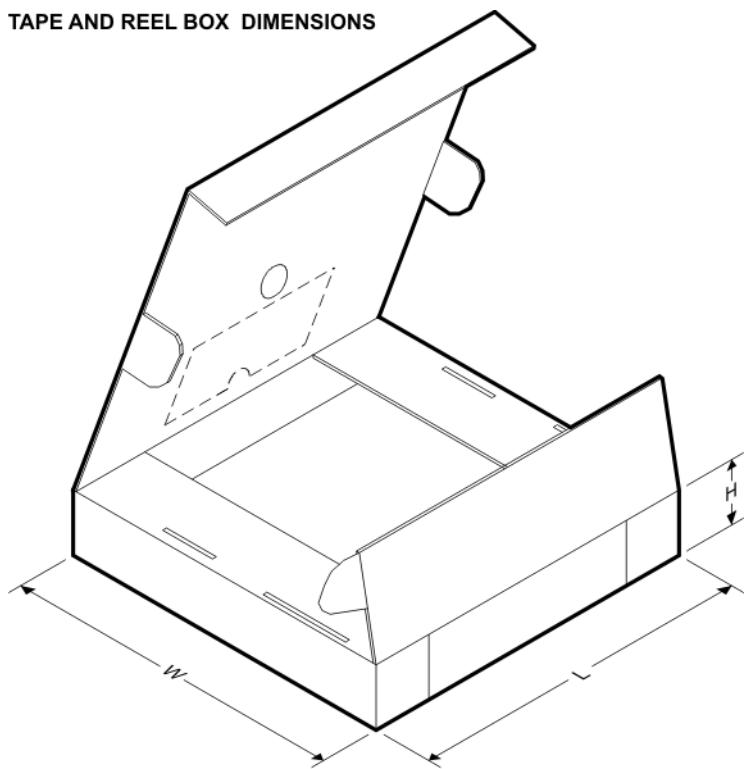
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS62730DRYR	SON	DRY	6	5000	179.0	8.4	1.2	1.65	0.7	4.0	8.0	Q1
TPS62730DRYT	SON	DRY	6	250	179.0	8.4	1.2	1.65	0.7	4.0	8.0	Q1
TPS62732DRYR	SON	DRY	6	5000	179.0	8.4	1.2	1.65	0.7	4.0	8.0	Q1
TPS62732DRYT	SON	DRY	6	250	179.0	8.4	1.2	1.65	0.7	4.0	8.0	Q1
TPS62733DRYR	SON	DRY	6	5000	179.0	8.4	1.2	1.65	0.7	4.0	8.0	Q1
TPS62733DRYT	SON	DRY	6	250	179.0	8.4	1.2	1.65	0.7	4.0	8.0	Q1

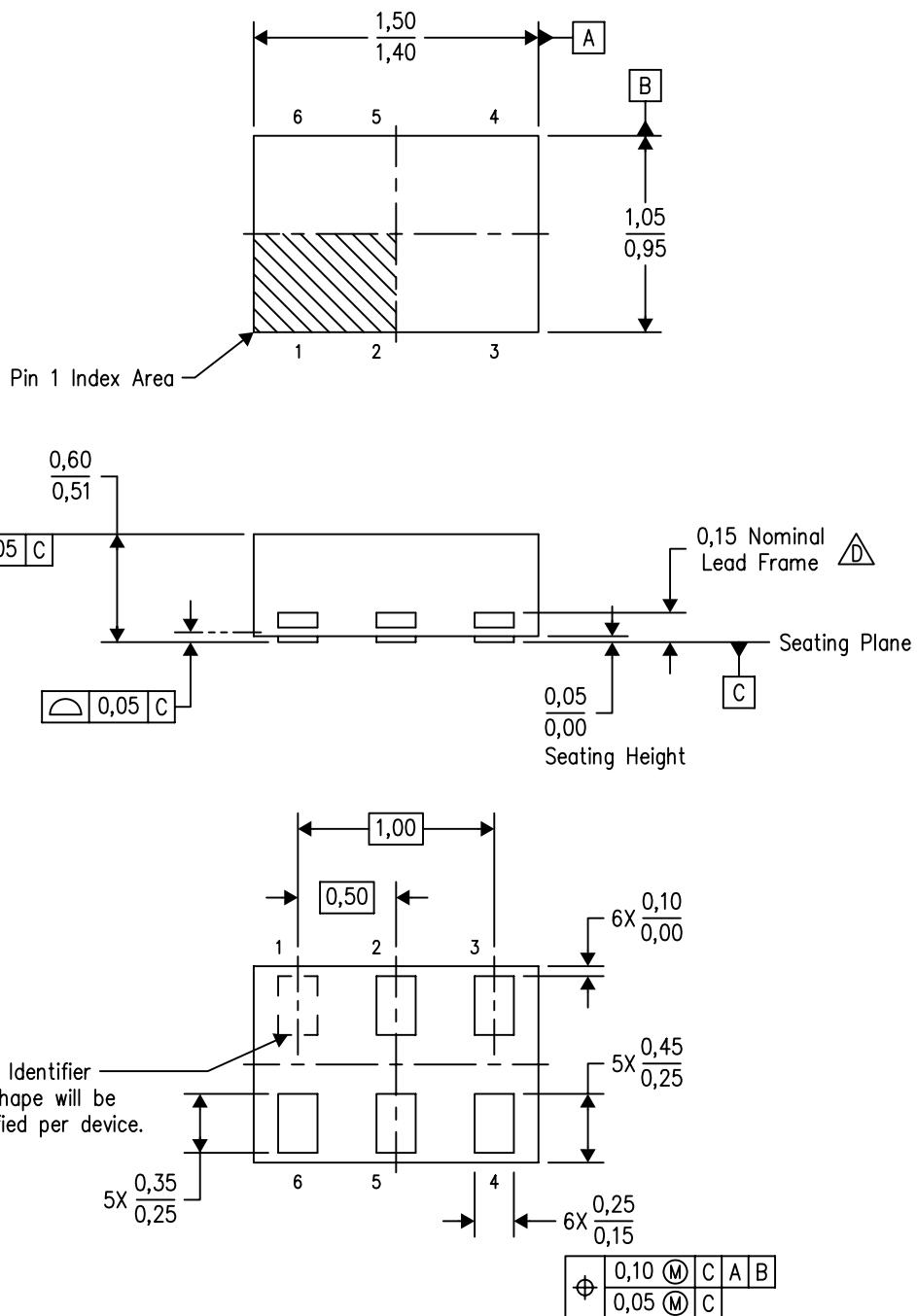
TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS62730DRYR	SON	DRY	6	5000	203.0	203.0	35.0
TPS62730DRYT	SON	DRY	6	250	203.0	203.0	35.0
TPS62732DRYR	SON	DRY	6	5000	203.0	203.0	35.0
TPS62732DRYT	SON	DRY	6	250	203.0	203.0	35.0
TPS62733DRYR	SON	DRY	6	5000	203.0	203.0	35.0
TPS62733DRYT	SON	DRY	6	250	203.0	203.0	35.0

DRY (R-PUSON-N6)

PLASTIC SMALL OUTLINE NO-LEAD



Bottom View

4207181/F 12/11

NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.

B. This drawing is subject to change without notice.

C. SON (Small Outline No-Lead) package configuration.

D. The exposed lead frame feature on side of package may or may not be present due to alternative lead frame designs.

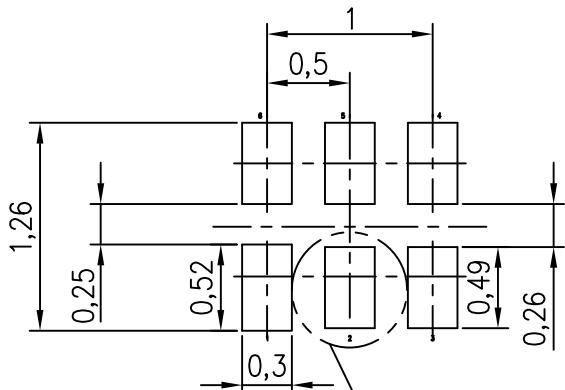
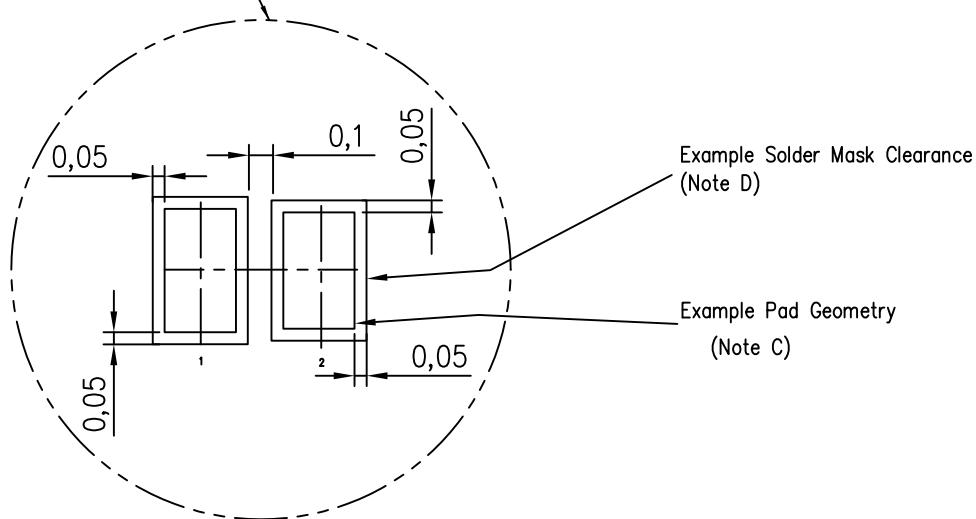
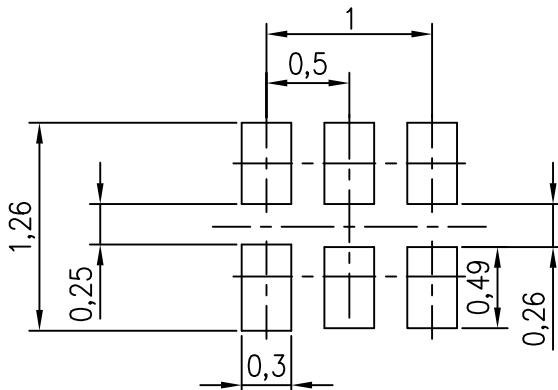
E. This package complies to JEDEC MO-287 variation UFAD.

F. See the additional figure in the Product Data Sheet for details regarding the pin 1 identifier shape.

DRY (R-PUSON-N6)

PLASTIC SMALL OUTLINE NO-LEAD

Example Board Layout

Example Stencil Design
(Note E, F, G)

4208310/E 02/13

- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
 - Maximum stencil thickness 0,127 mm (5 mils). All linear dimensions are in millimeters.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
 - Side aperture dimensions over-print land for acceptable area ratio > 0.66. Customer may reduce side aperture dimensions if stencil manufacturing process allows for sufficient release at smaller opening.

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Only those TI components which TI has specifically designated as military grade or "enhanced plastic" are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have **not** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

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