R.M.K. ENGINEERING COLLEGE

(An Autonomous Institution)

R.S.M Nagar, Kavaraipettai, Gummidipoondi Taluk Thiruvallur District, Tamil Nadu- 601206

Affiliated to Anna University, Chennai / Approved by AICTE, New Delhi

Accredited by NAAC with A+ Grade / An ISO 9001:2015 Certified Institution

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20CS401- COMPUTER ARCHITECTURE

REVISION TEST
Part A [40*2=80]
Answer any 40 questions

1. Write the basic functional units of computer
2. State the role of PC?
3. Explain how CPU execution time for a program is calculated?
4. Define Little Endian and Big Endian arrangement.
5. Define throughput and response time.
6. Define bus? What are the different buses in a CPU?
7. List the different types of addressing modes available.
8. Define Computer Architecture.
9. Discuss Stored Program Concept.
10. Solve 1 0 1 1 (-5) + 1 1 1 0 (-2)
11. List the overflow conditions for addition and subtraction.
12. Define EPC.
13. Represent the IEEE 754 representation of single precision floating point number.
14. Represent the IEEE 754 representation of double precision floating point number.
15. Write the rules for add operation on floating point numbers?
16. Write the rules for sub operation on floating point numbers?
17. What is normalized floating point number? Give example.
18. Write the algorithm for restoring division.
19. Write the algorithm for non-restoring division.
20. What is guard bit? List the ways to truncate the guard bits.
21. What is mean by branch history table / branch prediction / branch target buffer?
22. What is pipeline stall?
23. List the five stages in the instruction pipelining.
24. What are Hazards? List the types of hazards.
25. What is meant by hardwired control?
26. How data hazard can be prevented in pipelining?
27. Draw Two - state diagram for dynamic branch prediction?
28. Draw Four - state diagram for dynamic branch prediction?
29. What is superscalar processor?
30. Define pipelining.
31. What is temporal locality?
32. What is spatial locality?
33. Draw memory hierarchy
34. Define write-through scheme.
35. Define write-back scheme.
36. What is set-associative cache mapping?
37. What is associative cache mapping?
38. What is direct cache mapping?
39. What is the use of TLB?
40. Define cycle stealing.

41. What is flynn's classification?
42. Define Cluster.
43. What is UMA?
44. What is NUMA?
45. What is CC-NUMA?
46. Define SMP.
47. What is cache coherence problem.
48. What is MESI Protocol?
49. Give the taxonomy of parallel processing architecture.
50. What are the benefits of Clustering?

PART B

Answer All questions [50 marks]

1.	Explain Flynn's classification in detail.	(11)
2.	Explain SMP in detail	(13)
3.	Explain Cache coherence in detail.	(13)
4.	Explain Cluster with neat architecture diagram.	(13)