Title

Edge-AI Defect Classification for Semiconductor Images

Team Details

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Problem Statement Addressed

Edge-AI Defect Classification for Semiconductor Images

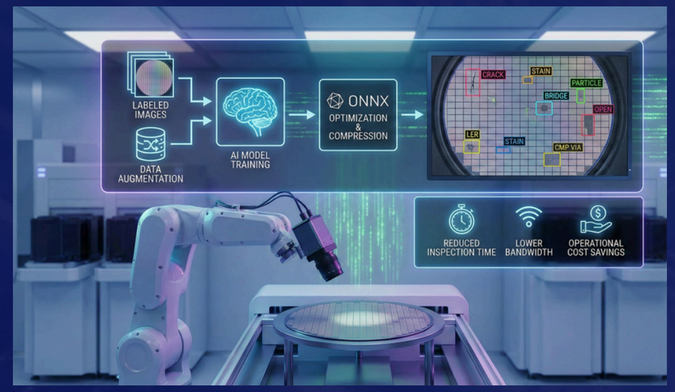
DESCRIPTION / DETAILS

- *Semiconductor manufacturing needs accurate defect detection to avoid yield loss and device failure.*
- *Manual and cloud-based inspection methods are slow and add latency.*
- *This project uses Edge-AI to automatically classify defects from semiconductor images.*
- *A lightweight deep learning model runs directly on low-power edge devices.*
- *Enables real-time, fast, and reliable quality inspection.*

Idea Description

KEY CONCEPT & APPROACH

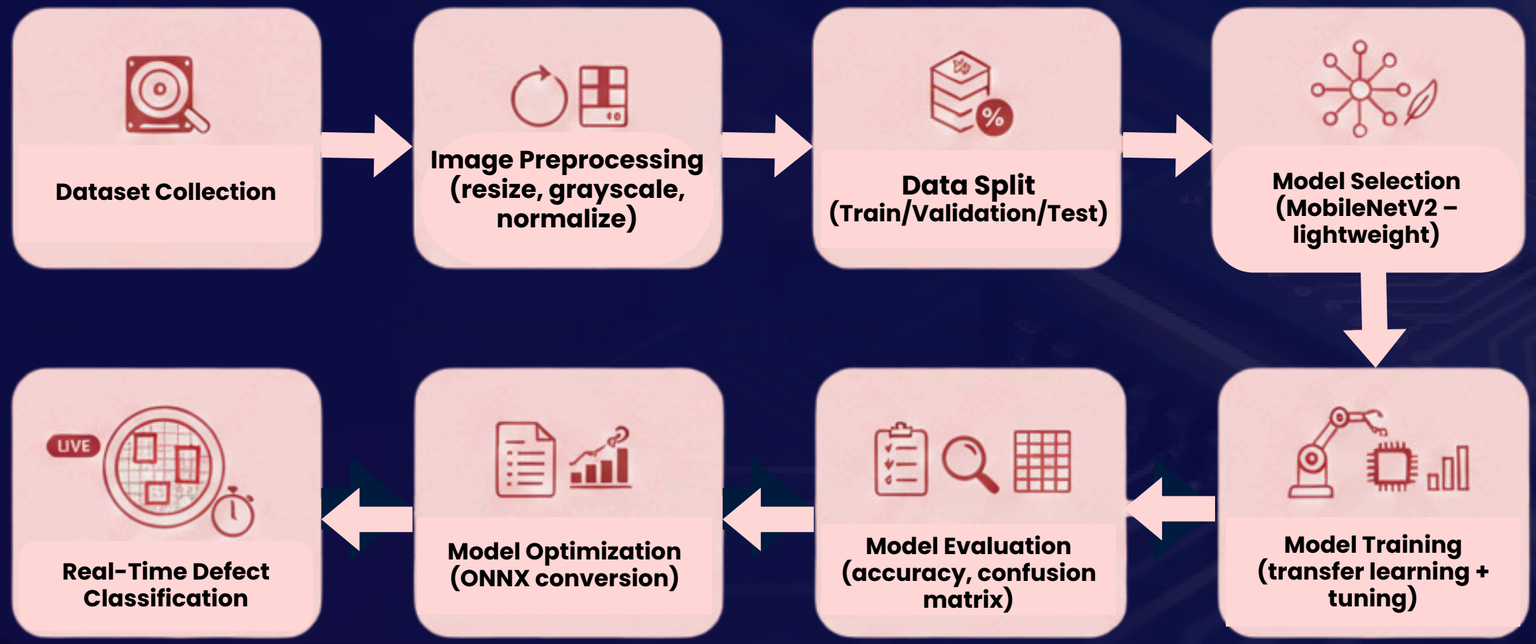
- *Edge-AI system for automated wafer defect classification*
- *Designed for real-time inspection environments*
- *Focus on low-latency & low-power execution*
- *Reduces manual review and cloud dependency*
- *Maintains high accuracy with compact models*



SOLUTION OVERVIEW

- *Train the model using labeled wafer and die images with data augmentation.*
- *Optimize the trained model using ONNX conversion and compression techniques.*
- *Classify multiple defect types such as cracks, stains, particles, bridge ,open ,LER, CMP vias.*
- *Reduce inspection time, bandwidth usage, and operational cost.*

Proposed Solution



SOLUTION DETAILS

- *A lightweight MobileNet-based deep learning model is trained on preprocessed semiconductor defect images using transfer learning, evaluated for accuracy, and optimized into an edge-compatible format (ONNX) to enable fast, real-time defect classification on low-resource devices.*

Innovation and Uniqueness

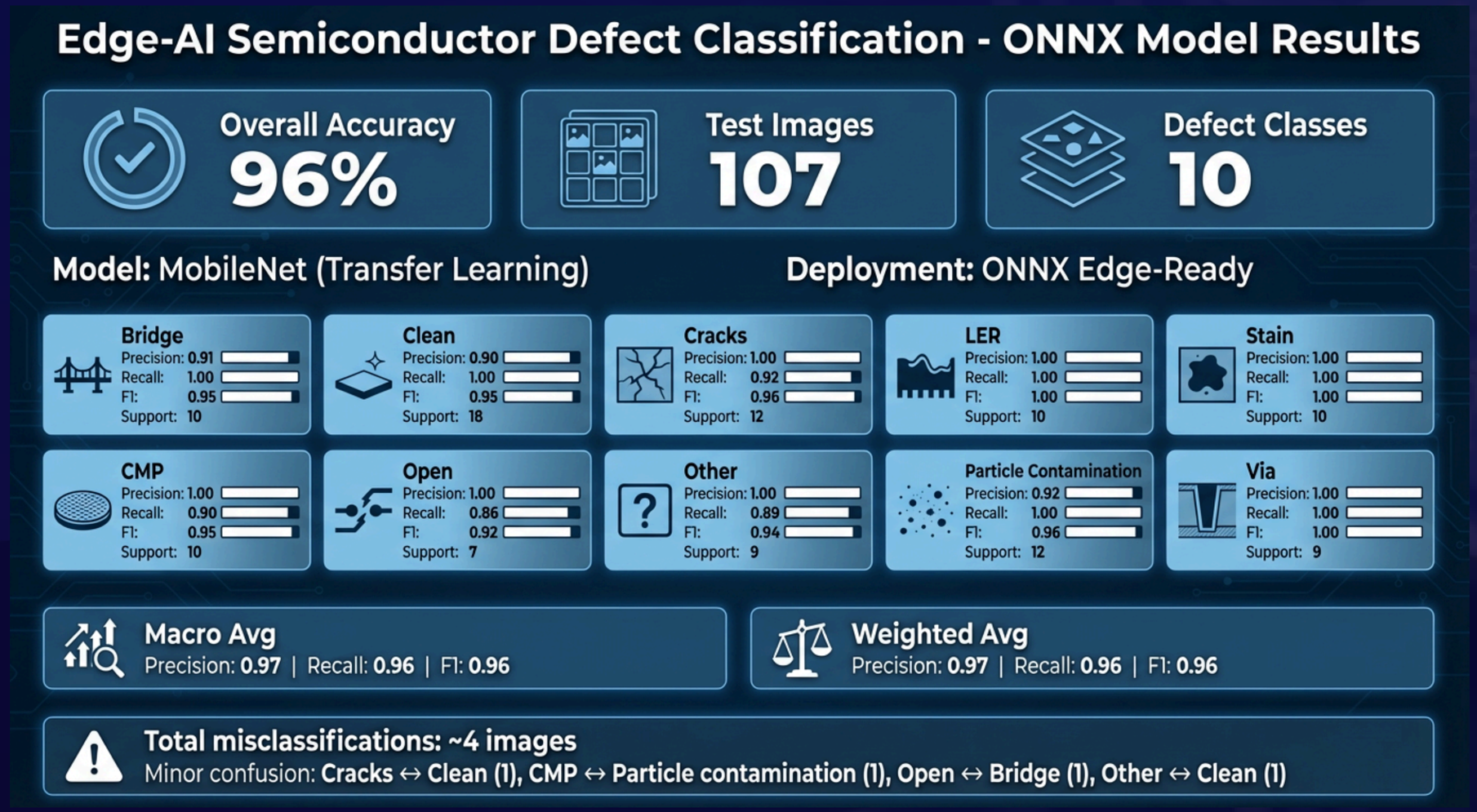
KEY INNOVATION

- *Edge-AI based semiconductor defect classification using lightweight MobileNet models*
- *Transfer learning + model optimization for low-size, high-accuracy performance*
- *Edge-ready model conversion ONNX built into the pipeline from the start*
- *Designed specifically for wafer/defect image categories, not generic image tasks*

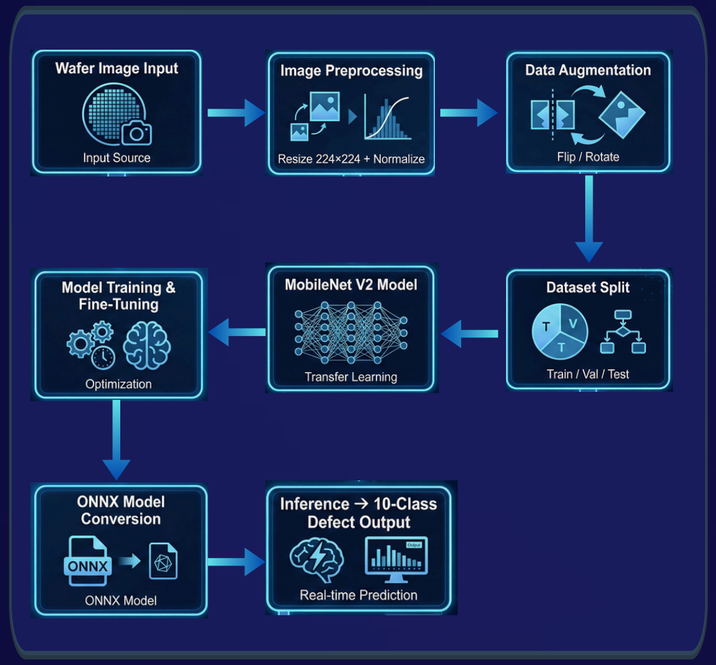
COMPETITIVE ADVANTAGE

- *Faster inference with low compute compared to heavy CNN/cloud models*
- *Lower deployment cost — runs on low-resource edge hardware*
- *No cloud dependency → reduced latency and better data privacy*
- *Scalable and easy to integrate into real-time inspection workflows*
- *High accuracy with small model size for practical industrial use*

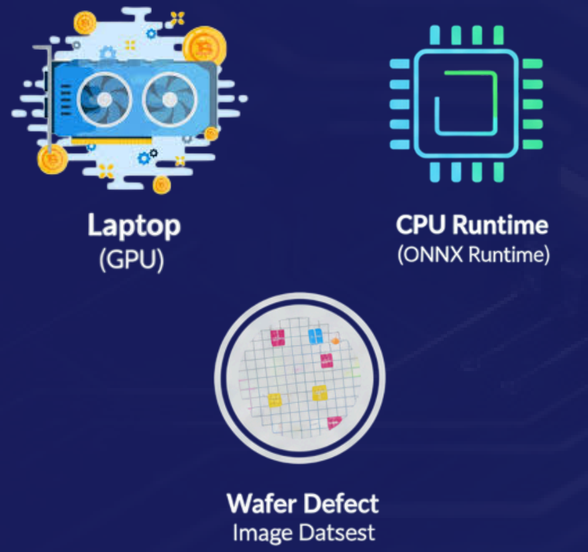
Impact and Benefits



Technology & Feasibility/Methodology Used



Software Architecture



Hardware Components

Development Tools

GitHub Link

GitHub Repository

https://github.com/Senthil7271/edge-ai-wafer-defect-classifier

Dataset Folder

https://drive.google.com/drive/folders/1nrMQLJqcVQ7cgJZH3JaNslrel6j5rm_e?usp=sharing

Research and References

Research Background & Methodology

- *Semiconductor wafer defects such as cracks, LER, particle contamination, stains, vias, and CMP show distinct visual patterns that can be automatically learned using CNN-based models.*
- *The system uses MobileNetV2 with transfer learning to achieve high accuracy with low computational requirements.*
- *The trained model is optimized and compressed (ONNX) to enable real-time edge deployment with low latency.*
- *This approach enables faster automated inspection, improving early defect detection and overall manufacturing yield.*

References & Citations

- Semiconductor Wafer Defect Detection using Deep Learning - **https://primerascientific.com/pdf/psen/PSEN-04-097.pdf**
- Inspection and Classification of Semiconductor Wafer Surface Defects Using CNN Deep Learning Networks - https://www.mdpi.com/2076-3417/10/15/5340
- "Wafer Map Failure Pattern Classification Using Geometric Transformation-Invariant CNN - https://primerascientific.com/pdf/psen/PSEN-04-097.pdf