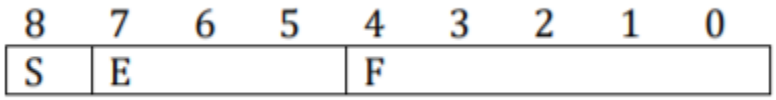
CSM152A Project2 Report

1. Introduction and requirement

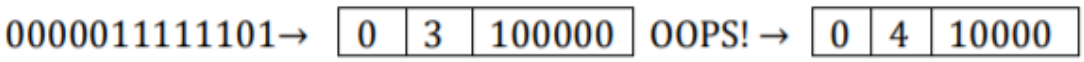
This lab uses Xilinx ISE to design and test a combinational circuit that converts a 13-bit linear encoding of an analog signal into a compounded 9-bit floating point representation (1-bit sign, 3-bit exponent, 5-bit significand).



To correctly design the circuit, we need to consider rounding, where we add 1 to significand if the sixth bit following the last leading zero is 1.

Rounding Examples		
Linear Encoding	**Floating Point Encoding**	**Rounding**
0000001101100	[0 010 11011]	Down
0000001101101	[0 010 11011]	Down
0000001101110	[0 010 11100]	Up
0000001101111	[0 010 11100]	Up

Also, we need to consider cases where the significand or exponent would overflow.



At last, we need to handle the most negative number (-4096) which cannot be represented in linear sign and magnitude form.

2. Design description

Basic Description of design:

Design of the circuit follows the overall design graph from the project spec. Firstly, we create a module that takes 13-bit number in two's complement form and obtain its sign and magnitude. Then we use another module which takes the magnitude, compute the raw exponent (before rounding) and extract six bits after the leading zero. At last, using the raw exponent and the extracted

six bits, the third module computes the final exponent and significand using the rounding rules.

Modules:

1. FPCVT

    input wire [12:0] D;

    output wire S;

    output wire [2:0] E;

    output wire [4:0] F;

Design idea: This module consists of the following three submodules to convert the two's complement in three steps: convert to sign-magnitude, compute raw exponent and extract six bits after leading zeros, compute final exponent and significand with rounding.

2. To_sign_mag

    input [12:0] twos_comp;

    output sign;

    output reg [12:0] mag;

Design idea: This submodule takes in a two's complement number and turns it into sign and magnitude. When determining magnitude, we need to look at sign to know whether to invert the number or not. Also if the number is -4096, we need to manually set the magnitude to max representation.

3. Raw_exp_mantissa

    input [12:0] mag;

    output reg [2:0] raw_exp;

    output reg [5:0] extract;

Design idea: This submodule takes in magnitude and compute the raw exponent and extract six bits after leading zeros. This can be done using the if … else if … else statement to implement the table from the spec. Also, we need to handle the case where there is equal to or more than 8 leading zeros.

4. Final_exp_mantissa

    input [2:0] raw_exp;

    input [5:0] extract;

    output reg [2:0] exp;

    output reg [4:0] mantissa;

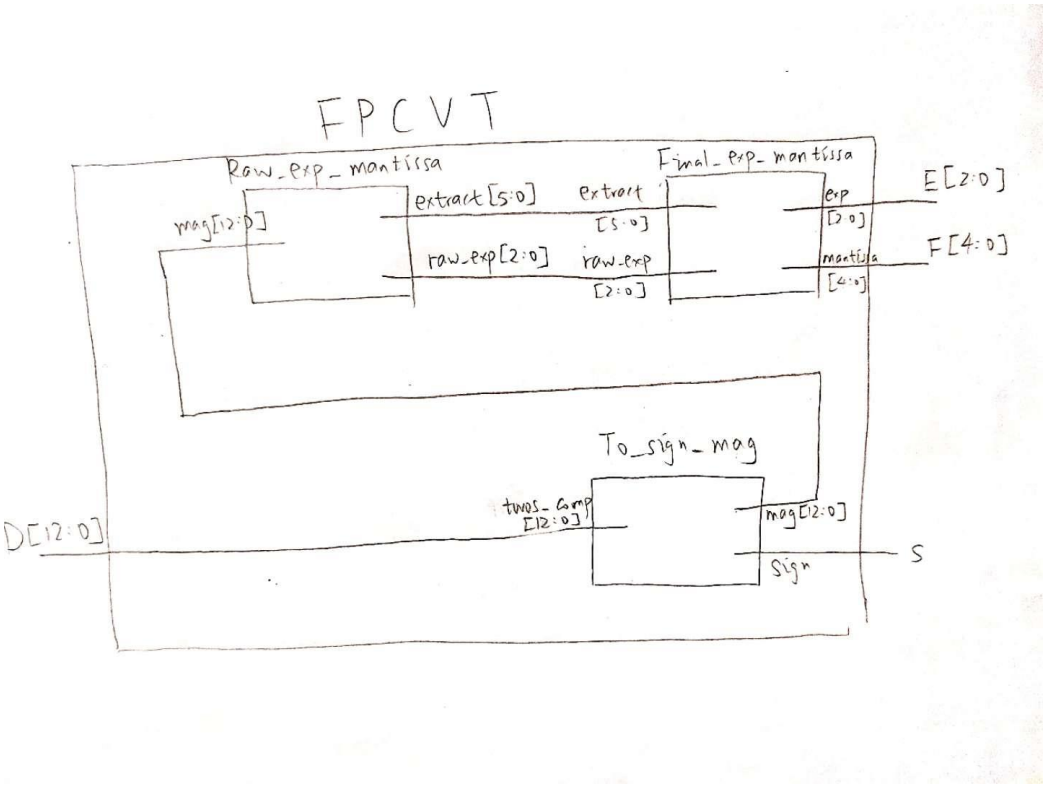
Design idea: This module takes in the raw exponent and extracted six bits and perform the rounding. We need to consider the case where the significand overflows after rounding up, and the corner case where the exponent overflows, in which we don't perform the rounding up at all.

Interaction among the modules:

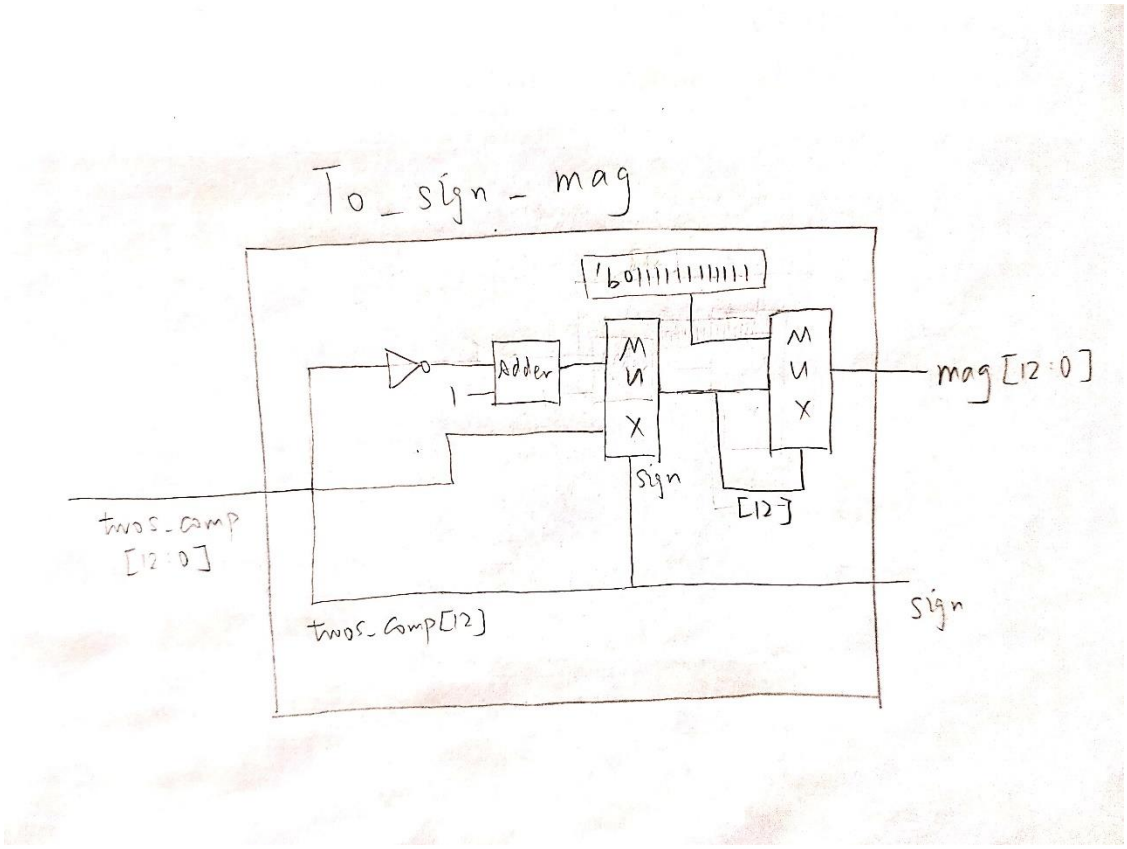
FPCVT module passes its input into To_sign_mag module, which returns the sign and magnitude of the input. Then it passes the magnitude into Raw_exp_mantissa, which returns the before-rounding exponent and six bits after the leading zeros. At last, Final_exp_mantissa takes in the raw exponent and six bits, and then using the rounding rules it computes the final exponent and mantissa. Together, the sign, exponent and significand are the output of FPCVT.

Hand-drawn Schematics:

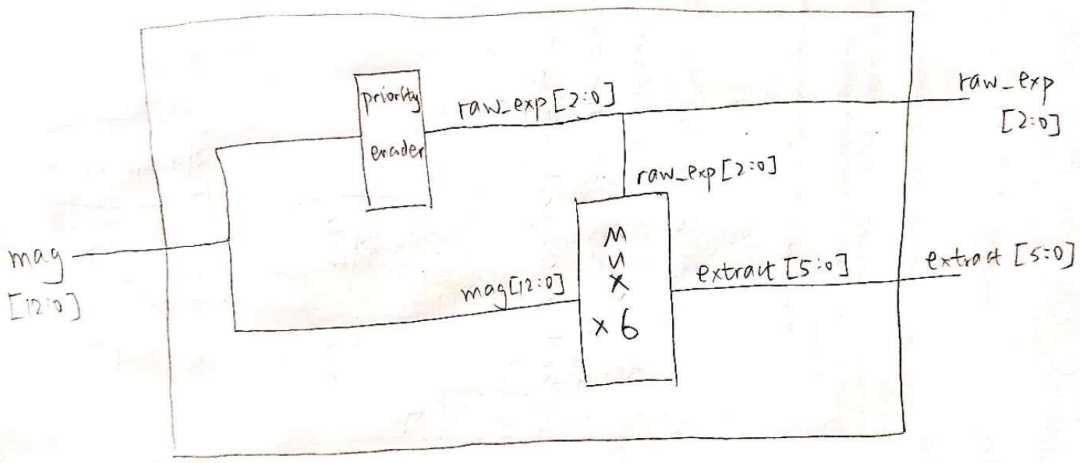
1. High-level module:



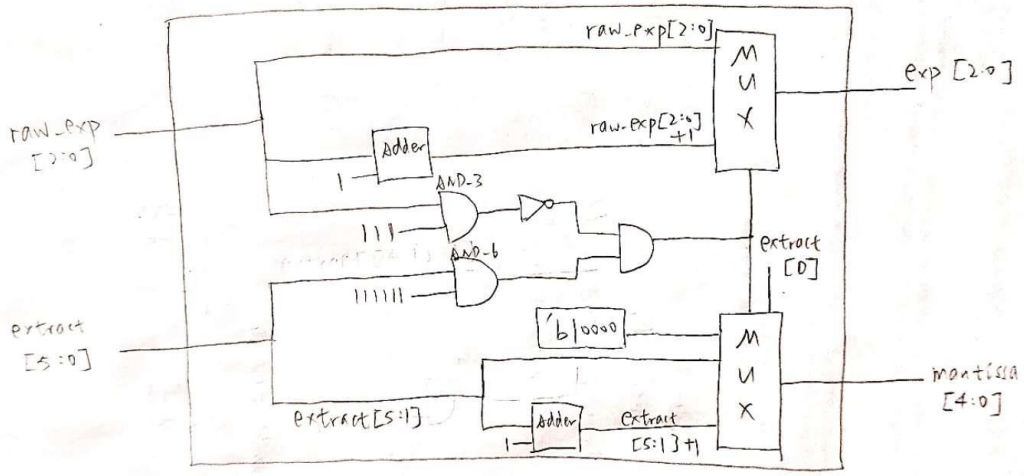
2. Individual minor modules



raw_exp_mantissa



Final_exp_mantissa



3. Simulation Documentation

simulation efforts:

My testbench provides inputs to the circuit and I need to manually check if the outputs are correct. The following are the test cases in my simulation (comment following each test case is the expected result):

// check if correctly handles equal or more than 8 leading zeros

D = 13'b0000000000000; // 0 000 00000

D = 13'b0000000000010; // 0 000 00010

D = 13'b0000000011111; // 0 000 11111

// general rounding test

D = 13'b0000001101100; // 0 010 11011

D = 13'b0000001101101; // 0 010 11011

D = 13'b0000001101110; // 0 010 11100

D = 13'b0000001101111; // 0 010 11100

// overflow rounding test

D = 13'b0000011111101; // 0 100 10000

D = 13'b0000000111111; // 0 010 10000

// negative test

D = 13'b1111001011010; // 1 100 11010

D = 13'b1111111111111; // 1 000 00001

// corner case test

// -4096

D = 13'b1000000000000; // 1 111 11111

// larger than max representation

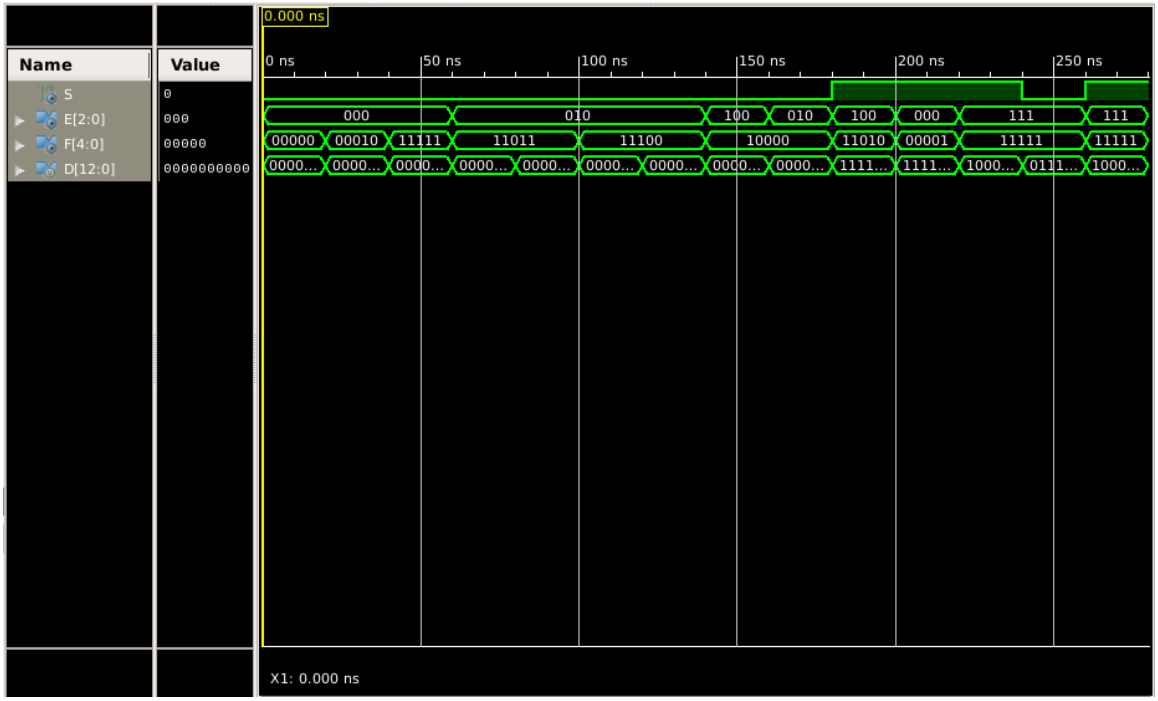
D = 13'b0111111101010; // 0 111 11111

D = 13'b1000000000111; // 1 111 11111

Bugs found during simulation:

In the overflow rounding test, I found that I accidentally set mantissa to 00000 instead of 10000 if it overflows, this causes results from that test incorrect, and I fixed it immediately.

simulation waveforms:



synthesis and implementation report:

1. Synthesis report

```
Release 14.7 - xst P.20131013 (lin64)
Copyright (c) 1995-2013 Xilinx, Inc.  All rights reserved.
-->
```

```
Parameter TMPDIR set to xst/projnav.tmp


Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.20 secs

-->
Parameter xsthdpdir set to xst


Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.20 secs

-->
Reading design: FPCVT.prj

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=========================================================================
*                      Synthesis Options Summary                        *
=========================================================================
---- Source Parameters
Input File Name                    : "FPCVT.prj"
Ignore Synthesis Constraint File   : NO

---- Target Parameters
Output File Name                   : "FPCVT"
Output Format                      : NGC
Target Device                      : xc6slx4-3-csg225

---- Source Options
Top Module Name                    : FPCVT
Automatic FSM Extraction           : YES
FSM Encoding Algorithm             : Auto
```

```
Safe Implementation               : No
FSM Style                         : LUT
RAM Extraction                    : Yes
RAM Style                         : Auto
ROM Extraction                    : Yes
Shift Register Extraction         : YES
ROM Style                         : Auto
Resource Sharing                  : YES
Asynchronous To Synchronous       : NO
Shift Register Minimum Size       : 2
Use DSP Block                     : Auto
Automatic Register Balancing      : No

---- Target Options
LUT Combining                     : Auto
Reduce Control Sets               : Auto
Add IO Buffers                    : YES
Global Maximum Fanout             : 100000
Add Generic Clock Buffer(BUFG)    : 16
Register Duplication              : YES
Optimize Instantiated Primitives  : NO
Use Clock Enable                  : Auto
Use Synchronous Set               : Auto
Use Synchronous Reset             : Auto
Pack IO Registers into IOBs       : Auto
Equivalent register Removal       : YES

---- General Options
Optimization Goal                 : Speed
Optimization Effort               : 1
Power Reduction                   : NO
Keep Hierarchy                    : No
Netlist Hierarchy                 : As_Optimized
RTL Output                        : Yes
Global Optimization               : AllClockNets
Read Cores                        : YES
Write Timing Constraints          : NO
Cross Clock Analysis              : NO
Hierarchy Separator               : /
Bus Delimiter                     : <>
Case Specifier                    : Maintain
Slice Utilization Ratio           : 100
BRAM Utilization Ratio            : 100
DSP48 Utilization Ratio           : 100
Auto BRAM Packing                 : NO
Slice Utilization Ratio Delta     : 5

=========================================================================


=========================================================================
*                          HDL Parsing                                  *
=========================================================================
Analyzing Verilog file "/home/ise/Project2/FPCVT.v" into library work
```

```
Parsing module <FPCVT>.
Parsing module <To_sign_mag>.
Parsing module <Raw_exp_mantissa>.
Parsing module <Final_exp_mantissa>.

=========================================================================
*                            HDL Elaboration                            *
=========================================================================

Elaborating module <FPCVT>.

Elaborating module <To_sign_mag>.
WARNING:HDLCompiler:413 - "/home/ise/Project2/FPCVT.v" Line 56: Result of 32-
bit expression is truncated to fit in 13-bit target.

Elaborating module <Raw_exp_mantissa>.

Elaborating module <Final_exp_mantissa>.
WARNING:HDLCompiler:413 - "/home/ise/Project2/FPCVT.v" Line 118: Result of 4-
bit expression is truncated to fit in 3-bit target.
WARNING:HDLCompiler:413 - "/home/ise/Project2/FPCVT.v" Line 122: Result of 6-
bit expression is truncated to fit in 5-bit target.

=========================================================================
*                           HDL Synthesis                               *
=========================================================================

Synthesizing Unit <FPCVT>.
    Related source file is "/home/ise/Project2/FPCVT.v".
    Summary:
      no macro.
Unit <FPCVT> synthesized.

Synthesizing Unit <To_sign_mag>.
    Related source file is "/home/ise/Project2/FPCVT.v".
    Found 32-bit adder for signal <n0010> created at line 56.
    Summary:
      inferred   1 Adder/Subtractor(s).
      inferred   2 Multiplexer(s).
Unit <To_sign_mag> synthesized.

Synthesizing Unit <Raw_exp_mantissa>.
    Related source file is "/home/ise/Project2/FPCVT.v".
WARNING:Xst:647 - Input <mag<12:12>> is never used. This port will be preserved
and left unconnected if it belongs to a top-level block or it belongs to a sub-
block and the hierarchy of this sub-block is preserved.
    Found 6-bit 8-to-1 multiplexer for signal <extract> created at line 92.
    Summary:
      inferred   7 Multiplexer(s).
Unit <Raw_exp_mantissa> synthesized.

Synthesizing Unit <Final_exp_mantissa>.
    Related source file is "/home/ise/Project2/FPCVT.v".
```

```
    Found 3-bit adder for signal <raw_exp[2]_GND_4_o_add_2_OUT> created at line
118.
    Found 5-bit adder for signal <extract[5]_GND_4_o_add_6_OUT> created at line
122.
    Summary:
      inferred   2 Adder/Subtractor(s).
      inferred   5 Multiplexer(s).
Unit <Final_exp_mantissa> synthesized.

=========================================================================
HDL Synthesis Report

Macro Statistics
# Adders/Subtractors                                   : 3
 3-bit adder                                           : 1
 32-bit adder                                          : 1
 5-bit adder                                           : 1
# Multiplexers                                         : 14
 13-bit 2-to-1 multiplexer                             : 2
 3-bit 2-to-1 multiplexer                              : 8
 5-bit 2-to-1 multiplexer                              : 3
 6-bit 8-to-1 multiplexer                              : 1

=========================================================================

=========================================================================
*                      Advanced HDL Synthesis                           *
=========================================================================


=========================================================================
Advanced HDL Synthesis Report

Macro Statistics
# Adders/Subtractors                                   : 3
 13-bit adder                                          : 1
 3-bit adder                                           : 1
 5-bit adder                                           : 1
# Multiplexers                                         : 14
 13-bit 2-to-1 multiplexer                             : 2
 3-bit 2-to-1 multiplexer                              : 8
 5-bit 2-to-1 multiplexer                              : 3
 6-bit 8-to-1 multiplexer                              : 1

=========================================================================

=========================================================================
*                         Low Level Synthesis                           *
=========================================================================

Optimizing unit <FPCVT> ...

Optimizing unit <To_sign_mag> ...
```

```
Mapping all equations...
Building and optimizing final netlist ...
Found area constraint ratio of 100 (+ 5) on block FPCVT, actual ratio is 3.

Final Macro Processing ...

=========================================================================
Final Register Report

Found no macro
=========================================================================

=========================================================================
*                           Partition Report                            *
=========================================================================

Partition Implementation Status
-------------------------------

  No Partitions were found in this design.

-------------------------------

=========================================================================
*                            Design Summary                             *
=========================================================================

Top Level Output File Name         : FPCVT.ngc

Primitive and Black Box Usage:
------------------------------
# BELS                             : 85
#      GND                         : 1
#      INV                         : 12
#      LUT1                        : 1
#      LUT4                        : 17
#      LUT5                        : 6
#      LUT6                        : 22
#      MUXCY                       : 12
#      VCC                         : 1
#      XORCY                       : 13
# IO Buffers                       : 22
#      IBUF                        : 13
#      OBUF                        : 9

Device utilization summary:
---------------------------

Selected Device : 6slx4csg225-3


Slice Logic Utilization:
 Number of Slice LUTs:                   58  out of   2400     2%
    Number used as Logic:                58  out of   2400     2%
```

```
Slice Logic Distribution:
 Number of LUT Flip Flop pairs used:     58
   Number with an unused Flip Flop:      58  out of     58   100%
   Number with an unused LUT:             0  out of     58     0%
   Number of fully used LUT-FF pairs:     0  out of     58     0%
   Number of unique control sets:         0

IO Utilization:
 Number of IOs:                          22
 Number of bonded IOBs:                  22  out of    132    16%

Specific Feature Utilization:

---------------------------
Partition Resource Summary:
---------------------------

  No Partitions were found in this design.

---------------------------


=================================================================================
Timing Report

NOTE: THESE TIMING NUMBERS ARE ONLY A SYNTHESIS ESTIMATE.
      FOR ACCURATE TIMING INFORMATION PLEASE REFER TO THE TRACE REPORT
      GENERATED AFTER PLACE-and-ROUTE.

Clock Information:
------------------
No clock signals found in this design

Asynchronous Control Signals Information:
----------------------------------------
No asynchronous control signals found in this design

Timing Summary:
---------------
Speed Grade: -3

   Minimum period: No path found
   Minimum input arrival time before clock: No path found
   Maximum output required time after clock: No path found
   Maximum combinational path delay: 16.307ns

Timing Details:
---------------
All values displayed in nanoseconds (ns)

=================================================================================
Timing constraint: Default path analysis
  Total number of paths / destination ports: 46540 / 9
```

```
--------------------------------------------------------------------------
Delay:               16.307ns (Levels of Logic = 13)
  Source:            D<12> (PAD)
  Destination:       E<2> (PAD)

  Data Path: D<12> to E<2>
                                Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     IBUF:I->O            18   1.222   1.049  D_12_IBUF (D_12_IBUF)
     INV:I->O              0   0.206   0.000  tsm/n0015<12>1_INV_0 (tsm/n0015<12>)
     XORCY:LI->O             16    0.136    1.233   tsm/Madd_n0010_Madd_xor<12>
(tsm/n0010<12>)
     LUT4:I1->O           13   0.205   1.277  tsm/Mmux_mag111 (M<8>)
     LUT6:I1->O          5   0.203   0.715  rem/Mmux_raw_exp11 (rem/Mmux_raw_exp1)
     LUT5:I4->O           11   0.205   1.130  rem/Mmux_raw_exp12 (raw_E<0>)
     LUT6:I2->O            1   0.203   0.580  rem/Mmux_extract44_SW0 (N12)
     LUT5:I4->O            1   0.205   0.808  rem/Mmux_extract45_SW0 (N16)
     LUT6:I3->O            4   0.205   1.048  rem/Mmux_extract45 (ex<3>)
     LUT6:I0->O            6   0.203   0.973  fem/GND_4_o_GND_4_o_equal_1_o<5>1
(fem/GND_4_o_GND_4_o_equal_1_o)
     LUT6:I3->O            1   0.205   0.944  fem/Mmux_exp211 (fem/Mmux_exp21)
     LUT6:I0->O            1   0.203   0.579  fem/Mmux_exp31 (E_2_OBUF)
     OBUF:I->O                 2.571          E_2_OBUF (E<2>)
    ----------------------------------------
    Total                     16.307ns (5.972ns logic, 10.335ns route)
                                       (36.6% logic, 63.4% route)

==========================================================================

Cross Clock Domains Report:
--------------------------


==========================================================================


Total REAL time to Xst completion: 14.00 secs
Total CPU time to Xst completion: 13.56 secs

-->


Total memory usage is 474616 kilobytes

Number of errors   :    0 (   0 filtered)
Number of warnings :    4 (   0 filtered)
Number of infos    :    0 (   0 filtered)
```

2. map report

```
Release 14.7 Map P.20131013 (lin64)
Xilinx Mapping Report File for Design 'FPCVT'

Design Information
------------------
Command Line   : map -intstyle ise -p xc6slx4-csg225-3 -w -logic_opt off -ol
high -t 1 -xt 0 -register_duplication off -r 4 -global_opt off -mt off -ir off
-pr off -lc off -power off -o FPCVT_map.ncd FPCVT.ngd FPCVT.pcf
Target Device  : xc6slx4
Target Package : csg225
Target Speed   : -3
Mapper Version : spartan6 -- $Revision: 1.55 $
Mapped Date    : Sun May  3 07:22:07 2020

Design Summary
--------------
Number of errors:      0
Number of warnings:    0
Slice Logic Utilization:
  Number of Slice Registers:                     0 out of   4,800    0%
  Number of Slice LUTs:                         55 out of   2,400    2%
    Number used as logic:                       55 out of   2,400    2%
      Number using O6 output only:              40
      Number using O5 output only:              12
      Number using O5 and O6:                    3
      Number used as ROM:                        0
    Number used as Memory:                       0 out of   1,200    0%

Slice Logic Distribution:
  Number of occupied Slices:                    23 out of     600    3%
  Number of MUXCYs used:                        16 out of   1,200    1%
  Number of LUT Flip Flop pairs used:           55
    Number with an unused Flip Flop:            55 out of      55  100%
    Number with an unused LUT:                   0 out of      55    0%
    Number of fully used LUT-FF pairs:           0 out of      55    0%
    Number of slice register sites lost
      to control set restrictions:               0 out of   4,800    0%

  A LUT Flip Flop pair for this architecture represents one LUT paired with
  one Flip Flop within a slice.  A control set is a unique combination of
  clock, reset, set, and enable signals for a registered element.
  The Slice Logic Distribution report is not meaningful if the design is
  over-mapped for a non-slice resource or if Placement fails.

IO Utilization:
  Number of bonded IOBs:                        22 out of     132   16%

Specific Feature Utilization:
  Number of RAMB16BWERs:                         0 out of      12    0%
  Number of RAMB8BWERs:                          0 out of      24    0%
  Number of BUFIO2/BUFIO2_2CLKs:                 0 out of      32    0%
```

```
  Number of BUFIO2FB/BUFIO2FB_2CLKs:             0 out of      32    0%
  Number of BUFG/BUFGMUXs:                       0 out of      16    0%
  Number of DCM/DCM_CLKGENs:                     0 out of       4    0%
  Number of ILOGIC2/ISERDES2s:                   0 out of     200    0%
  Number of IODELAY2/IODRP2/IODRP2_MCBs:         0 out of     200    0%
  Number of OLOGIC2/OSERDES2s:                   0 out of     200    0%
  Number of BSCANs:                              0 out of       4    0%
  Number of BUFHs:                               0 out of     128    0%
  Number of BUFPLLs:                             0 out of       8    0%
  Number of BUFPLL_MCBs:                         0 out of       4    0%
  Number of DSP48A1s:                            0 out of       8    0%
  Number of ICAPs:                               0 out of       1    0%
  Number of PCILOGICSEs:                         0 out of       2    0%
  Number of PLL_ADVs:                            0 out of       2    0%
  Number of PMVs:                                0 out of       1    0%
  Number of STARTUPs:                            0 out of       1    0%
  Number of SUSPEND_SYNCs:                       0 out of       1    0%

Average Fanout of Non-Clock Nets:                3.28

Peak Memory Usage:  735 MB
Total REAL time to MAP completion:  15 secs
Total CPU time to MAP completion:   14 secs

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Section 1 - Errors
------------------

Section 2 - Warnings
--------------------

Section 3 - Informational
-------------------------
INFO:MapLib:562 - No environment variables are currently set.
INFO:LIT:244 - All of the single ended outputs in this design are using slew
   rate limited output drivers. The delay on speed critical single ended outputs
   can be dramatically reduced by designating them as fast outputs.
INFO:Pack:1716 - Initializing temperature to 85.000 Celsius. (default - Range:
   0.000 to 85.000 Celsius)
```

INFO:Pack:1720 - Initializing voltage to 1.140 Volts. (default - Range: 1.140 to
   1.260 Volts)
INFO:Map:215 - The Interim Design Summary has been generated in the MAP Report
   (.mrp).
INFO:Pack:1650 - Map created a placed design.

Section 4 - Removed Logic Summary
----
   2 block(s) optimized away

Section 5 - Removed Logic

Optimized Block(s):
TYPE   BLOCK
GND   XST_GND
VCC   XST_VCC

To enable printing of redundant blocks removed and signals merged, set the
detailed map report option and rerun map.

Section 6 - IOB Properties

IOB Name	Type	Direction	IO Standard	Diff	Drive	Slew	Reg (s)	Resistor	IOB		Term	Strength	Rate			Delay
D<0>	IOB	INPUT	LVCMOS25							
D<1>	IOB	INPUT	LVCMOS25							
D<2>	IOB	INPUT	LVCMOS25							
D<3>	IOB	INPUT	LVCMOS25							
D<4>	IOB	INPUT	LVCMOS25							
D<5>	IOB	INPUT	LVCMOS25							
D<6>	IOB	INPUT	LVCMOS25							
D<7>	IOB	INPUT	LVCMOS25							
D<8>	IOB	INPUT	LVCMOS25							
D<9>	IOB	INPUT	LVCMOS25							

D<10>				IOB	INPUT	LVCMOS25
D<11>				IOB	INPUT	LVCMOS25
D<12>				IOB	INPUT	LVCMOS25
E<0>	12	SLOW		IOB	OUTPUT	LVCMOS25
E<1>	12	SLOW		IOB	OUTPUT	LVCMOS25
E<2>	12	SLOW		IOB	OUTPUT	LVCMOS25
F<0>	12	SLOW		IOB	OUTPUT	LVCMOS25
F<1>	12	SLOW		IOB	OUTPUT	LVCMOS25
F<2>	12	SLOW		IOB	OUTPUT	LVCMOS25
F<3>	12	SLOW		IOB	OUTPUT	LVCMOS25
F<4>	12	SLOW		IOB	OUTPUT	LVCMOS25
S	12	SLOW		IOB	OUTPUT	LVCMOS25

Section 7 - RPMs

Section 8 - Guide Report

Guide not run on this design.

Section 9 - Area Group and Partition Summary

Partition Implementation Status

  No Partitions were found in this design.

Area Group Information

  No area groups were found in this design.

Section 10 - Timing Report

A logic-level (pre-route) timing report can be generated by using Xilinx static

timing analysis tools, Timing Analyzer (GUI) or TRCE (command line), with the mapped NCD and PCF files. Please note that this timing report will be generated using estimated delay information. For accurate numbers, please generate a timing report with the post Place and Route NCD file.

For more information about the Timing Analyzer, consult the Xilinx Timing Analyzer Reference Manual; for more information about TRCE, consult the Xilinx Command Line Tools User Guide "TRACE" chapter.

Section 11 - Configuration String Details

Use the "-detail" map option to print out Configuration Strings

Section 12 - Control Set Information

Use the "-detail" map option to print out Control Set Information.

Section 13 - Utilization by Hierarchy

Use the "-detail" map option to print out the Utilization by Hierarchy section.

3. Place and Route Report

Release 14.7 par P.20131013 (lin64)

localhost.localdomain:: Sun May 03 07:22:27 2020

par -w -intstyle ise -ol high -mt off FPCVT_map.ncd FPCVT.ncd FPCVT.pcf

Constraints file: FPCVT.pcf.
Loading device for application Rf_Device from file '6slx4.nph' in environment /opt/Xilinx/14.7/ISE_DS/ISE/.
   "FPCVT" is an NCD, version 3.2, device xc6slx4, package csg225, speed -3

Initializing temperature to 85.000 Celsius. (default - Range: 0.000 to 85.000 Celsius)
Initializing voltage to 1.140 Volts. (default - Range: 1.140 to 1.260 Volts)

INFO:Par:282 - No user timing constraints were detected or you have set the option to ignore timing constraints ("par
   -x"). Place and Route will run in "Performance Evaluation Mode" to automatically improve the performance of all
   internal clocks in this design. Because there are not defined timing requirements, a timing score will not be
   reported in the PAR report in this mode. The PAR timing summary will list the performance achieved for each clock.
   Note: For the fastest runtime, set the effort level to "std". For best performance, set the effort level to "high".

Device speed data version: "PRODUCTION 1.23 2013-10-13".

Device Utilization Summary:

Slice Logic Utilization:				
Number of Slice Registers:	0	out of	4,800	0%
Number of Slice LUTs:	55	out of	2,400	2%
Number used as logic:	55	out of	2,400	2%
Number using O6 output only:	40			
Number using O5 output only:	12			
Number using O5 and O6:	3			
Number used as ROM:	0			
Number used as Memory:	0	out of	1,200	0%
Slice Logic Distribution:				
Number of occupied Slices:	23	out of	600	3%
Number of MUXCYs used:	16	out of	1,200	1%
Number of LUT Flip Flop pairs used:	55			
Number with an unused Flip Flop:	55	out of	55	100%
Number with an unused LUT:	0	out of	55	0%
Number of fully used LUT-FF pairs:	0	out of	55	0%
Number of slice register sites lost to control set restrictions:	0	out of	4,800	0%

A LUT Flip Flop pair for this architecture represents one LUT paired with one Flip Flop within a slice. A control set is a unique combination of clock, reset, set, and enable signals for a registered element.
The Slice Logic Distribution report is not meaningful if the design is over-mapped for a non-slice resource or if Placement fails.

IO Utilization:				
Number of bonded IOBs:	22	out of	132	16%
Specific Feature Utilization:				
Number of RAMB16BWERs:	0	out of	12	0%
Number of RAMB8BWERs:	0	out of	24	0%
Number of BUFIO2/BUFIO2_2CLKs:	0	out of	32	0%
Number of BUFIO2FB/BUFIO2FB_2CLKs:	0	out of	32	0%
Number of BUFG/BUFGMUXs:	0	out of	16	0%
Number of DCM/DCM_CLKGENs:	0	out of	4	0%
Number of ILOGIC2/ISERDES2s:	0	out of	200	0%
Number of IODELAY2/IODRP2/IODRP2_MCBs:	0	out of	200	0%
Number of OLOGIC2/OSERDES2s:	0	out of	200	0%
Number of BSCANs:	0	out of	4	0%
Number of BUFHs:	0	out of	128	0%
Number of BUFPLLs:	0	out of	8	0%
Number of BUFPLL_MCBs:	0	out of	4	0%
Number of DSP48A1s:	0	out of	8	0%
Number of ICAPs:	0	out of	1	0%
Number of PCILOGICSEs:	0	out of	2	0%
Number of PLL_ADVs:	0	out of	2	0%
Number of PMVs:	0	out of	1	0%
Number of STARTUPs:	0	out of	1	0%
Number of SUSPEND_SYNCs:	0	out of	1	0%

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Overall effort level (-ol):   High
Router effort level (-rl):    High

Starting initial Timing Analysis.  REAL time: 8 secs
Finished initial Timing Analysis.  REAL time: 8 secs

Starting Router


Phase  1  : 258 unrouted;      REAL time: 8 secs

Phase  2  : 243 unrouted;      REAL time: 8 secs

Phase  3  : 102 unrouted;      REAL time: 8 secs

Phase  4  : 102 unrouted; (Par is working to improve performance)     REAL time:
9 secs

Updating file: FPCVT.ncd with current fully routed design.

Phase  5  : 0 unrouted; (Par is working to improve performance)     REAL time:
9 secs

Phase  6  : 0 unrouted; (Par is working to improve performance)     REAL time:
9 secs

Phase  7  : 0 unrouted; (Par is working to improve performance)     REAL time:
9 secs

Phase  8  : 0 unrouted; (Par is working to improve performance)     REAL time:
9 secs

Phase  9  : 0 unrouted; (Par is working to improve performance)     REAL time:
9 secs

Phase 10  : 0 unrouted; (Par is working to improve performance)     REAL time:
9 secs
Total REAL time to Router completion: 9 secs
Total CPU time to Router completion: 9 secs

Partition Implementation Status
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  No Partitions were found in this design.

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Generating "PAR" statistics.
INFO:Par:459 - The Clock Report is not displayed in the non timing-driven mode.
Timing Score: 0 (Setup: 0, Hold: 0)
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Generating Pad Report.

All signals are completely routed.

Total REAL time to PAR completion: 10 secs
Total CPU time to PAR completion: 9 secs

Peak Memory Usage:  596 MB

Placer: Placement generated during map.
Routing: Completed - No errors found.

Number of error messages: 0
Number of warning messages: 0
Number of info messages: 2

Writing design to file FPCVT.ncd


PAR done!
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4. Conclusion

This project consists of one major module and three minor modules, and the major module chains the three minor modules together to complete the process of turning a 13-bit two's complement number to a 9-bit floating point. The crucial part of the project is splitting the process into multiple parts and use a minor module to implement that part. I had some difficulty in coming up with the hand-drawn schematics since the logic of some of the modules is rather complicated. To solve this problem, I look at each of the module and try to simply the logic until I could translate them into a combination of circuit components.