CSM152A Project5 Report

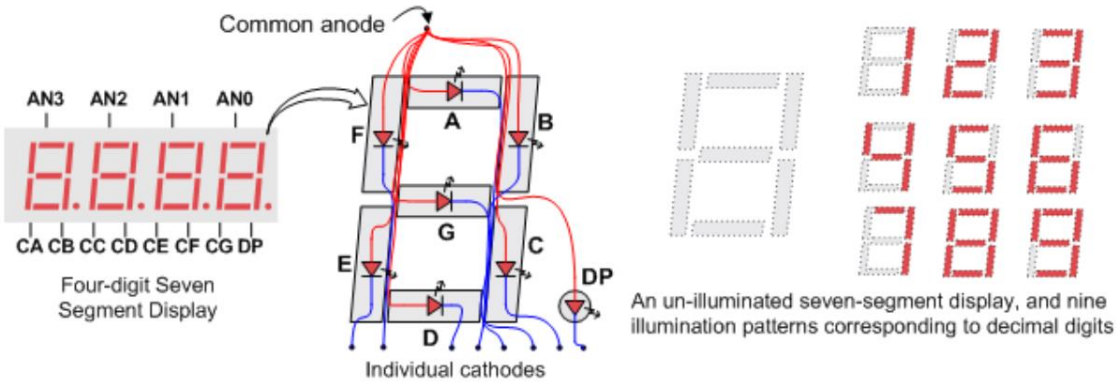
1. Introduction and Requirement

For this lab, we use Xilinx ISE software to design and test a parking meter that simulates the coins being added and display the time remaining.

The input to the parking meter is illustrated in the following table:

Inputs	Function
add1	add 60 seconds
add2	add 120 seconds
add3	add 180 seconds
add4	add 300 seconds
rst1	reset time to 16 seconds
rst2	reset time to 150 seconds
clk	frequency of 100 Hz
rst	resets to the initial state

The time remaining is displayed using 4 seven segment displays. Since the seven-segment display is not available, the parking meter module will output the signals for those four seven segment displays, which are 4 anodes a1, a2, a3, a4, and a seven-segment vector led_seg. The following picture illustrates the structure of the 4 seven segment displays.



In addition, the display has the following features:

In the initial state, the seven-segment displays should be flashing 0000 with period of 1 sec.

When less than 180 seconds remain, the display should flash with a period of 2 seconds, and even values would be displayed, and odd values would be blanked out. When time expires it should have the same behavior as the initial state.

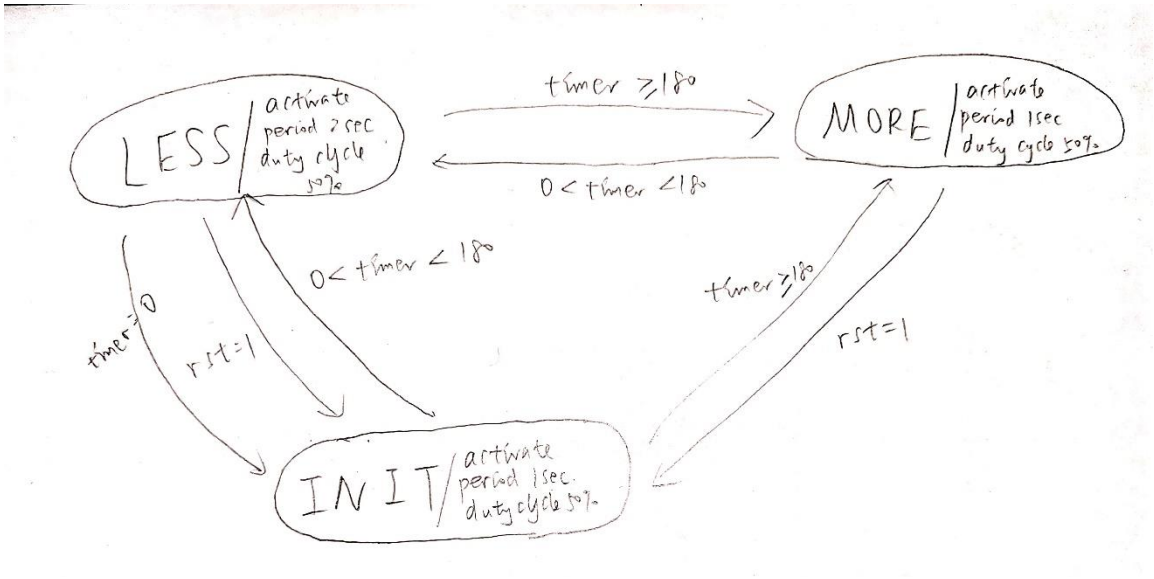
When more than 180 seconds remaining, the display should flash with a period of 1 second.

All the duty cycles are 50%, and the max time remaining should be 9999 seconds.

2. Design description

Basic Description of Design:

To implement the parking meter, it is necessary to use the idea of Finite State Machine. Below is a hand-drawn state diagram (it is a Moore Machine).



There are three states in this FSM:

- INIT: The state of the FSM after rst = 1, or after the timer reaches 0.
- LESS: The state when there are between 0 and 180 seconds left.
- MORE: The state when there are more than 180 seconds left.

Modules:

1. parking_meter

    input add1,

    input add2,

    input add3,

    input add4,

    input rst1,

    input rst2,

    input clk,

    input rst,

    output [6:0] seg_vector,

    output a1,

    output a2,

    output a3,

    output a4,

    output [3:0] val1,

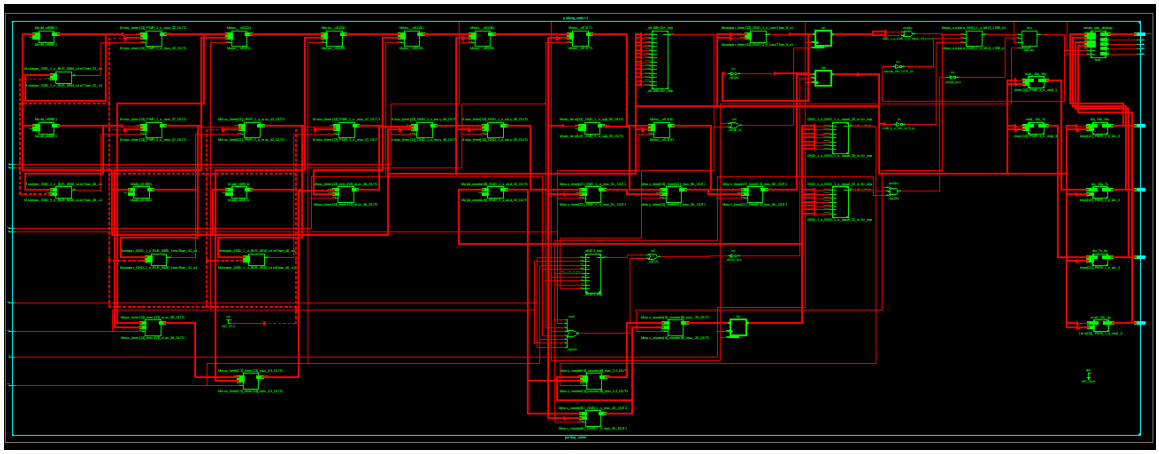
    output [3:0] val2,

    output [3:0] val3,

    output [3:0] val4

This is the main module with the specified input and output ports.

Schematics:



explanation: The schematics of the parking meter is rather complicated. Most of the circuit consists of registers or combinational logic (implemented using Multiplexer) for the timer, state, and the internal counter, which is use to implement a 1Hz clock, so that we can decrement the timer every 1 second.

2. seven_seg_display

input [3:0] time1,

input [3:0] time2,

input [3:0] time3,

input [3:0] time4,

input activate,

input clk,

output reg [6:0] seg_vector,

output reg a1,

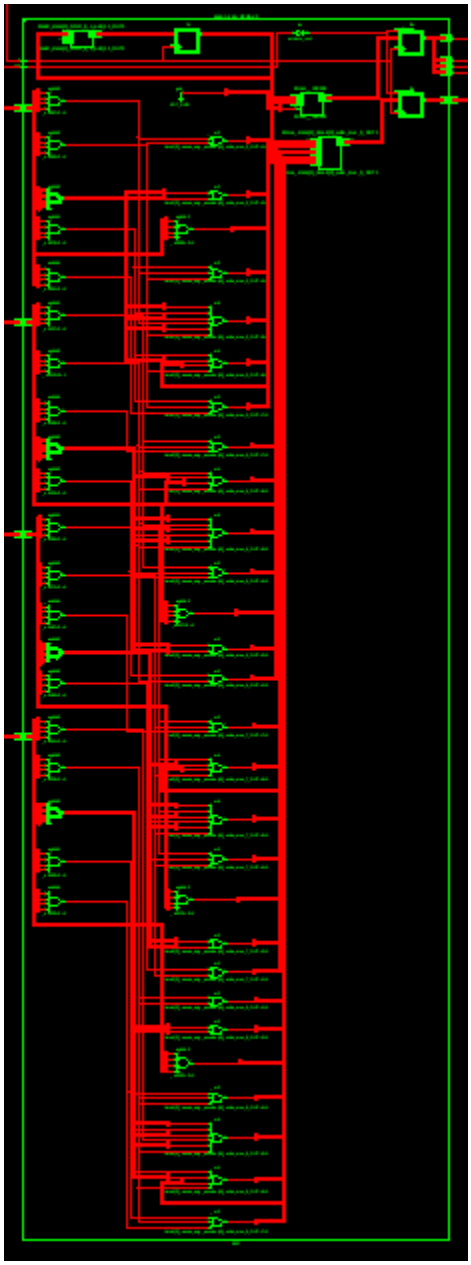
output reg a2,

output reg a3,

output reg a4

The functionality of this submodule is to transform 4 digit time from the main module to seven segment vector and 4 anode values.

Schematics:



explanation: Again, this schematics is pretty complicated, but I can see the circuit consists mostly of AND and OR gate, and this agrees with my Verilog code since the function of this submodule is to produce seven segment vector and four anodes from the input of 4 digit timer.

Design Summary of Synthesis and Implementation (map) report:

```
================================================================================
*                            Design Summary                                    *
================================================================================

Top Level Output File Name         : parking_meter.ngc

Primitive and Black Box Usage:
------------------------------
# BELS                             : 706
#      GND                         : 1
#      INV                         : 29
#      LUT1                        : 25
#      LUT2                        : 15
#      LUT3                        : 26
#      LUT4                        : 46
#      LUT5                        : 117
#      LUT6                        : 309
#      MUXCY                       : 60
#      MUXF7                       : 15
#      VCC                         : 1
#      XORCY                       : 62
# FlipFlops/Latches                : 54
#      FD                          : 6
#      FDE                         : 31
#      FDR                         : 9
#      FDRE                        : 1
#      FDS                         : 7
# Clock Buffers                    : 1
#      BUFGP                       : 1
# IO Buffers                       : 34
#      IBUF                        : 7
#      OBUF                        : 27

Device utilization summary:
---------------------------

Selected Device : 6slx4csg225-3


Slice Logic Utilization:
 Number of Slice Registers:              54  out of   4800     1%
 Number of Slice LUTs:                  567  out of   2400    23%
    Number used as Logic:               567  out of   2400    23%

Slice Logic Distribution:
 Number of LUT Flip Flop pairs used:    587
   Number with an unused Flip Flop:     533  out of    587    90%
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   Number with an unused LUT:            20  out of    587     3%
   Number of fully used LUT-FF pairs:    34  out of    587     5%
   Number of unique control sets:         6

IO Utilization:
 Number of IOs:                          35
 Number of bonded IOBs:                  35  out of    132    26%

Specific Feature Utilization:
 Number of BUFG/BUFGCTRLs:                1  out of     16     6%

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Partition Resource Summary:
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  No Partitions were found in this design.

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=================================================================================
Timing Report

NOTE: THESE TIMING NUMBERS ARE ONLY A SYNTHESIS ESTIMATE.
      FOR ACCURATE TIMING INFORMATION PLEASE REFER TO THE TRACE REPORT
      GENERATED AFTER PLACE-and-ROUTE.

Clock Information:
------------------
-----------------------------------+------------------------+-------+
Clock Signal                       | Clock buffer(FF name)  | Load  |
-----------------------------------+------------------------+-------+
clk                                | BUFGP                  | 54    |
-----------------------------------+------------------------+-------+

Asynchronous Control Signals Information:
----------------------------------------
No asynchronous control signals found in this design

Timing Summary:
---------------
Speed Grade: -3

   Minimum period: 16.340ns (Maximum Frequency: 61.201MHz)
   Minimum input arrival time before clock: 5.779ns
   Maximum output required time after clock: 17.683ns
   Maximum combinational path delay: No path found

Timing Details:
---------------
All values displayed in nanoseconds (ns)
```

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================================================================================
Timing constraint: Default period analysis for Clock 'clk'
  Clock period: 16.340ns (frequency: 61.201MHz)
  Total number of paths / destination ports: 102931253 / 95
--------------------------------------------------------------------------------
Delay:               16.340ns (Levels of Logic = 14)
  Source:            timer_9_1 (FF)
  Destination:       ssd/seg_vector_3 (FF)
  Source Clock:      clk rising
  Destination Clock: clk rising

  Data Path: timer_9_1 to ssd/seg_vector_3
                                Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     FDE:C->Q              8   0.447   1.147  timer_9_1 (timer_9_1)
     LUT6:I1->O            9   0.203   1.174
timer[13]_PWR_1_o_mod_3/Mmux_a[10]_a[13]_MUX_1067_o12
(timer[13]_PWR_1_o_mod_3/Madd_a[13]_GND_5_o_add_19_OUT_lut<10>)
     LUT6:I1->O           17   0.203   1.028
timer[13]_PWR_1_o_mod_3/BUS_0010_INV_873_o1
(timer[13]_PWR_1_o_mod_3/BUS_0010_INV_873_o1)
     LUT6:I5->O           12   0.205   1.013
timer[13]_PWR_1_o_mod_3/Mmux_a[11]_a[13]_MUX_1080_o11
(timer[13]_PWR_1_o_mod_3/a[11]_a[13]_MUX_1080_o)
     LUT6:I4->O            5   0.203   0.962
timer[13]_PWR_1_o_mod_3/BUS_0012_INV_903_o14
(timer[13]_PWR_1_o_mod_3/BUS_0012_INV_903_o13)
     LUT5:I1->O           17   0.203   1.028
timer[13]_PWR_1_o_mod_3/BUS_0012_INV_903_o15
(timer[13]_PWR_1_o_mod_3/BUS_0012_INV_903_o)
     LUT6:I5->O            7   0.205   0.878
timer[13]_PWR_1_o_mod_3/Mmux_a[13]_a[13]_MUX_1106_o1
(timer[13]_PWR_1_o_mod_3/a[13]_a[13]_MUX_1106_o)
     LUT6:I4->O           17   0.203   1.028
timer[13]_PWR_1_o_mod_3/BUS_0013_INV_918_o1
(timer[13]_PWR_1_o_mod_3/BUS_0013_INV_918_o)
     LUT6:I5->O            7   0.205   0.878
timer[13]_PWR_1_o_mod_3/Mmux_a[0]_a[13]_MUX_1133_o16
(timer[13]_PWR_1_o_mod_3/Madd_a[13]_GND_5_o_add_27_OUT_lut<6>)
     LUT6:I4->O            4   0.203   0.684
timer[13]_PWR_1_o_mod_3/BUS_0014_INV_933_o1
(timer[13]_PWR_1_o_mod_3/BUS_0014_INV_933_o)
     LUT6:I5->O            4   0.205   0.684
timer[13]_PWR_1_o_mod_3/Mmux_a[0]_a[13]_MUX_1147_o15
(timer[13]_PWR_1_o_mod_3/Madd_a[13]_GND_5_o_add_29_OUT_Madd_lut<5>)
     LUT6:I5->O            2   0.205   0.721  timer[13]_PWR_1_o_mod_3/Mmux_o41
(timer[13]_PWR_1_o_mod_3_OUT<3>)
     LUT5:I3->O            8   0.203   1.031  timer[13]_PWR_1_o_div_4/o<1>1
(val3_1_OBUF)
```

```
     LUT6:I3->O            1   0.205   0.684
ssd/Mmux_state[1]_time4[3]_wide_mux_9_OUT43
(ssd/Mmux_state[1]_time4[3]_wide_mux_9_OUT42)
     LUT6:I4->O            1   0.203   0.000
ssd/Mmux_state[1]_time4[3]_wide_mux_9_OUT46
(ssd/state[1]_time4[3]_wide_mux_9_OUT<3>)
     FDS:D                     0.102          ssd/seg_vector_3
    ----------------------------------------
    Total                     16.340ns (3.403ns logic, 12.937ns route)
                                       (20.8% logic, 79.2% route)

=========================================================================
Timing constraint: Default OFFSET IN BEFORE for Clock 'clk'
  Total number of paths / destination ports: 448 / 72
-------------------------------------------------------------------------
Offset:              5.779ns (Levels of Logic = 5)
  Source:            add3 (PAD)
  Destination:       timer_1 (FF)
  Destination Clock: clk rising

  Data Path: add3 to timer_1
                                Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     IBUF:I->O            14   1.222   1.302  add3_IBUF (add3_IBUF)
     LUT5:I0->O            7   0.203   0.878
Mmux_timer[13]_timer[13]_mux_56_OUT13111
(Mmux_timer[13]_timer[13]_mux_56_OUT1311)
     LUT3:I1->O            3   0.203   0.879
Mmux_timer[13]_timer[13]_mux_56_OUT7111
(Mmux_timer[13]_timer[13]_mux_56_OUT711)
     LUT6:I3->O            1   0.205   0.580
Mmux_timer[13]_timer[13]_mux_56_OUT61 (Mmux_timer[13]_timer[13]_mux_56_OUT6)
     LUT4:I3->O            1   0.205   0.000
Mmux_timer[13]_timer[13]_mux_56_OUT62 (timer[13]_timer[13]_mux_56_OUT<1>)
     FDE:D                     0.102          timer_1
    ----------------------------------------
    Total                     5.779ns (2.140ns logic, 3.639ns route)
                                       (37.0% logic, 63.0% route)

=========================================================================
Timing constraint: Default OFFSET OUT AFTER for Clock 'clk'
  Total number of paths / destination ports: 15575455 / 27
-------------------------------------------------------------------------
Offset:              17.683ns (Levels of Logic = 13)
  Source:            timer_9_1 (FF)
  Destination:       val3<2> (PAD)
  Source Clock:      clk rising

  Data Path: timer_9_1 to val3<2>
                                Gate     Net
```

```
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     FDE:C->Q              8   0.447   1.147  timer_9_1 (timer_9_1)
     LUT6:I1->O            9   0.203   1.174
timer[13]_PWR_1_o_mod_3/Mmux_a[10]_a[13]_MUX_1067_o12
(timer[13]_PWR_1_o_mod_3/Madd_a[13]_GND_5_o_add_19_OUT_lut<10>)
     LUT6:I1->O           17   0.203   1.028
timer[13]_PWR_1_o_mod_3/BUS_0010_INV_873_o1
(timer[13]_PWR_1_o_mod_3/BUS_0010_INV_873_o1)
     LUT6:I5->O           12   0.205   1.013
timer[13]_PWR_1_o_mod_3/Mmux_a[11]_a[13]_MUX_1080_o11
(timer[13]_PWR_1_o_mod_3/a[11]_a[13]_MUX_1080_o)
     LUT6:I4->O            5   0.203   0.962
timer[13]_PWR_1_o_mod_3/BUS_0012_INV_903_o14
(timer[13]_PWR_1_o_mod_3/BUS_0012_INV_903_o13)
     LUT5:I1->O           17   0.203   1.028
timer[13]_PWR_1_o_mod_3/BUS_0012_INV_903_o15
(timer[13]_PWR_1_o_mod_3/BUS_0012_INV_903_o)
     LUT6:I5->O            7   0.205   0.878
timer[13]_PWR_1_o_mod_3/Mmux_a[13]_a[13]_MUX_1106_o1
(timer[13]_PWR_1_o_mod_3/a[13]_a[13]_MUX_1106_o)
     LUT6:I4->O           17   0.203   1.028
timer[13]_PWR_1_o_mod_3/BUS_0013_INV_918_o1
(timer[13]_PWR_1_o_mod_3/BUS_0013_INV_918_o)
     LUT6:I5->O            7   0.205   0.878
timer[13]_PWR_1_o_mod_3/Mmux_a[0]_a[13]_MUX_1133_o16
(timer[13]_PWR_1_o_mod_3/Madd_a[13]_GND_5_o_add_27_OUT_lut<6>)
     LUT6:I4->O            4   0.203   0.684
timer[13]_PWR_1_o_mod_3/BUS_0014_INV_933_o1
(timer[13]_PWR_1_o_mod_3/BUS_0014_INV_933_o)
     LUT6:I5->O            7   0.205   0.774  timer[13]_PWR_1_o_mod_3/Mmux_o71
(timer[13]_PWR_1_o_mod_3_OUT<6>)
     LUT4:I3->O            1   0.205   0.827
timer[13]_PWR_1_o_div_4/o<2>1_SW0 (N714)
     LUT6:I2->O            8   0.203   0.802  timer[13]_PWR_1_o_div_4/o<2>1
(val3_2_OBUF)
     OBUF:I->O                 2.571          val3_2_OBUF (val3<2>)
    ----------------------------------------
    Total                     17.683ns (5.464ns logic, 12.219ns route)
                                       (30.9% logic, 69.1% route)

==========================================================================

Cross Clock Domains Report:
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Clock to Setup on destination clock clk
---------------+---------+---------+---------+---------+
               | Src:Rise| Src:Fall| Src:Rise| Src:Fall|
Source Clock   |Dest:Rise|Dest:Rise|Dest:Fall|Dest:Fall|
---------------+---------+---------+---------+---------+
```

```
clk            |   16.340|         |         |         |
---------------+---------+---------+---------+---------+

=========================================================================


Total REAL time to Xst completion: 60.00 secs
Total CPU time to Xst completion: 52.41 secs

-->


Total memory usage is 493528 kilobytes

Number of errors   :    0 (   0 filtered)
Number of warnings :   12 (   0 filtered)
Number of infos    :    1 (   0 filtered)
```

Design Summary of map report:

```
Design Summary
--------------
Number of errors:      0
Number of warnings:    0
Slice Logic Utilization:
  Number of Slice Registers:                    57 out of   4,800    1%
    Number used as Flip Flops:                  54
    Number used as Latches:                      0
    Number used as Latch-thrus:                  0
    Number used as AND/OR logics:                3
  Number of Slice LUTs:                       547 out of   2,400   22%
    Number used as logic:                     545 out of   2,400   22%
      Number using O6 output only:            471
      Number using O5 output only:             25
      Number using O5 and O6:                  49
      Number used as ROM:                       0
    Number used as Memory:                      0 out of   1,200    0%
    Number used exclusively as route-thrus:     2
      Number with same-slice register load:     2
      Number with same-slice carry load:        0
      Number with other load:                   0

Slice Logic Distribution:
  Number of occupied Slices:                  182 out of     600   30%
  Number of MUXCYs used:                       64 out of   1,200    5%
  Number of LUT Flip Flop pairs used:         555
    Number with an unused Flip Flop:          503 out of     555   90%
    Number with an unused LUT:                  8 out of     555    1%
    Number of fully used LUT-FF pairs:         44 out of     555    7%
    Number of unique control sets:              6
```

```
    Number of slice register sites lost
      to control set restrictions:              18 out of   4,800    1%

  A LUT Flip Flop pair for this architecture represents one LUT paired with
  one Flip Flop within a slice.  A control set is a unique combination of
  clock, reset, set, and enable signals for a registered element.
  The Slice Logic Distribution report is not meaningful if the design is
  over-mapped for a non-slice resource or if Placement fails.

IO Utilization:
  Number of bonded IOBs:                        35 out of     132   26%

Specific Feature Utilization:
  Number of RAMB16BWERs:                         0 out of      12    0%
  Number of RAMB8BWERs:                          0 out of      24    0%
  Number of BUFIO2/BUFIO2_2CLKs:                 0 out of      32    0%
  Number of BUFIO2FB/BUFIO2FB_2CLKs:             0 out of      32    0%
  Number of BUFG/BUFGMUXs:                       1 out of      16    6%
    Number used as BUFGs:                        1
    Number used as BUFGMUX:                      0
  Number of DCM/DCM_CLKGENs:                     0 out of       4    0%
  Number of ILOGIC2/ISERDES2s:                   0 out of     200    0%
  Number of IODELAY2/IODRP2/IODRP2_MCBs:         0 out of     200    0%
  Number of OLOGIC2/OSERDES2s:                   0 out of     200    0%
  Number of BSCANs:                              0 out of       4    0%
  Number of BUFHs:                               0 out of     128    0%
  Number of BUFPLLs:                             0 out of       8    0%
  Number of BUFPLL_MCBs:                         0 out of       4    0%
  Number of DSP48A1s:                            0 out of       8    0%
  Number of ICAPs:                               0 out of       1    0%
  Number of PCILOGICSEs:                         0 out of       2    0%
  Number of PLL_ADVs:                            0 out of       2    0%
  Number of PMVs:                                0 out of       1    0%
  Number of STARTUPs:                            0 out of       1    0%
  Number of SUSPEND_SYNCs:                       0 out of       1    0%

Average Fanout of Non-Clock Nets:                4.61

Peak Memory Usage:  745 MB
Total REAL time to MAP completion:  55 secs
Total CPU time to MAP completion:   52 secs
```

<u>conclusions drawn from these reports:</u>

There is a large number of slice registers used and 54 of 57 are used as flip-flops. This means that the many parts of the synthesized circuit is sequential, and this agrees with my Verilog code since in the module there are multiple counters that changes value upon positive edge of the clock.

3. Simulation documentation

simulation efforts:

The testbench for the parking meter module has the following test cases:

1. at initial state, flash with 0000 with period 1 sec

2. check each add button and reset button

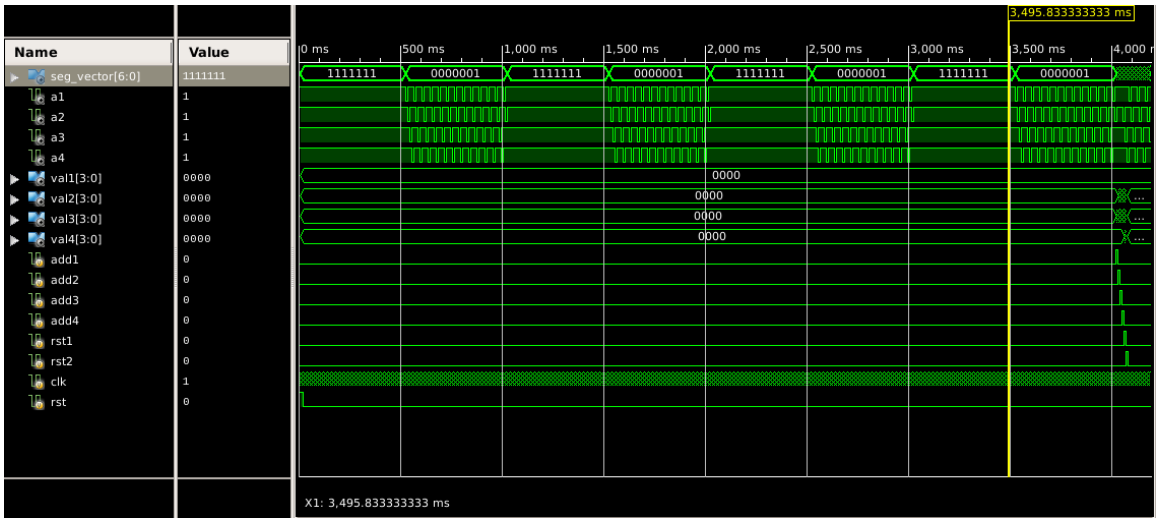
3. When less than 180 seconds, the display should flash with a period of 2 seconds

4. When more than 180 seconds, the display should flash with a period of 1 second

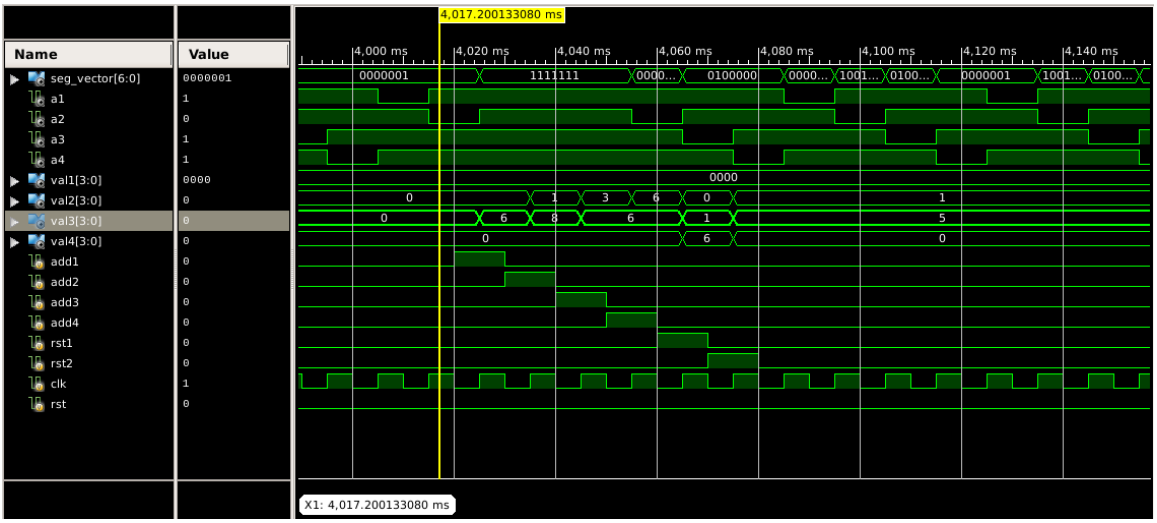
5. Timer will be 9999 when it goes beyond that value

simulation waveform:

1. at initial state, flash with 0000 with period 1 sec

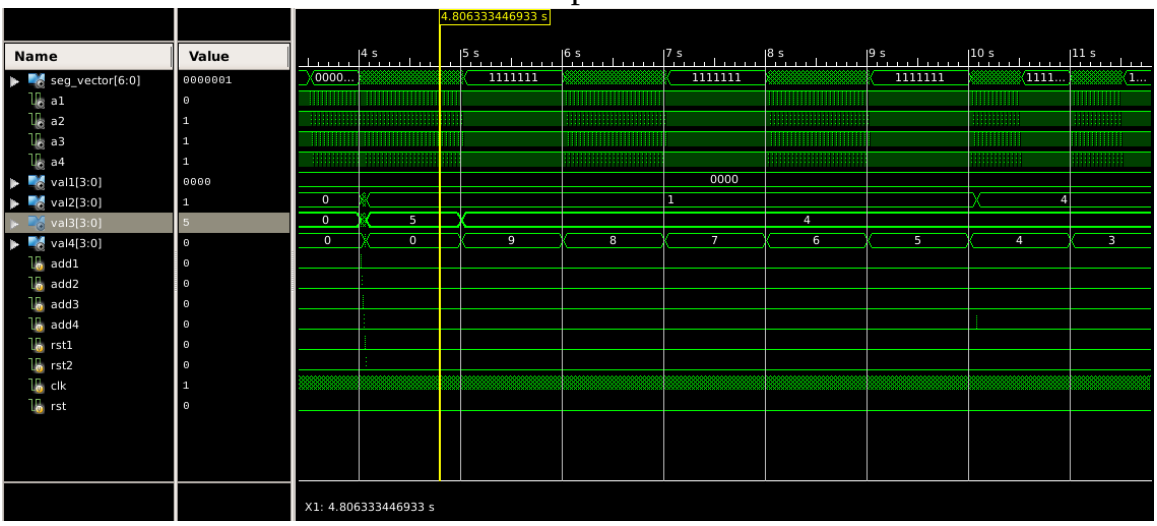


2. check each add button and reset button

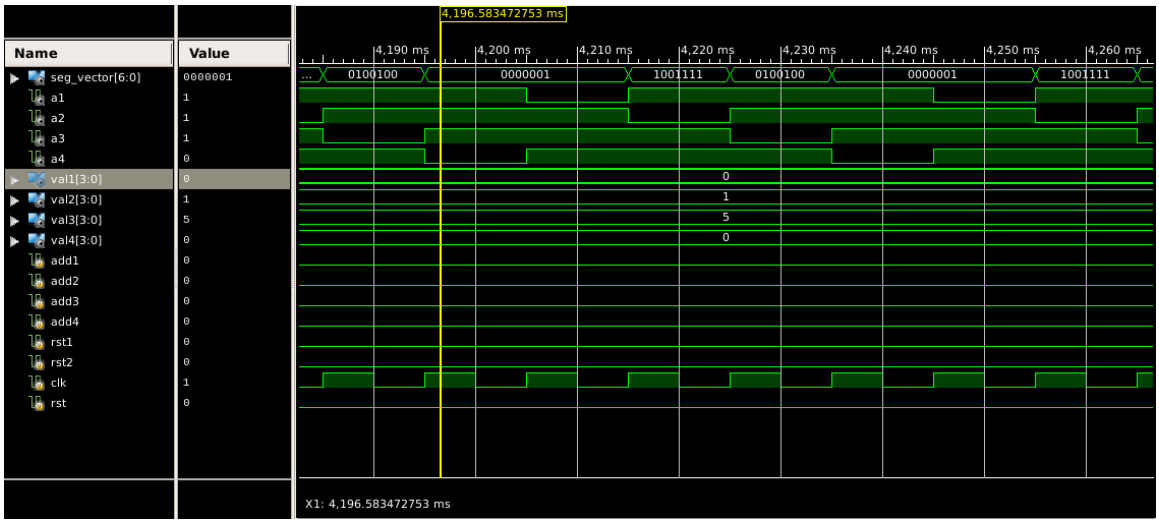


3. When less than 180 seconds, the display should flash with a period of 2 seconds

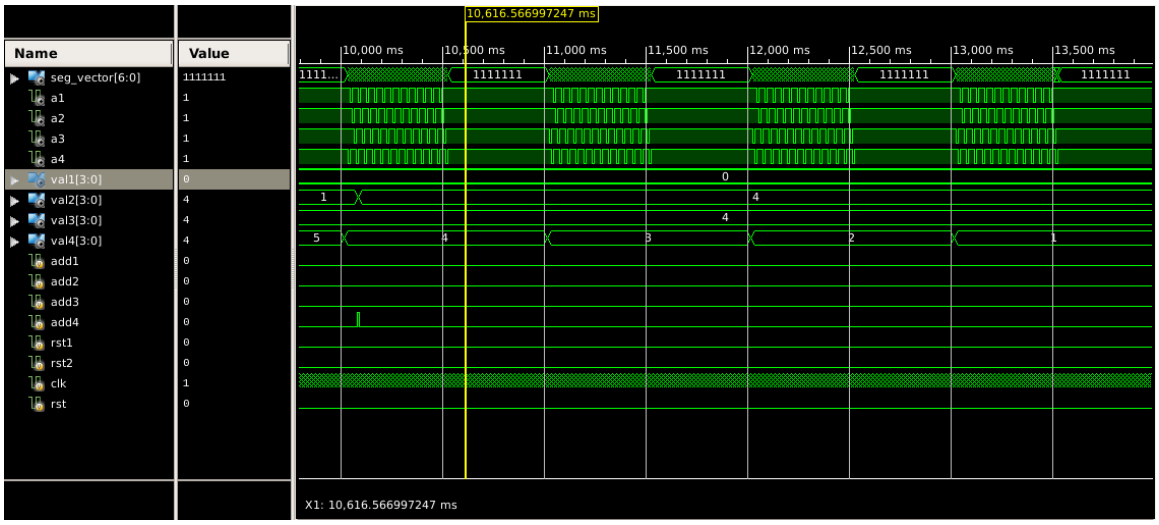
correct timer decrement / flash with a period of 2 seconds:



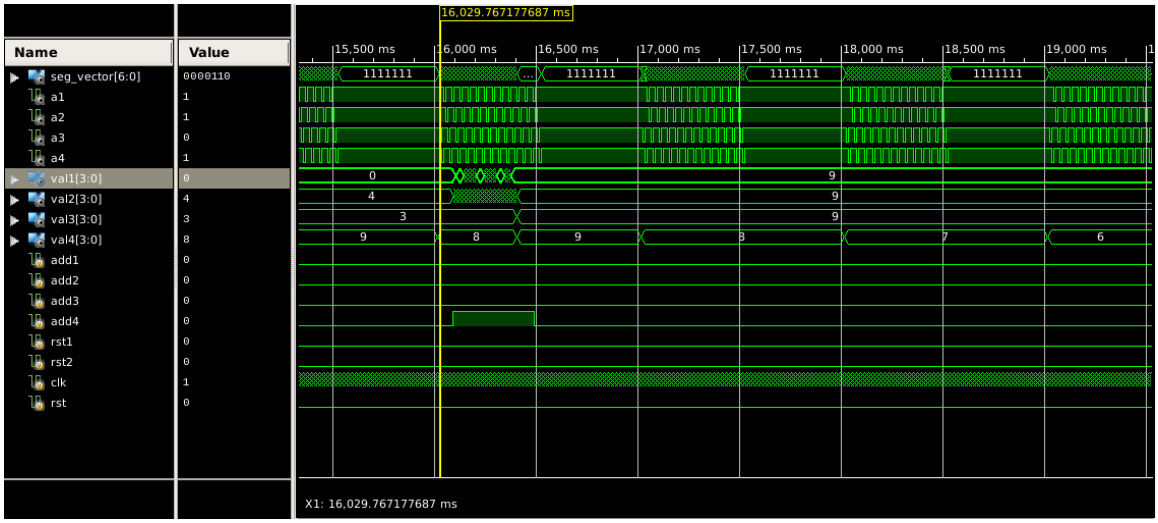
correct seg_vector display:



4. When more than 180 seconds, the display should flash with a period of 1 second



5. Timer will be 9999 when it goes beyond that value



4. Conclusion

In this project, we incorporate things we have learned in previous projects together: counter with specific duty cycle and finite state machine. The hard part of this project is to design the seven-segment display since I am not too familiar with how it is implemented. I also used function in my code, which is a convenient feature of Verilog to transform input into output using combinational logic. And unlike previous projects where the testbench usually runs for less than milliseconds, the time span of the testbench is in the magnitude of seconds, so we need to manually set the time the testbench runs in the Xilinx ISE software.