CSM152A Project3 Report

1. Introduction and requirement

For this lab, we use Xilinx ISE software to design and test various clock waveforms. There are four sections in this lab:

1. Clock Divider by Power of 2s

In this section, we will assign 4 1-bit wires to each of the bits from the 4-bit counter, and each wire works as a clock divider with different division ratio.

2. Even Division Clock Using Counters

In this section, we implement even division clock by flipping the counter according to the counter value.

3. Odd Division Clock Using Counters

In this section, firstly we design clock with a specific duty cycle, and using logical or we implement a 50% duty cycle divide-by-5 clock.

4. Pulse/Strobes

In this section we explore pulses/strobes which have very low duty cycle, and at last we implement a glitchy counter using input clock and a strobe.

2. Design description

Basic Description of Design:

Modules in these four different sections implements different clocks, and hence they are independent of each other. The *clock_gen* module uses modules from these four sections, and the testbench for the *clock_gen* module generates waveform produced by modules from these four different sections.

Modules:

1. clock_div_two

```
input clk_in,
input rst,
```

output clk_div_2,

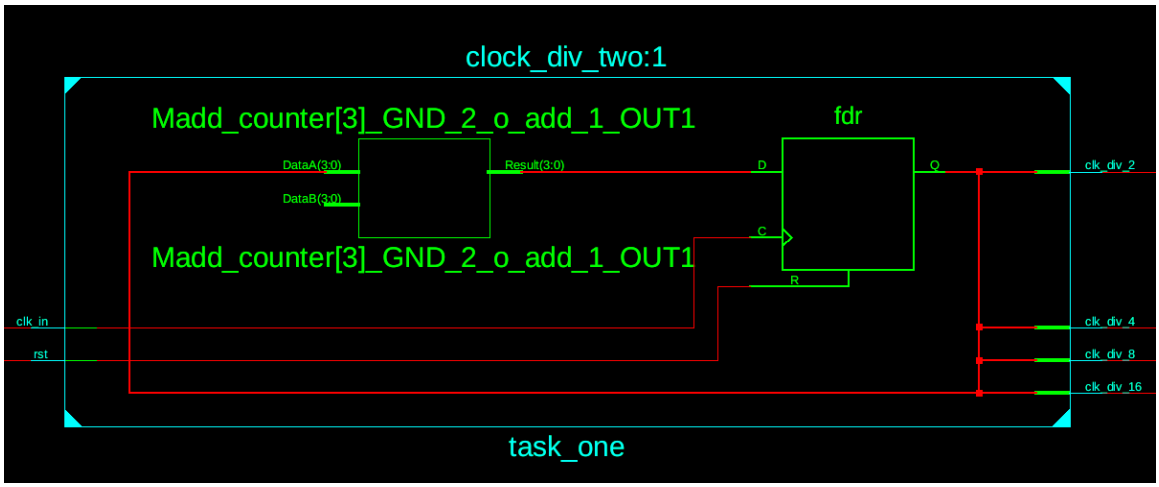
output clk_div_4,

output clk_div_8,

output clk_div_16

Design idea: This is a simple module that assigns four wires to each bit of the four bit counter.

Schematics:



explanation: This schematics simply show that four wires are attached to each of the bits of the 4-bit counter.

2. clock_div_twenty_eight

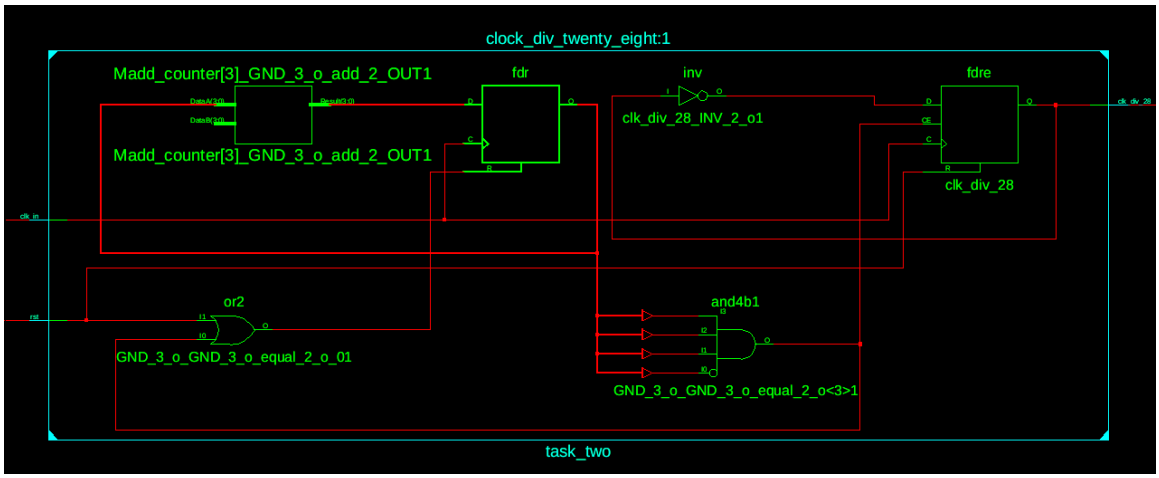
input clk_in,

input rst,

output reg clk_div_28

Design idea: This module uses a counter, and whenever the counter has value of 13, the counter is reset and the output clk_div_28 is flipped.

Schematics:



explanation: This schematics show that this module has a counter, and it uses some combinational logic to check the value of the counter, and uses the result to update the output signal, which is stored in the flip-flop on the right.

3. clock_div_five

    input clk_in,

    input rst,

    output clk_div_5

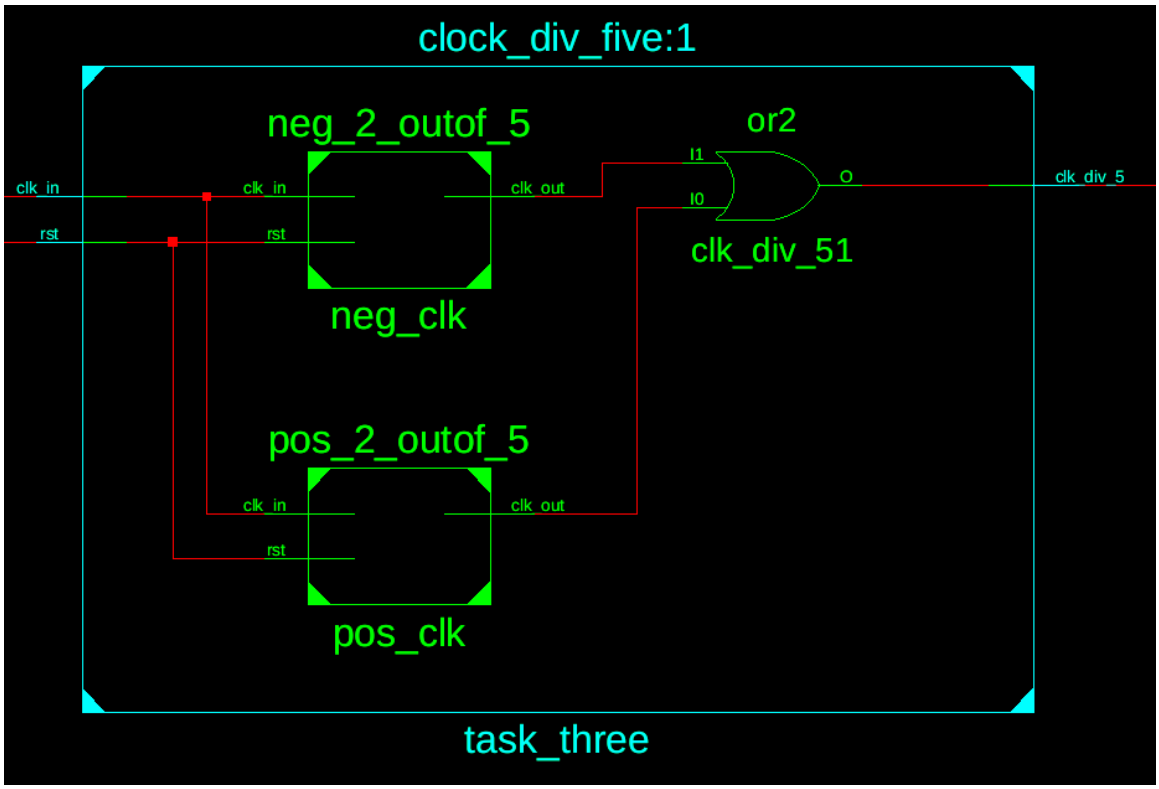
Design idea: This module uses two submodules:

1. 40% duty cycle divided-by-5 clock (always block triggers on posedge)

2. 40% duty cycle divided-by-5 clock (always block triggers on negedge)

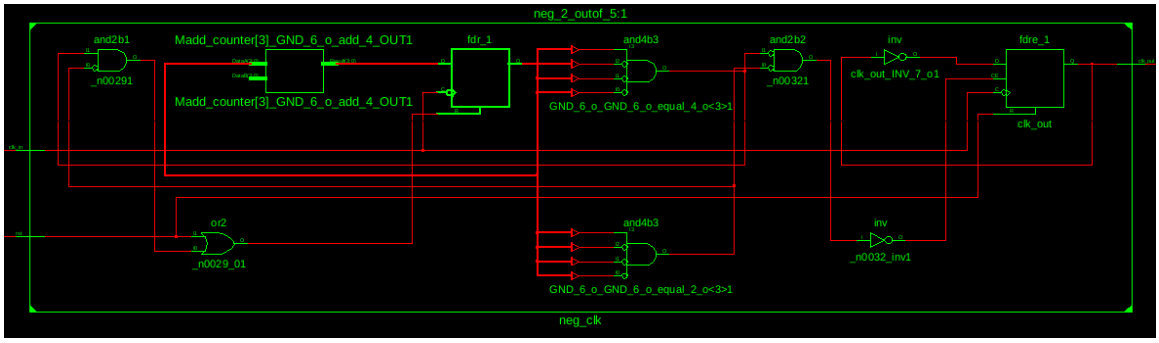
This module use the output clock from these two submodules and take the logical-or of the output. This creates a 50% duty cycle divide-by-5 clock.

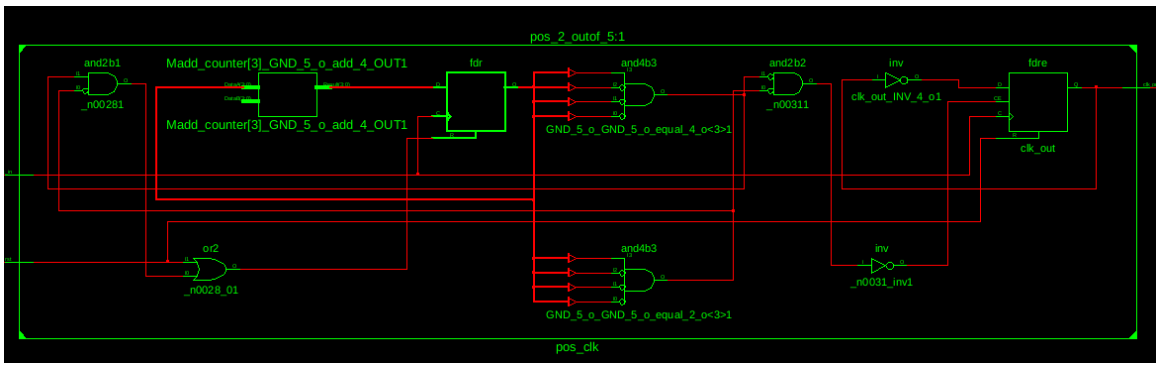
Schematics:



explanation: This is the same as what the design idea explained.

Schematics of submodules:





explanation: These two submodules have similar structures. They have a counter and use some combinational logic to determine when to invert the value stored in the flip-flop on the right.

4. clock_strobe

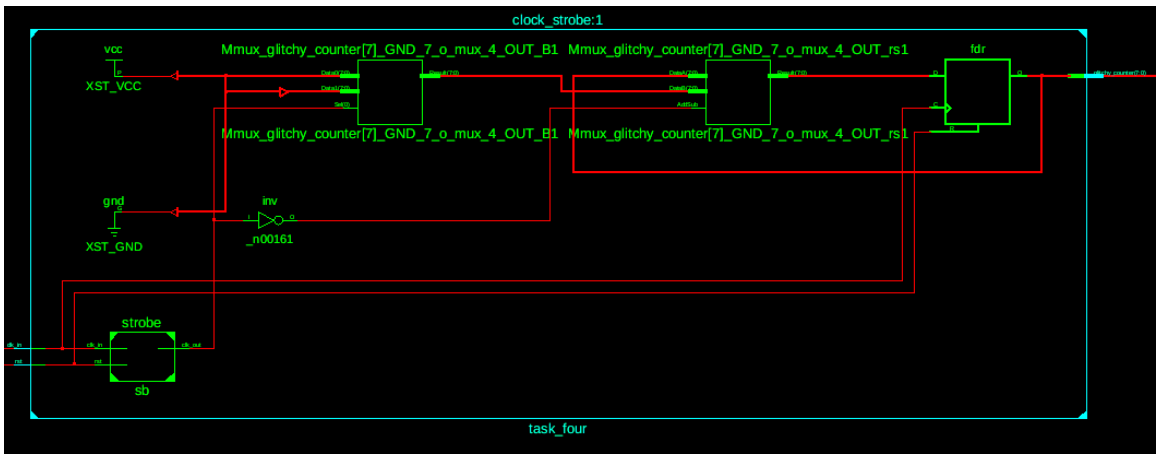
    input clk_in,

    input rst,

    output reg [7:0] glitchy_counter

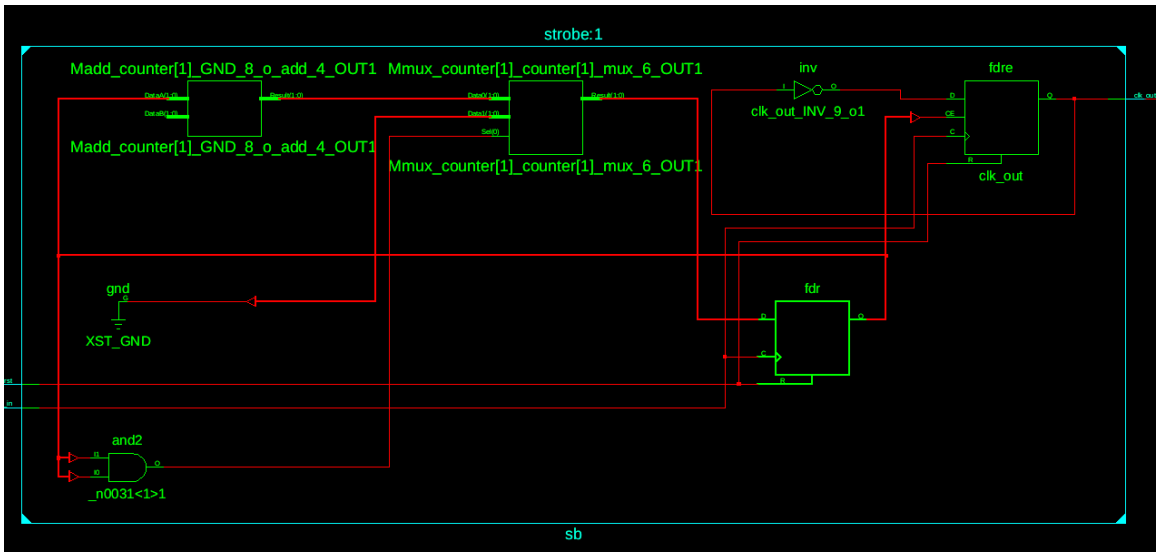
Design idea: This module uses a *strobe* submodule, which output a divide-by-4 25% duty cycle strobe clock, and at every positive edge of the input clock, if the strobe clock has value of 1, then decrease the counter by 5, otherwise increase the counter by 2.

Schematics:



explanation: This schematics uses multiplexer to implement the if statement and the select signal comes from the strobe.

Schematics of submodule:



explanation: This strobe is basically a 25% duty cycle divided-by-4 clock, hence it uses a counter and a mux to determine when to invert the output clock.

5. clock_gen

input clk_in,

input rst,

output clk_div_2,

output clk_div_4,

output clk_div_8,

output clk_div_16,

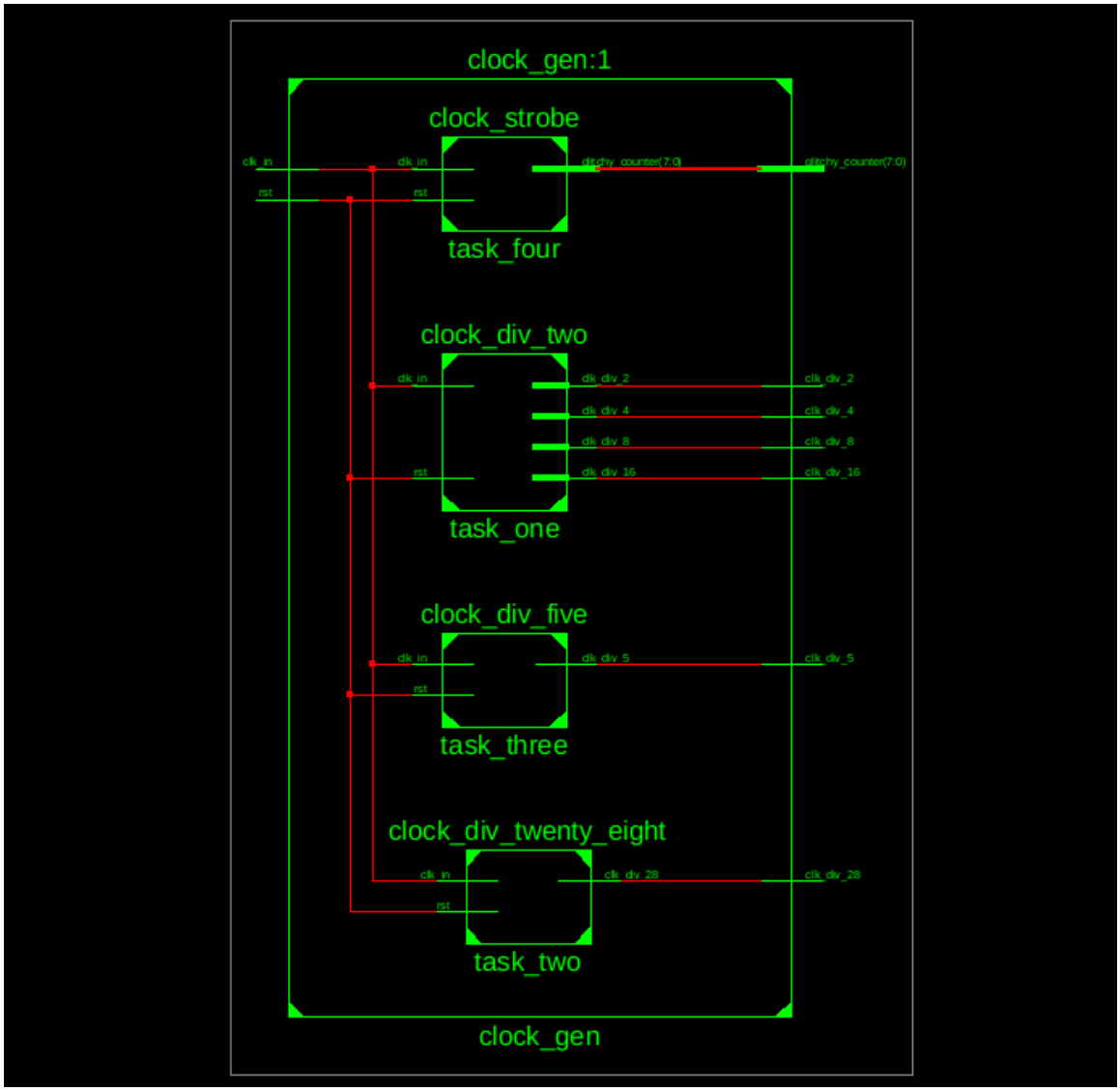
output clk_div_28,

output clk_div_5,

output [7:0] glitchy_counter

Design idea: This clock generator module is required by the spec, and it uses the above four modules and collect their output.

Schematics:



explanation: The clock_gen module uses the four modules and collect their output.

3. Simulation documentation

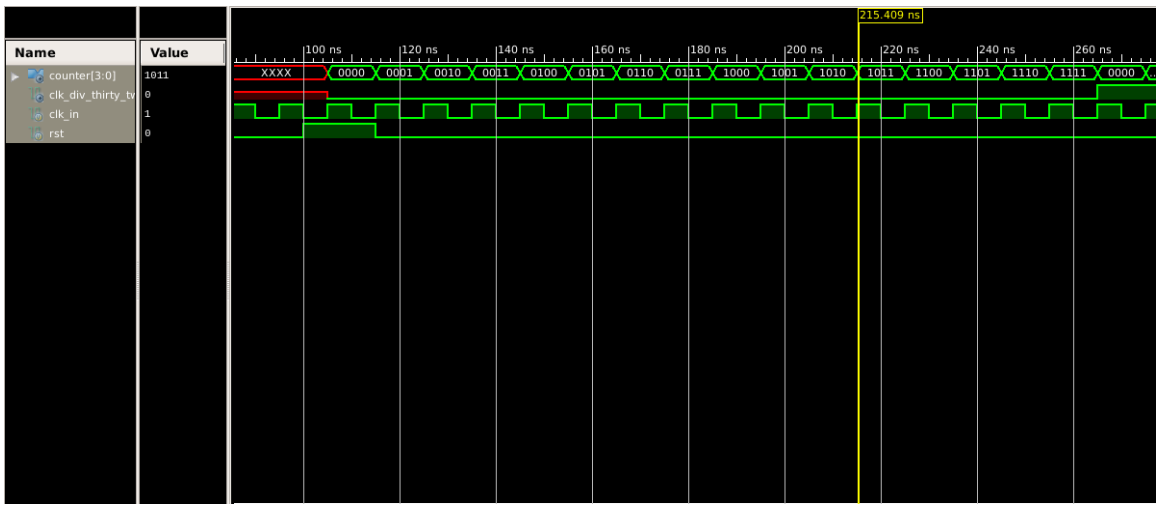
<u>simulation efforts:</u>

Below are 10 simulation waveforms in the order required by the project spec. They all use similar testbenches, which set the reset signal to 1 for 15ns, and then set the reset signal to 0 and run the testbench for 200 ns.

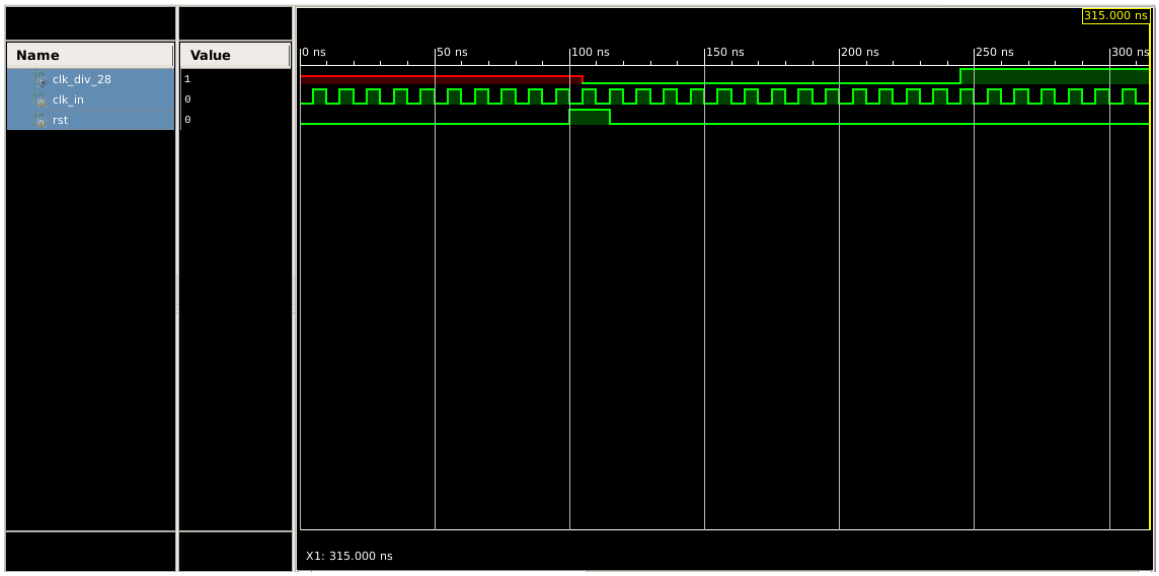
(1):


Name
Value
clk_div_2
clk_div_4
clk_div_8
clk_div_16
clk_in
rst
X
X
X
X
0
0
0.000 ns
0 ns
50 ns
100 ns
150 ns
200 ns
250 ns
300 ns
X1: 0.000 ns

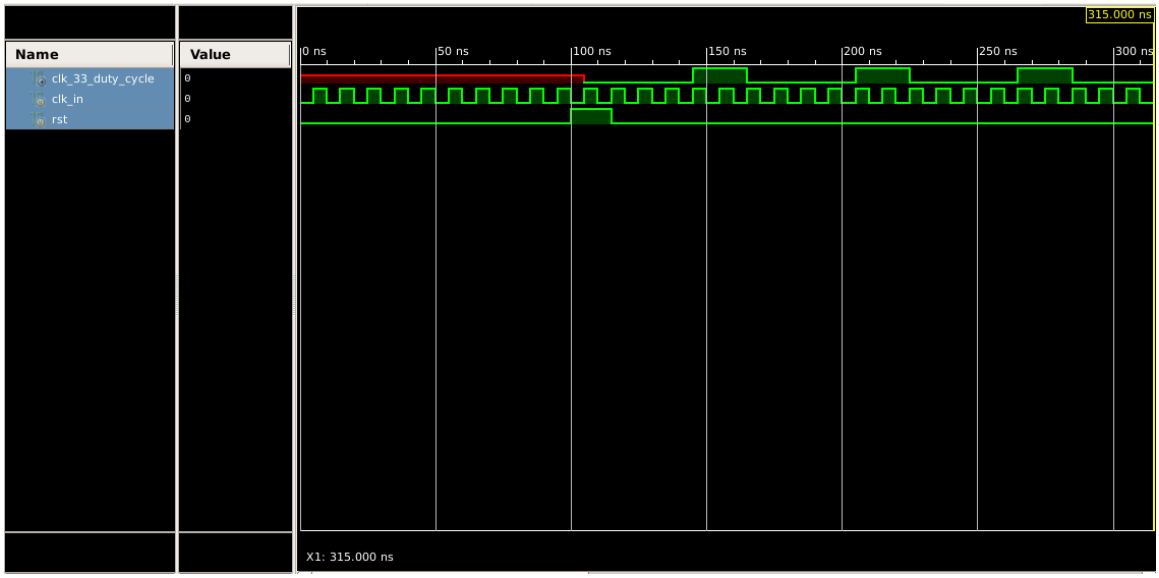
(2):


Name
Value
counter[3:0]
clk_div_thirty_tv
clk_in
rst
1011
0
1
0
215.409 ns
100 ns
120 ns
140 ns
160 ns
180 ns
200 ns
220 ns
240 ns
260 ns
XXXX
0000
0001
0010
0011
0100
0101
0110
0111
1000
1001
1010
1011
1100
1101
1110
1111
0000

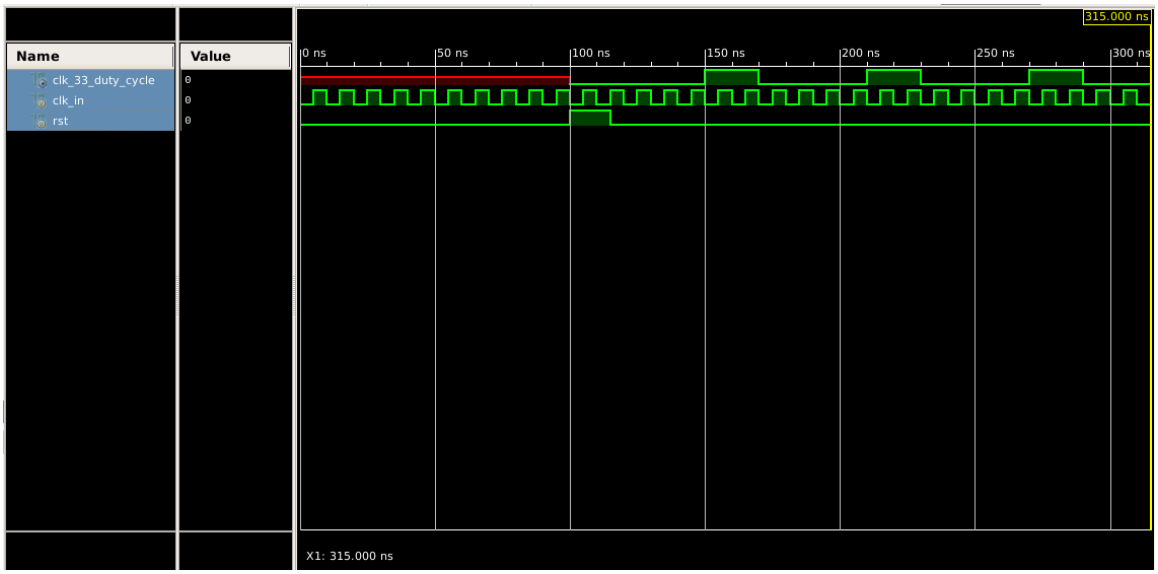
(3):


Name
Value
clk_div_28
clk_in
rst
1
0
0
315.000 ns
0 ns
50 ns
100 ns
150 ns
200 ns
250 ns
300 ns
X1: 315.000 ns

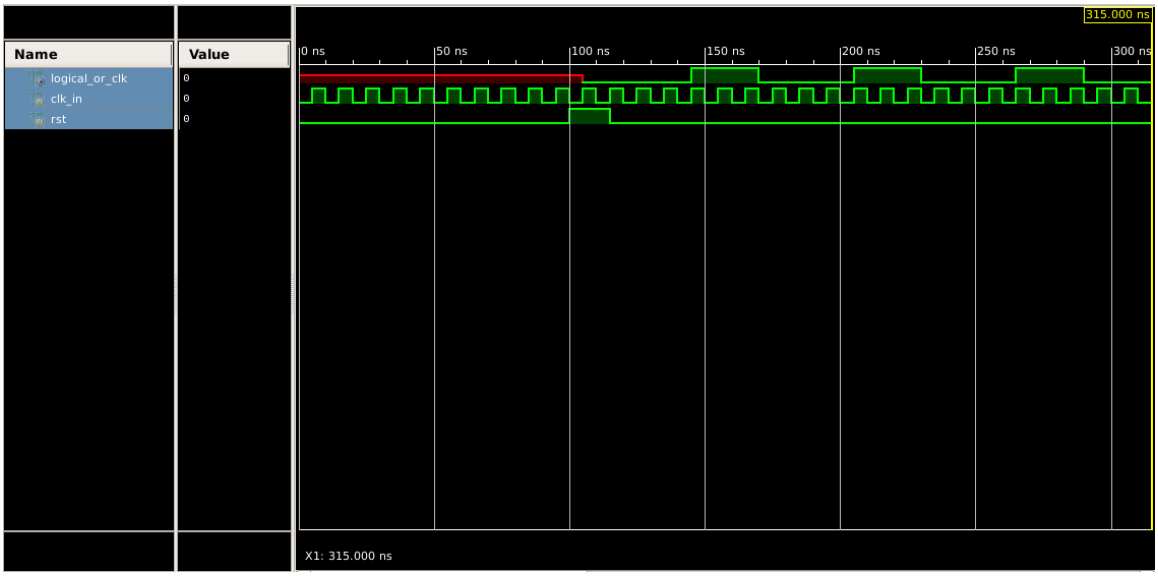
(4):


Name
Value
clk_33_duty_cycle
clk_in
rst
0
0
0
315.000 ns
0 ns
50 ns
100 ns
150 ns
200 ns
250 ns
300 ns
X1: 315.000 ns

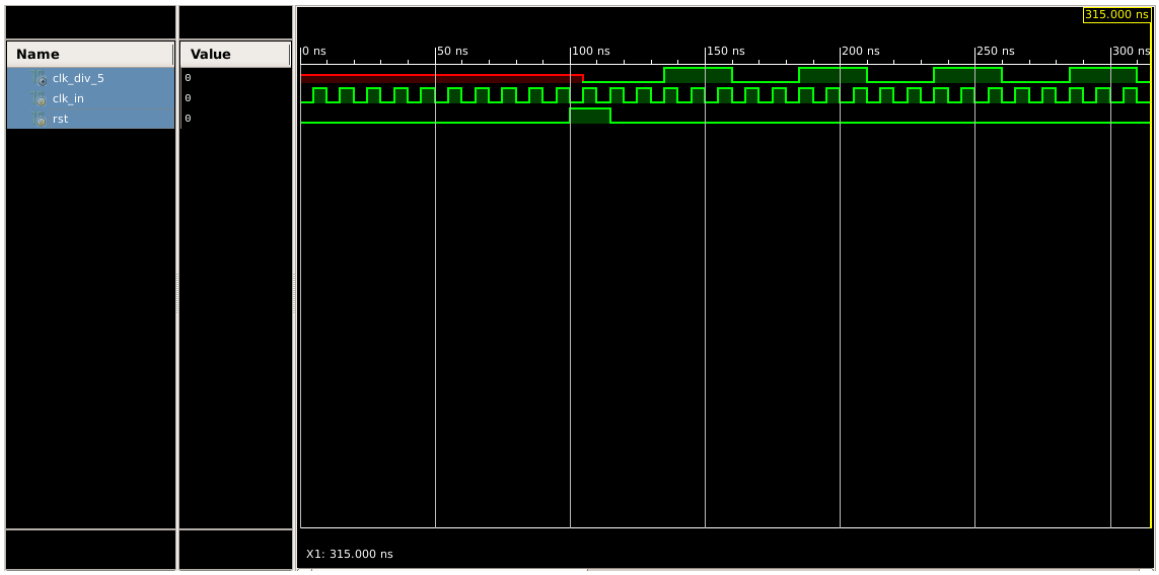
(5):


Name
Value
clk_33_duty_cycle
clk_in
rst
0
0
0
315.000 ns
0 ns
50 ns
100 ns
150 ns
200 ns
250 ns
300 ns
X1: 315.000 ns

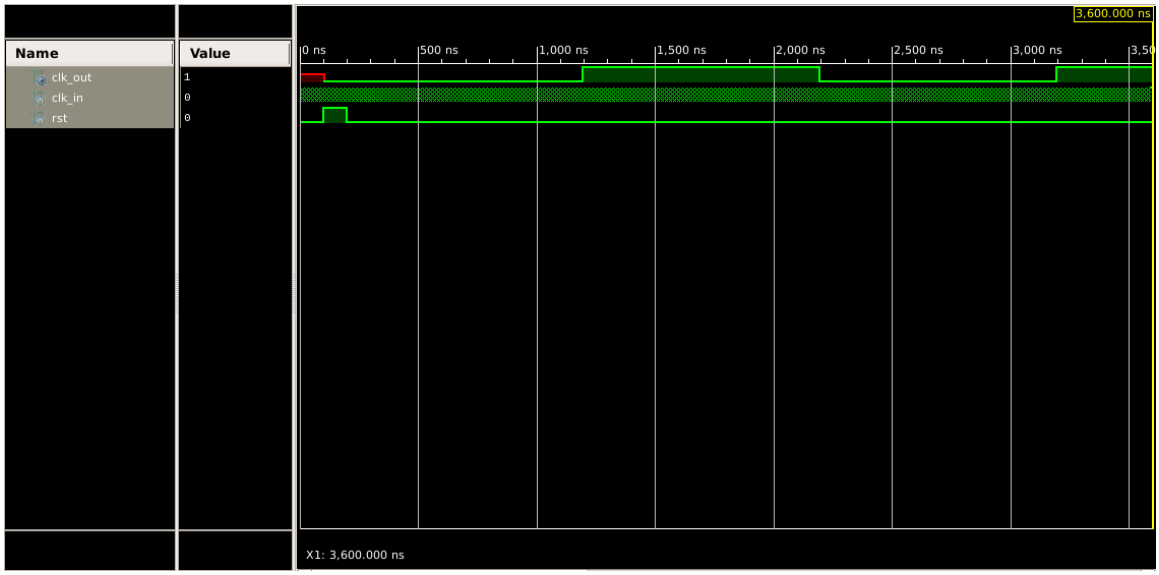
(6):


Name
Value
logical_or_clk
clk_in
rst
0
0
0
315.000 ns
0 ns
50 ns
100 ns
150 ns
200 ns
250 ns
300 ns
X1: 315.000 ns

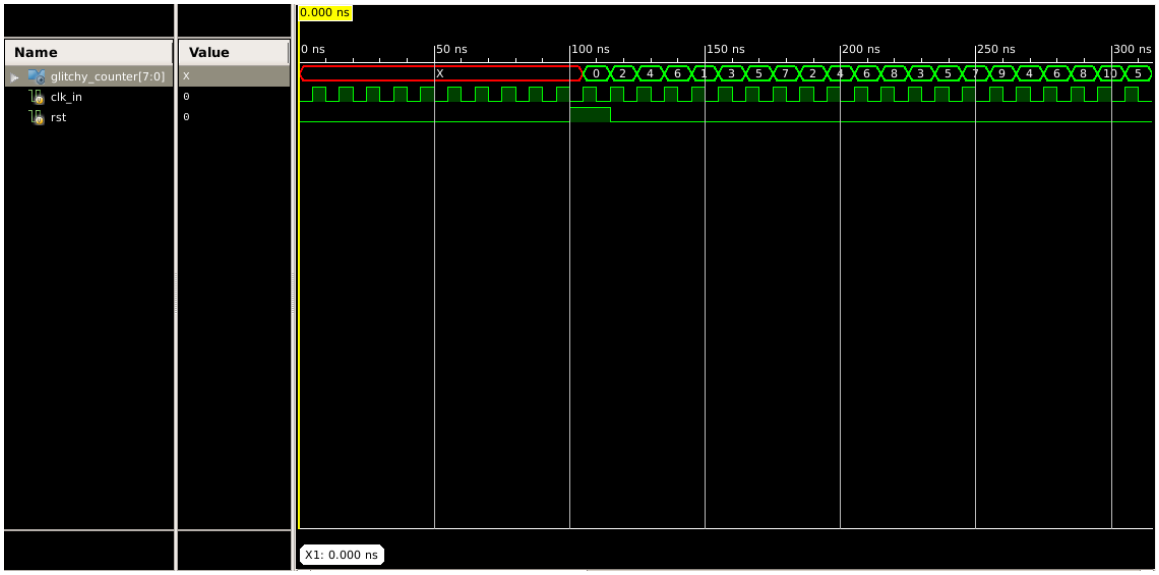
(7):


Name
Value
clk_div_5
clk_in
rst
0
0
0
315.000 ns
0 ns
50 ns
100 ns
150 ns
200 ns
250 ns
300 ns
X1: 315.000 ns

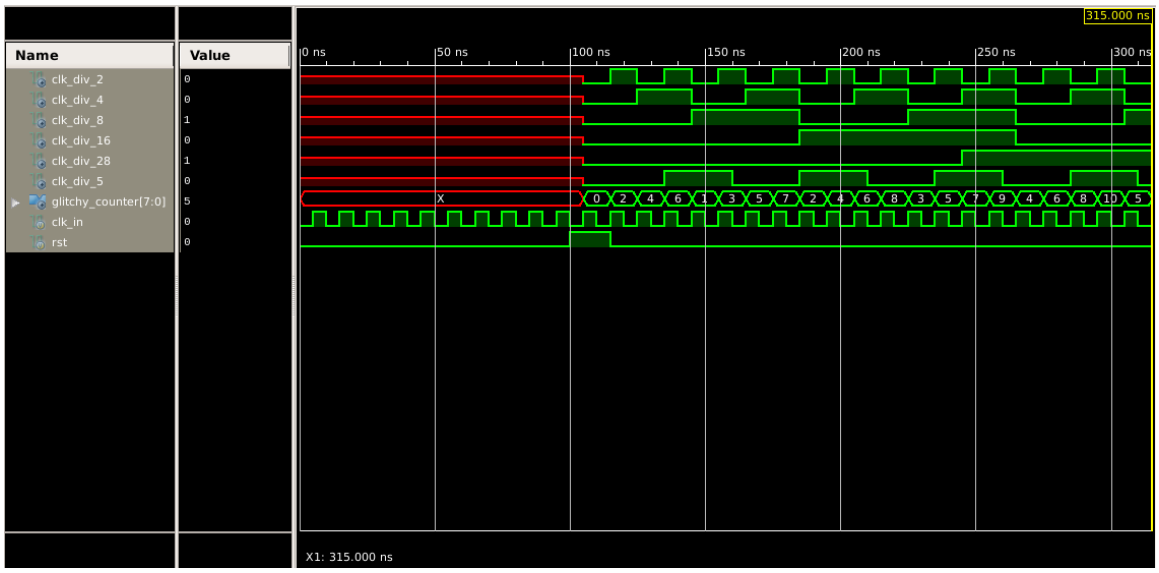
(8):


Name
Value
clk_out
clk_in
rst
1
0
0
3,600.000 ns
0 ns
500 ns
1,000 ns
1,500 ns
2,000 ns
2,500 ns
3,000 ns
X1: 3,600.000 ns

(9):



(10):



Relevant information in Synthesis & Implementation Report:

```
Synthesizing Unit <clock_gen>.
    Related source file is "/home/ise/Project3/clock_gen.v".
    Summary:
        no macro.
Unit <clock_gen> synthesized.

Synthesizing Unit <clock_div_two>.
    Related source file is "/home/ise/Project3/clock_gen.v".
    Found 4-bit register for signal <counter>.
    Found 4-bit adder for signal <counter[3]_GND_2_o_add_1_OUT> created at line 74.
```

```
    Summary:
       inferred   1 Adder/Subtractor(s).
       inferred   4 D-type flip-flop(s).
Unit <clock_div_two> synthesized.

Synthesizing Unit <clock_div_twenty_eight>.
    Related source file is "/home/ise/Project3/clock_gen.v".
    Found 1-bit register for signal <clk_div_28>.
    Found 4-bit register for signal <counter>.
    Found 4-bit adder for signal <counter[3]_GND_3_o_add_2_OUT> created at line 96.
    Summary:
       inferred   1 Adder/Subtractor(s).
       inferred   5 D-type flip-flop(s).
Unit <clock_div_twenty_eight> synthesized.

Synthesizing Unit <clock_div_five>.
    Related source file is "/home/ise/Project3/clock_gen.v".
    Summary:
       no macro.
Unit <clock_div_five> synthesized.

Synthesizing Unit <pos_2_outof_5>.
    Related source file is "/home/ise/Project3/clock_gen.v".
    Found 1-bit register for signal <clk_out>.
    Found 4-bit register for signal <counter>.
    Found 4-bit adder for signal <counter[3]_GND_5_o_add_4_OUT> created at line 143.
    Summary:
       inferred   1 Adder/Subtractor(s).
       inferred   5 D-type flip-flop(s).
Unit <pos_2_outof_5> synthesized.

Synthesizing Unit <neg_2_outof_5>.
    Related source file is "/home/ise/Project3/clock_gen.v".
    Found 1-bit register for signal <clk_out>.
    Found 4-bit register for signal <counter>.
    Found 4-bit adder for signal <counter[3]_GND_6_o_add_4_OUT> created at line 169.
    Summary:
       inferred   1 Adder/Subtractor(s).
       inferred   5 D-type flip-flop(s).
Unit <neg_2_outof_5> synthesized.

Synthesizing Unit <clock_strobe>.
    Related source file is "/home/ise/Project3/clock_gen.v".
    Found 8-bit register for signal <glitchy_counter>.
    Found 8-bit adder for signal <glitchy_counter[7]_GND_7_o_add_3_OUT> created at line
193.
    Found 8-bit subtractor for signal <GND_7_o_GND_7_o_sub_3_OUT<7:0>> created at line
191.
    Summary:
       inferred   1 Adder/Subtractor(s).
       inferred   8 D-type flip-flop(s).
       inferred   1 Multiplexer(s).
Unit <clock_strobe> synthesized.

Synthesizing Unit <strobe>.
    Related source file is "/home/ise/Project3/clock_gen.v".
    Found 1-bit register for signal <clk_out>.
```

```
    Found 2-bit register for signal <counter>.
    Found 2-bit adder for signal <counter[1]_GND_8_o_add_4_OUT> created at line 218.
    Summary:
        inferred   1 Adder/Subtractor(s).
        inferred   3 D-type flip-flop(s).
        inferred   1 Multiplexer(s).
Unit <strobe> synthesized.

=========================================================================
HDL Synthesis Report

Macro Statistics
# Adders/Subtractors                                   : 6
 2-bit adder                                           : 1
 4-bit adder                                           : 4
 8-bit addsub                                          : 1
# Registers                                            : 10
 1-bit register                                        : 4
 2-bit register                                        : 1
 4-bit register                                        : 4
 8-bit register                                        : 1
# Multiplexers                                         : 2
 2-bit 2-to-1 multiplexer                              : 1
 8-bit 2-to-1 multiplexer                              : 1
```

4. Conclusion

This project experiments different type of clocks and how to use counters to implement modules that outputs these clock signals. The tasks in this lab is straightforward since they are independent of each other. The important part of this lab is to understand exactly when we should flip the signal and reset the counter. For example, if we flip the signal when the counter is 3, the signal is actually flipped after four cycles are completed. In this lab, if I am not sure about how to flip the signal I usually just use the ‘trial and error’ method and uses the testbench to see what the result is.

```
=====================================================
SYNTHESIS REPORT
=====================================================
Release 14.7 - xst P.20131013 (lin64)
Copyright (c) 1995-2013 Xilinx, Inc.  All rights reserved.
-->
Parameter TMPDIR set to xst/projnav.tmp


Total REAL time to Xst completion: 1.00 secs
Total CPU time to Xst completion: 0.10 secs

-->
Parameter xsthdpdir set to xst


Total REAL time to Xst completion: 1.00 secs
Total CPU time to Xst completion: 0.10 secs

-->
Reading design: clock_gen.prj

TABLE OF CONTENTS
  1) Synthesis Options Summary
  2) HDL Parsing
  3) HDL Elaboration
  4) HDL Synthesis
       4.1) HDL Synthesis Report
  5) Advanced HDL Synthesis
       5.1) Advanced HDL Synthesis Report
  6) Low Level Synthesis
  7) Partition Report
  8) Design Summary
       8.1) Primitive and Black Box Usage
       8.2) Device utilization summary
       8.3) Partition Resource Summary
       8.4) Timing Report
            8.4.1) Clock Information
            8.4.2) Asynchronous Control Signals Information
            8.4.3) Timing Summary
            8.4.4) Timing Details
            8.4.5) Cross Clock Domains Report


=========================================================================
*                      Synthesis Options Summary                        *
=========================================================================
---- Source Parameters
Input File Name                    : "clock_gen.prj"
Ignore Synthesis Constraint File   : NO

---- Target Parameters
Output File Name                   : "clock_gen"
Output Format                      : NGC
Target Device                      : xc6slx4-3-csg225

---- Source Options
```

```
Top Module Name                    : clock_gen
Automatic FSM Extraction           : YES
FSM Encoding Algorithm             : Auto
Safe Implementation                : No
FSM Style                          : LUT
RAM Extraction                     : Yes
RAM Style                          : Auto
ROM Extraction                     : Yes
Shift Register Extraction          : YES
ROM Style                          : Auto
Resource Sharing                   : YES
Asynchronous To Synchronous        : NO
Shift Register Minimum Size        : 2
Use DSP Block                      : Auto
Automatic Register Balancing       : No

---- Target Options
LUT Combining                      : Auto
Reduce Control Sets                : Auto
Add IO Buffers                     : YES
Global Maximum Fanout              : 100000
Add Generic Clock Buffer(BUFG)     : 16
Register Duplication               : YES
Optimize Instantiated Primitives   : NO
Use Clock Enable                   : Auto
Use Synchronous Set                : Auto
Use Synchronous Reset              : Auto
Pack IO Registers into IOBs        : Auto
Equivalent register Removal        : YES

---- General Options
Optimization Goal                  : Speed
Optimization Effort                : 1
Power Reduction                    : NO
Keep Hierarchy                     : No
Netlist Hierarchy                  : As_Optimized
RTL Output                         : Yes
Global Optimization                : AllClockNets
Read Cores                         : YES
Write Timing Constraints           : NO
Cross Clock Analysis               : NO
Hierarchy Separator                : /
Bus Delimiter                      : <>
Case Specifier                     : Maintain
Slice Utilization Ratio            : 100
BRAM Utilization Ratio             : 100
DSP48 Utilization Ratio            : 100
Auto BRAM Packing                  : NO
Slice Utilization Ratio Delta      : 5

=========================================================================


=========================================================================
*                          HDL Parsing                                  *
=========================================================================
Analyzing Verilog file "/home/ise/Project3/clock_gen.v" into library work
```

```
Parsing module <clock_gen>.
Parsing module <clock_div_two>.
Parsing module <clock_div_twenty_eight>.
Parsing module <clock_div_five>.
Parsing module <pos_2_outof_5>.
Parsing module <neg_2_outof_5>.
Parsing module <clock_strobe>.
Parsing module <strobe>.

=========================================================================
*                           HDL Elaboration                             *
=========================================================================

Elaborating module <clock_gen>.

Elaborating module <clock_div_two>.
WARNING:HDLCompiler:413 - "/home/ise/Project3/clock_gen.v" Line 74: Result of 5-bit expression
is truncated to fit in 4-bit target.

Elaborating module <clock_div_twenty_eight>.

Elaborating module <clock_div_five>.

Elaborating module <pos_2_outof_5>.

Elaborating module <neg_2_outof_5>.

Elaborating module <clock_strobe>.

Elaborating module <strobe>.
WARNING:HDLCompiler:413 - "/home/ise/Project3/clock_gen.v" Line 191: Result of 32-bit
expression is truncated to fit in 8-bit target.
WARNING:HDLCompiler:413 - "/home/ise/Project3/clock_gen.v" Line 193: Result of 9-bit
expression is truncated to fit in 8-bit target.

=========================================================================
*                           HDL Synthesis                               *
=========================================================================

Synthesizing Unit <clock_gen>.
    Related source file is "/home/ise/Project3/clock_gen.v".
    Summary:
       no macro.
Unit <clock_gen> synthesized.

Synthesizing Unit <clock_div_two>.
    Related source file is "/home/ise/Project3/clock_gen.v".
    Found 4-bit register for signal <counter>.
    Found 4-bit adder for signal <counter[3]_GND_2_o_add_1_OUT> created at line 74.
    Summary:
       inferred   1 Adder/Subtractor(s).
       inferred   4 D-type flip-flop(s).
Unit <clock_div_two> synthesized.

Synthesizing Unit <clock_div_twenty_eight>.
    Related source file is "/home/ise/Project3/clock_gen.v".
    Found 1-bit register for signal <clk_div_28>.
```

```
    Found 4-bit register for signal <counter>.
    Found 4-bit adder for signal <counter[3]_GND_3_o_add_2_OUT> created at line 96.
    Summary:
       inferred   1 Adder/Subtractor(s).
       inferred   5 D-type flip-flop(s).
Unit <clock_div_twenty_eight> synthesized.

Synthesizing Unit <clock_div_five>.
    Related source file is "/home/ise/Project3/clock_gen.v".
    Summary:
       no macro.
Unit <clock_div_five> synthesized.

Synthesizing Unit <pos_2_outof_5>.
    Related source file is "/home/ise/Project3/clock_gen.v".
    Found 1-bit register for signal <clk_out>.
    Found 4-bit register for signal <counter>.
    Found 4-bit adder for signal <counter[3]_GND_5_o_add_4_OUT> created at line 143.
    Summary:
       inferred   1 Adder/Subtractor(s).
       inferred   5 D-type flip-flop(s).
Unit <pos_2_outof_5> synthesized.

Synthesizing Unit <neg_2_outof_5>.
    Related source file is "/home/ise/Project3/clock_gen.v".
    Found 1-bit register for signal <clk_out>.
    Found 4-bit register for signal <counter>.
    Found 4-bit adder for signal <counter[3]_GND_6_o_add_4_OUT> created at line 169.
    Summary:
       inferred   1 Adder/Subtractor(s).
       inferred   5 D-type flip-flop(s).
Unit <neg_2_outof_5> synthesized.

Synthesizing Unit <clock_strobe>.
    Related source file is "/home/ise/Project3/clock_gen.v".
    Found 8-bit register for signal <glitchy_counter>.
    Found 8-bit adder for signal <glitchy_counter[7]_GND_7_o_add_3_OUT> created at line 193.
    Found 8-bit subtractor for signal <GND_7_o_GND_7_o_sub_3_OUT<7:0>> created at line 191.
    Summary:
       inferred   1 Adder/Subtractor(s).
       inferred   8 D-type flip-flop(s).
       inferred   1 Multiplexer(s).
Unit <clock_strobe> synthesized.

Synthesizing Unit <strobe>.
    Related source file is "/home/ise/Project3/clock_gen.v".
    Found 1-bit register for signal <clk_out>.
    Found 2-bit register for signal <counter>.
    Found 2-bit adder for signal <counter[1]_GND_8_o_add_4_OUT> created at line 218.
    Summary:
       inferred   1 Adder/Subtractor(s).
       inferred   3 D-type flip-flop(s).
       inferred   1 Multiplexer(s).
Unit <strobe> synthesized.

=========================================================================
HDL Synthesis Report
```

```
Macro Statistics
# Adders/Subtractors                                   : 6
 2-bit adder                                           : 1
 4-bit adder                                           : 4
 8-bit addsub                                          : 1
# Registers                                            : 10
 1-bit register                                        : 4
 2-bit register                                        : 1
 4-bit register                                        : 4
 8-bit register                                        : 1
# Multiplexers                                         : 2
 2-bit 2-to-1 multiplexer                              : 1
 8-bit 2-to-1 multiplexer                              : 1

=========================================================================
INFO:Xst:1767 - HDL ADVISOR - Resource sharing has identified that some arithmetic operations
in this design can share the same physical resources for reduced device utilization. For
improved clock frequency you may try to disable resource sharing.

=========================================================================
*                       Advanced HDL Synthesis                          *
=========================================================================


Synthesizing (advanced) Unit <clock_div_twenty_eight>.
The following registers are absorbed into counter <counter>: 1 register on signal <counter>.
Unit <clock_div_twenty_eight> synthesized (advanced).

Synthesizing (advanced) Unit <clock_div_two>.
The following registers are absorbed into counter <counter>: 1 register on signal <counter>.
Unit <clock_div_two> synthesized (advanced).

Synthesizing (advanced) Unit <clock_strobe>.
The following registers are absorbed into accumulator <glitchy_counter>: 1 register on signal
<glitchy_counter>.
Unit <clock_strobe> synthesized (advanced).

Synthesizing (advanced) Unit <neg_2_outof_5>.
The following registers are absorbed into counter <counter>: 1 register on signal <counter>.
Unit <neg_2_outof_5> synthesized (advanced).

Synthesizing (advanced) Unit <pos_2_outof_5>.
The following registers are absorbed into counter <counter>: 1 register on signal <counter>.
Unit <pos_2_outof_5> synthesized (advanced).

=========================================================================
Advanced HDL Synthesis Report

Macro Statistics
# Adders/Subtractors                                   : 1
 2-bit adder                                           : 1
# Counters                                             : 4
 4-bit up counter                                      : 4
# Accumulators                                         : 1
 8-bit updown accumulator                              : 1
# Registers                                            : 6
```

```
 Flip-Flops                                        : 6

=========================================================================

=========================================================================
*                        Low Level Synthesis                            *
=========================================================================

Optimizing unit <clock_gen> ...
WARNING:Xst:1710 - FF/Latch <task_three/pos_clk/counter_3> (without init value) has a constant
value of 0 in block <clock_gen>. This FF/Latch will be trimmed during the optimization
process.
INFO:Xst:2261 - The FF/Latch <task_one/counter_2> in Unit <clock_gen> is equivalent to the
following FF/Latch, which will be removed : <task_four/glitchy_counter_0>
INFO:Xst:2261 - The FF/Latch <task_four/sb/counter_0> in Unit <clock_gen> is equivalent to the
following 2 FFs/Latches, which will be removed : <task_one/counter_0> <task_two/counter_0>
INFO:Xst:2261 - The FF/Latch <task_four/sb/counter_1> in Unit <clock_gen> is equivalent to the
following FF/Latch, which will be removed : <task_one/counter_1>

Mapping all equations...
Building and optimizing final netlist ...
Found area constraint ratio of 100 (+ 5) on block clock_gen, actual ratio is 2.

Final Macro Processing ...

=========================================================================
Final Register Report

Macro Statistics
# Registers                                       : 25
 Flip-Flops                                       : 25

=========================================================================

=========================================================================
*                          Partition Report                             *
=========================================================================

Partition Implementation Status
-------------------------------

  No Partitions were found in this design.

-------------------------------

=========================================================================
*                           Design Summary                              *
=========================================================================

Top Level Output File Name         : clock_gen.ngc

Primitive and Black Box Usage:
-------------------------------
# BELS                             : 28
#      INV                         : 2
#      LUT2                        : 3
#      LUT3                        : 4
```

```
#      LUT4                        : 6
#      LUT5                        : 11
#      LUT6                        : 2
# FlipFlops/Latches                : 25
#      FD                          : 10
#      FDR                         : 14
#      FDR_1                       : 1
# Clock Buffers                    : 1
#      BUFGP                       : 1
# IO Buffers                       : 15
#      IBUF                        : 1
#      OBUF                        : 14

Device utilization summary:
---------------------------

Selected Device : 6slx4csg225-3


Slice Logic Utilization:
 Number of Slice Registers:             25  out of   4800     0%
 Number of Slice LUTs:                  28  out of   2400     1%
    Number used as Logic:               28  out of   2400     1%

Slice Logic Distribution:
 Number of LUT Flip Flop pairs used:    28
   Number with an unused Flip Flop:      3  out of     28    10%
   Number with an unused LUT:            0  out of     28     0%
   Number of fully used LUT-FF pairs:   25  out of     28    89%
   Number of unique control sets:        3

IO Utilization:
 Number of IOs:                         16
 Number of bonded IOBs:                 16  out of    132    12%

Specific Feature Utilization:
 Number of BUFG/BUFGCTRLs:               1  out of     16     6%

---------------------------
Partition Resource Summary:
---------------------------

  No Partitions were found in this design.

---------------------------


=================================================================================
Timing Report

NOTE: THESE TIMING NUMBERS ARE ONLY A SYNTHESIS ESTIMATE.
      FOR ACCURATE TIMING INFORMATION PLEASE REFER TO THE TRACE REPORT
      GENERATED AFTER PLACE-and-ROUTE.

Clock Information:
------------------
-----------------------------------+------------------------+-------+
```

```
Clock Signal                       | Clock buffer(FF name)  | Load  |
-----------------------------------+------------------------+-------+
clk_in                             | BUFGP                  | 25    |
-----------------------------------+------------------------+-------+

Asynchronous Control Signals Information:
----------------------------------------
No asynchronous control signals found in this design

Timing Summary:
---------------
Speed Grade: -3

   Minimum period: 2.636ns (Maximum Frequency: 379.391MHz)
   Minimum input arrival time before clock: 3.064ns
   Maximum output required time after clock: 4.521ns
   Maximum combinational path delay: No path found

Timing Details:
---------------
All values displayed in nanoseconds (ns)

=========================================================================
Timing constraint: Default period analysis for Clock 'clk_in'
  Clock period: 2.636ns (frequency: 379.391MHz)
  Total number of paths / destination ports: 105 / 25
-------------------------------------------------------------------------
Delay:               2.636ns (Levels of Logic = 2)
  Source:            task_four/glitchy_counter_3 (FF)
  Destination:       task_four/glitchy_counter_5 (FF)
  Source Clock:      clk_in rising
  Destination Clock: clk_in rising

  Data Path: task_four/glitchy_counter_3 to task_four/glitchy_counter_5
                                Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     FDR:C->Q              4   0.447   1.028  task_four/glitchy_counter_3
(task_four/glitchy_counter_3)
     LUT5:I0->O            3   0.203   0.651  task_four/Maccum_glitchy_counter_cy<3>11
(task_four/Maccum_glitchy_counter_cy<3>)
     LUT6:I5->O            1   0.205   0.000  task_four/Maccum_glitchy_counter_xor<7>11
(Result<7>)
     FDR:D                     0.102          task_four/glitchy_counter_7
    ----------------------------------------
    Total                      2.636ns (0.957ns logic, 1.679ns route)
                                       (36.3% logic, 63.7% route)

=========================================================================
Timing constraint: Default OFFSET IN BEFORE for Clock 'clk_in'
  Total number of paths / destination ports: 25 / 25
-------------------------------------------------------------------------
Offset:              3.064ns (Levels of Logic = 2)
  Source:            rst (PAD)
  Destination:       task_two/counter_3 (FF)
  Destination Clock: clk_in rising
```

```
  Data Path: rst to task_two/counter_3
                                Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     IBUF:I->O            25   1.222   1.537  rst_IBUF (rst_IBUF)
     LUT5:I0->O            1   0.203   0.000  task_two/counter_3_rstpot
(task_two/counter_3_rstpot)
     FD:D                      0.102          task_two/counter_3
    ----------------------------------------
    Total                      3.064ns (1.527ns logic, 1.537ns route)
                                       (49.8% logic, 50.2% route)

=========================================================================
Timing constraint: Default OFFSET OUT AFTER for Clock 'clk_in'
  Total number of paths / destination ports: 15 / 14
-------------------------------------------------------------------------
Offset:              4.521ns (Levels of Logic = 2)
  Source:            task_three/pos_clk/clk_out (FF)
  Destination:       clk_div_5 (PAD)
  Source Clock:      clk_in rising

  Data Path: task_three/pos_clk/clk_out to clk_div_5
                                Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     FDR:C->Q              2   0.447   0.721  task_three/pos_clk/clk_out
(task_three/pos_clk/clk_out)
     LUT2:I0->O            1   0.203   0.579  task_three/clk_div_51 (clk_div_5_OBUF)
     OBUF:I->O                 2.571          clk_div_5_OBUF (clk_div_5)
    ----------------------------------------
    Total                      4.521ns (3.221ns logic, 1.300ns route)
                                       (71.2% logic, 28.8% route)

=========================================================================

Cross Clock Domains Report:
--------------------------

Clock to Setup on destination clock clk_in
---------------+---------+---------+---------+---------+
               | Src:Rise| Src:Fall| Src:Rise| Src:Fall|
Source Clock   |Dest:Rise|Dest:Rise|Dest:Fall|Dest:Fall|
---------------+---------+---------+---------+---------+
clk_in         |    2.636|         |    1.811|         |
---------------+---------+---------+---------+---------+

=========================================================================


Total REAL time to Xst completion: 14.00 secs
Total CPU time to Xst completion: 13.22 secs

-->


Total memory usage is 482740 kilobytes
```

```
Number of errors   :    0 (   0 filtered)
Number of warnings :    4 (   0 filtered)
Number of infos    :    4 (   0 filtered)

================================================
MAP REPORT
================================================
Release 14.7 Map P.20131013 (lin64)
Xilinx Mapping Report File for Design 'clock_gen'

Design Information
------------------
Command Line   : map -intstyle ise -p xc6slx4-csg225-3 -w -logic_opt off -ol
high -t 1 -xt 0 -register_duplication off -r 4 -global_opt off -mt off -ir off
-pr off -lc off -power off -o clock_gen_map.ncd clock_gen.ngd clock_gen.pcf
Target Device  : xc6slx4
Target Package : csg225
Target Speed   : -3
Mapper Version : spartan6 -- $Revision: 1.55 $
Mapped Date    : Sun May 10 23:32:35 2020

Design Summary
--------------
Number of errors:      0
Number of warnings:    0
Slice Logic Utilization:
  Number of Slice Registers:                   25 out of   4,800    1%
    Number used as Flip Flops:                 25
    Number used as Latches:                     0
    Number used as Latch-thrus:                 0
    Number used as AND/OR logics:               0
  Number of Slice LUTs:                        19 out of   2,400    1%
    Number used as logic:                      19 out of   2,400    1%
      Number using O6 output only:             11
      Number using O5 output only:              0
      Number using O5 and O6:                   8
      Number used as ROM:                       0
    Number used as Memory:                      0 out of   1,200    0%

Slice Logic Distribution:
  Number of occupied Slices:                    9 out of     600    1%
  Number of MUXCYs used:                        0 out of   1,200    0%
  Number of LUT Flip Flop pairs used:          19
    Number with an unused Flip Flop:            1 out of      19    5%
    Number with an unused LUT:                  0 out of      19    0%
    Number of fully used LUT-FF pairs:         18 out of      19   94%
    Number of unique control sets:              4
    Number of slice register sites lost
      to control set restrictions:             15 out of   4,800    1%

  A LUT Flip Flop pair for this architecture represents one LUT paired with
  one Flip Flop within a slice.  A control set is a unique combination of
  clock, reset, set, and enable signals for a registered element.
  The Slice Logic Distribution report is not meaningful if the design is
  over-mapped for a non-slice resource or if Placement fails.

IO Utilization:
```

```
  Number of bonded IOBs:                          16 out of     132   12%

Specific Feature Utilization:
  Number of RAMB16BWERs:                           0 out of      12    0%
  Number of RAMB8BWERs:                            0 out of      24    0%
  Number of BUFIO2/BUFIO2_2CLKs:                   0 out of      32    0%
  Number of BUFIO2FB/BUFIO2FB_2CLKs:               0 out of      32    0%
  Number of BUFG/BUFGMUXs:                         1 out of      16    6%
    Number used as BUFGs:                          1
    Number used as BUFGMUX:                        0
  Number of DCM/DCM_CLKGENs:                       0 out of       4    0%
  Number of ILOGIC2/ISERDES2s:                     0 out of     200    0%
  Number of IODELAY2/IODRP2/IODRP2_MCBs:           0 out of     200    0%
  Number of OLOGIC2/OSERDES2s:                     0 out of     200    0%
  Number of BSCANs:                                0 out of       4    0%
  Number of BUFHs:                                 0 out of     128    0%
  Number of BUFPLLs:                               0 out of       8    0%
  Number of BUFPLL_MCBs:                           0 out of       4    0%
  Number of DSP48A1s:                              0 out of       8    0%
  Number of ICAPs:                                 0 out of       1    0%
  Number of PCILOGICSEs:                           0 out of       2    0%
  Number of PLL_ADVs:                              0 out of       2    0%
  Number of PMVs:                                  0 out of       1    0%
  Number of STARTUPs:                              0 out of       1    0%
  Number of SUSPEND_SYNCs:                         0 out of       1    0%

Average Fanout of Non-Clock Nets:                3.93

Peak Memory Usage:  737 MB
Total REAL time to MAP completion:  24 secs
Total CPU time to MAP completion:   23 secs

Table of Contents
-----------------
Section 1 - Errors
Section 2 - Warnings
Section 3 - Informational
Section 4 - Removed Logic Summary
Section 5 - Removed Logic
Section 6 - IOB Properties
Section 7 - RPMs
Section 8 - Guide Report
Section 9 - Area Group and Partition Summary
Section 10 - Timing Report
Section 11 - Configuration String Information
Section 12 - Control Set Information
Section 13 - Utilization by Hierarchy

Section 1 - Errors
------------------

Section 2 - Warnings
--------------------

Section 3 - Informational
-------------------------
INFO:MapLib:562 - No environment variables are currently set.
```

```
INFO:LIT:244 - All of the single ended outputs in this design are using slew
   rate limited output drivers. The delay on speed critical single ended outputs
   can be dramatically reduced by designating them as fast outputs.
INFO:Pack:1716 - Initializing temperature to 85.000 Celsius. (default - Range:
   0.000 to 85.000 Celsius)
INFO:Pack:1720 - Initializing voltage to 1.140 Volts. (default - Range: 1.140 to
   1.260 Volts)
INFO:Map:215 - The Interim Design Summary has been generated in the MAP Report
   (.mrp).
INFO:Pack:1650 - Map created a placed design.

Section 4 - Removed Logic Summary
---------------------------------

Section 5 - Removed Logic
-------------------------

To enable printing of redundant blocks removed and signals merged, set the
detailed map report option and rerun map.

Section 6 - IOB Properties
--------------------------

+----------------------------------------------------------------------------------------------------
----------------------------------------------------------+
| IOB Name                           | Type             | Direction | IO Standard          |
Diff  | Drive    | Slew | Reg (s)      | Resistor | IOB      |
|                                    |                  |           |                      |
Term  | Strength | Rate |              |          | Delay    |
+----------------------------------------------------------------------------------------------------
----------------------------------------------------------+
| clk_div_2                          | IOB              | OUTPUT    | LVCMOS25             |
| 12       | SLOW |              |          |          |
| clk_div_4                          | IOB              | OUTPUT    | LVCMOS25             |
| 12       | SLOW |              |          |          |
| clk_div_5                          | IOB              | OUTPUT    | LVCMOS25             |
| 12       | SLOW |              |          |          |
| clk_div_8                          | IOB              | OUTPUT    | LVCMOS25             |
| 12       | SLOW |              |          |          |
| clk_div_16                         | IOB              | OUTPUT    | LVCMOS25             |
| 12       | SLOW |              |          |          |
| clk_div_28                         | IOB              | OUTPUT    | LVCMOS25             |
| 12       | SLOW |              |          |          |
| clk_in                             | IOB              | INPUT     | LVCMOS25             |
|          |      |              |          |          |
| glitchy_counter<0>                 | IOB              | OUTPUT    | LVCMOS25             |
| 12       | SLOW |              |          |          |
| glitchy_counter<1>                 | IOB              | OUTPUT    | LVCMOS25             |
| 12       | SLOW |              |          |          |
| glitchy_counter<2>                 | IOB              | OUTPUT    | LVCMOS25             |
| 12       | SLOW |              |          |          |
| glitchy_counter<3>                 | IOB              | OUTPUT    | LVCMOS25             |
| 12       | SLOW |              |          |          |
| glitchy_counter<4>                 | IOB              | OUTPUT    | LVCMOS25             |
| 12       | SLOW |              |          |          |
| glitchy_counter<5>                 | IOB              | OUTPUT    | LVCMOS25             |
| 12       | SLOW |              |          |          |
```

glitchy_counter<6>	IOB	OUTPUT	LVCMOS25
12	SLOW			
glitchy_counter<7>	IOB	OUTPUT	LVCMOS25
12	SLOW			
rst	IOB	INPUT	LVCMOS25
+---
---+

Section 7 - RPMs

Section 8 - Guide Report

Guide not run on this design.

Section 9 - Area Group and Partition Summary

Partition Implementation Status

  No Partitions were found in this design.

Area Group Information

  No area groups were found in this design.

Section 10 - Timing Report

A logic-level (pre-route) timing report can be generated by using Xilinx static
timing analysis tools, Timing Analyzer (GUI) or TRCE (command line), with the
mapped NCD and PCF files. Please note that this timing report will be generated
using estimated delay information. For accurate numbers, please generate a
timing report with the post Place and Route NCD file.

For more information about the Timing Analyzer, consult the Xilinx Timing
Analyzer Reference Manual; for more information about TRCE, consult the Xilinx
Command Line Tools User Guide "TRACE" chapter.

Section 11 - Configuration String Details

Use the "-detail" map option to print out Configuration Strings

Section 12 - Control Set Information

Use the "-detail" map option to print out Control Set Information.

Section 13 - Utilization by Hierarchy

Use the "-detail" map option to print out the Utilization by Hierarchy section.