1. Description

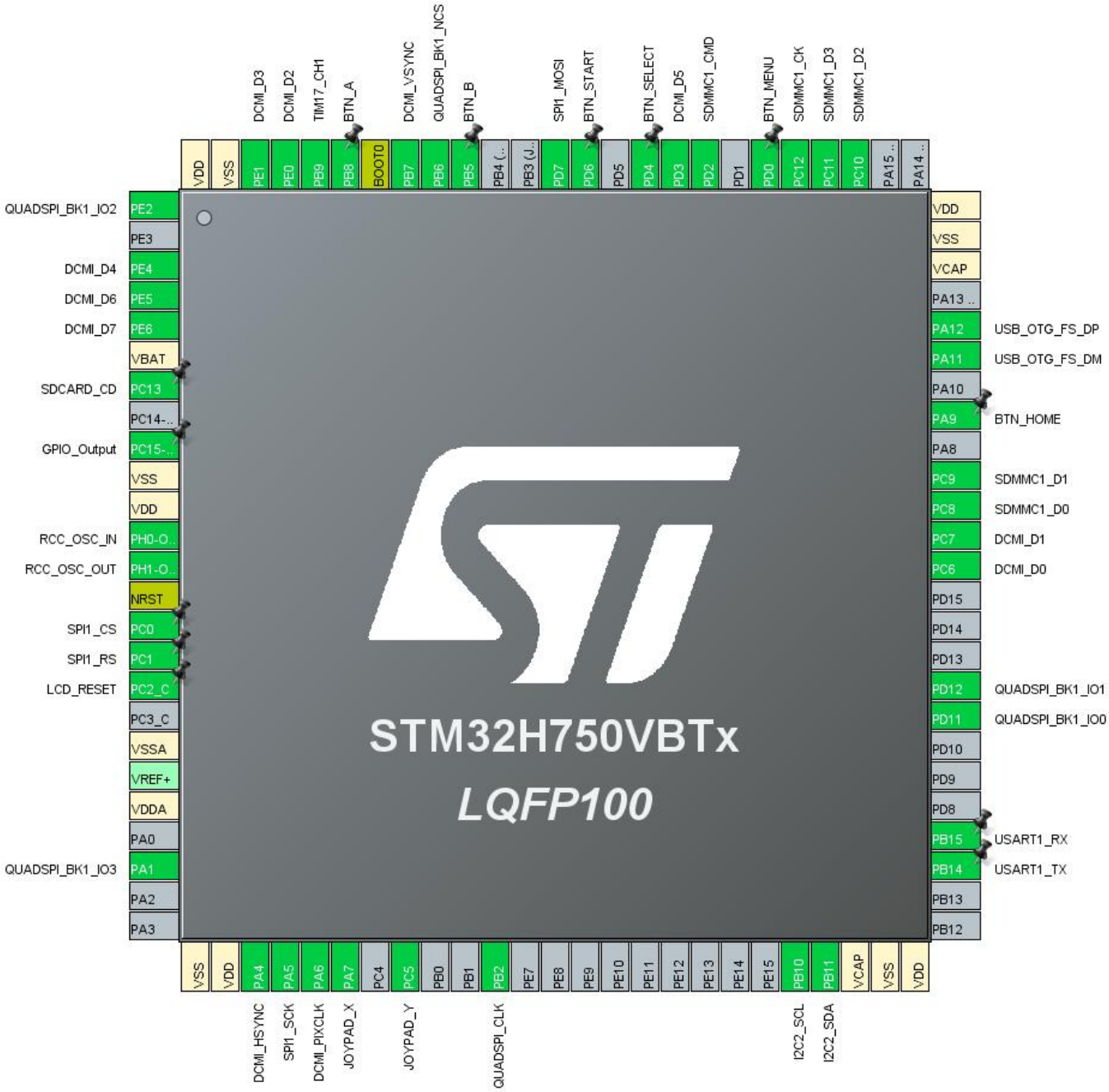
1.1. Project

Project Name	stm32h750
Board Name	custom
Generated with:	STM32CubeMX 5.5.0
Date	02/01/2020

1.2. MCU

MCU Series	STM32H7
MCU Line	STM32H750 Value line
MCU name	STM32H750VBTx
MCU Package	LQFP100
MCU Pin number	100

2. Pinout Configuration



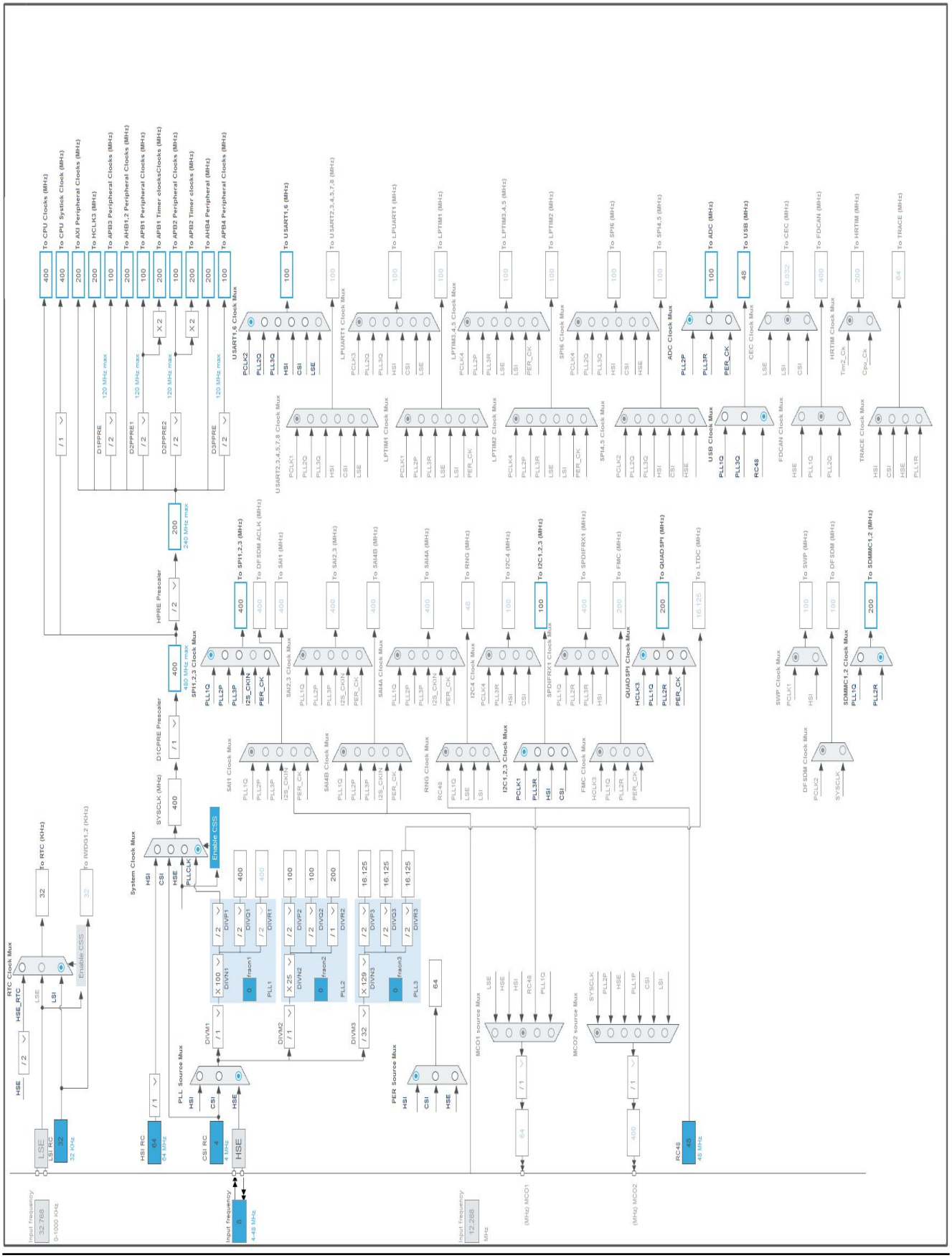
3. Pins Configuration

Pin Number LQFP100	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
1	PE2	I/O	QUADSPI_BK1_IO2	
3	PE4	I/O	DCMI_D4	
4	PE5	I/O	DCMI_D6	
5	PE6	I/O	DCMI_D7	
6	VBAT	Power		
7	PC13 *	I/O	GPIO_Input	SDCARD_CD
9	PC15-OSC32_OUT (OSC32_OUT) *	I/O	GPIO_Output	
10	VSS	Power		
11	VDD	Power		
12	PH0-OSC_IN (PH0)	I/O	RCC_OSC_IN	
13	PH1-OSC_OUT (PH1)	I/O	RCC_OSC_OUT	
14	NRST	Reset		
15	PC0 *	I/O	GPIO_Output	SPI1_CS
16	PC1 *	I/O	GPIO_Output	SPI1_RS
17	PC2_C *	I/O	GPIO_Output	LCD_RESET
19	VSSA	Power		
21	VDDA	Power		
23	PA1	I/O	QUADSPI_BK1_IO3	
26	VSS	Power		
27	VDD	Power		
28	PA4	I/O	DCMI_HSYNC	
29	PA5	I/O	SPI1_SCK	
30	PA6	I/O	DCMI_PIXCLK	
31	PA7	I/O	ADC1_INP7	JOYPAD_X
33	PC5	I/O	ADC1_INP8	JOYPAD_Y
36	PB2	I/O	QUADSPI_CLK	
46	PB10	I/O	I2C2_SCL	
47	PB11	I/O	I2C2_SDA	
48	VCAP	Power		
49	VSS	Power		
50	VDD	Power		
53	PB14	I/O	USART1_TX	
54	PB15	I/O	USART1_RX	
58	PD11	I/O	QUADSPI_BK1_IO0	
59	PD12	I/O	QUADSPI_BK1_IO1	

Pin Number LQFP100	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
63	PC6	I/O	DCMI_D0	
64	PC7	I/O	DCMI_D1	
65	PC8	I/O	SDMMC1_D0	
66	PC9	I/O	SDMMC1_D1	
68	PA9 *	I/O	GPIO_Input	BTN_HOME
70	PA11	I/O	USB_OTG_FS_DM	
71	PA12	I/O	USB_OTG_FS_DP	
73	VCAP	Power		
74	VSS	Power		
75	VDD	Power		
78	PC10	I/O	SDMMC1_D2	
79	PC11	I/O	SDMMC1_D3	
80	PC12	I/O	SDMMC1_CK	
81	PD0 *	I/O	GPIO_Input	BTN_MENU
83	PD2	I/O	SDMMC1_CMD	
84	PD3	I/O	DCMI_D5	
85	PD4 *	I/O	GPIO_Input	BTN_SELECT
87	PD6 *	I/O	GPIO_Input	BTN_START
88	PD7	I/O	SPI1_MOSI	
91	PB5 *	I/O	GPIO_Input	BTN_B
92	PB6	I/O	QUADSPI_BK1_NCS	
93	PB7	I/O	DCMI_VSYNC	
94	BOOT0	Boot		
95	PB8 *	I/O	GPIO_Input	BTN_A
96	PB9	I/O	TIM17_CH1	
97	PE0	I/O	DCMI_D2	
98	PE1	I/O	DCMI_D3	
99	VSS	Power		
100	VDD	Power		

* The pin is affected with an I/O function

4. Clock Tree Configuration



5. Software Project

5.1. Project Settings

Name	Value
Project Name	stm32h750
Project Folder	D:\git\stm32h750\stm32h750_fw\src\lib\cubemx\stm32h750
Toolchain / IDE	TrueSTUDIO
Firmware Package Name and Version	STM32Cube FW_H7 V1.6.0

5.2. Code Generation Settings

Name	Value
STM32Cube MCU packages and embedded software	Copy only the necessary library files
Generate peripheral initialization as a pair of '.c/.h' files	Yes
Backup previously generated files when re-generating	No
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No

6. Power Consumption Calculator report

6.1. Microcontroller Selection

Series	STM32H7
Line	STM32H750 Value line
MCU	STM32H750VBTx
Datasheet	DS12556_Rev2

6.2. Parameter Selection

Temperature	25
Vdd	3.0

7. IPs and Middleware Configuration

7.1. ADC1

mode: IN7

mode: IN8

7.1.1. Parameter Settings:

ADCs_Common_Settings:	
Mode	Independent mode
ADC_Settings:	
Clock Prescaler	Asynchronous clock mode divided by 4
Resolution	**ADC 12-bit resolution ***
Scan Conversion Mode	Enabled
Continuous Conversion Mode	**Enabled ***
Discontinuous Conversion Mode	Disabled
End Of Conversion Selection	End of single conversion
Overrun behaviour	Overrun data preserved
Conversion Data Management Mode	**DMA Circular Mode ***
Low Power Auto Wait	Disabled
ADC_Regular_ConversionMode:	
Enable Regular Conversions	Enable
Left Bit Shift	No bit shift
Enable Regular Oversampling	Disable
Number Of Conversion	**2 ***
External Trigger Conversion Source	Regular Conversion launched by software
External Trigger Conversion Edge	None
Rank	1
Channel	Channel 7
Sampling Time	1.5 Cycles
Offset Number	No offset
Rank	**2 ***
Channel	**Channel 8 ***
Sampling Time	1.5 Cycles
Offset Number	No offset
ADC_Injected_ConversionMode:	
Enable Injected Conversions	Disable
Analog Watchdog 1:	
Enable Analog WatchDog1 Mode	false
Analog Watchdog 2:	
Enable Analog WatchDog2 Mode	false

Analog Watchdog 3:

Enable Analog WatchDog3 Mode	false

7.2. CORTEX_M7

7.2.1. Parameter Settings:

Cortex Interface Settings:

CPU ICache	Disabled
CPU DCache	Disabled

Cortex Memory Protection Unit Control Settings:

MPU Control Mode	MPU NOT USED

7.3. DCMI

DCMI: Slave 8 bits External Synchro

7.3.1. Parameter Settings:

Mode Config:

Pixel clock polarity	Active on Falling edge
Vertical synchronization polarity	Active Low
Horizontal synchronization polarity	Active Low
Frequency of frame capture	All frames are captured
JPEG mode	Disabled

Interface Capture Config:

Byte Select Mode	Interface captures all received bytes
Line Select Mode	Interface captures all received lines

7.4. DMA2D

mode: Activated

7.4.1. Parameter Settings:

Basic Parameters:

Transfer Mode	Memory to Memory
Color Mode	ARGB8888
Output Offset	0
DMA2D Bytes Swap	Bytes in regular order in output FIFO

DMA2D Line Offset Mode	Line offsets expressed in pixels

Foreground layer Configuration:

DMA2D Input Color Mode	ARGB8888
DMA2D ALPHA MODE	No modification of the alpha channel value
Input Alpha	0
Input Offset	0
DMA2D ALPHA Inversion	Regular Alpha
DMA2D Red and Blue swap	Regular mode (RGB or ARGB)
DMA2D Chroma Sub-Sampling Mode	No chroma sub-sampling 4:4:4

7.5. GPIO

7.6. I2C2

I2C: I2C

7.6.1. Parameter Settings:

Timing configuration:

I2C Speed Mode	Standard Mode
I2C Speed Frequency (KHz)	100
Rise Time (ns)	0
Fall Time (ns)	0
Coefficient of Digital Filter	0
Analog Filter	Enabled
Timing	**0x10C0ECFF ***

Slave Features:

Clock No Stretch Mode	Disabled
General Call Address Detection	Disabled
Primary Address Length selection	7-bit
Dual Address Acknowledged	Disabled
Primary slave address	0

7.7. QUADSPI

QuadSPI Mode: Bank1 with Quad SPI Lines

7.7.1. Parameter Settings:

General Parameters:

Clock Prescaler

	1 *
Fifo Threshold	**4 ***
Sample Shifting	**Sample Shifting Half Cycle ***
Flash Size	**23 ***
Chip Select High Time	**6 Cycles ***
Clock Mode	Low
Flash ID	Flash ID 1
Dual Flash	Disabled

7.8. RCC

High Speed Clock (HSE): Crystal/Ceramic Resonator

7.8.1. Parameter Settings:

SupplySource	PWR_LDO_SUPPLY
RCC Parameters:	
TIM Prescaler Selection	Disabled
HSE Startup Timout Value (ms)	100
LSE Startup Timout Value (ms)	5000
CSI Calibration Value	16
HSI Calibration Value	32
System Parameters:	
VDD voltage (V)	3.3
Flash Latency(WS)	2 WS (3 CPU cycle)
Power Parameters:	
Power Regulator Voltage Scale	Power Regulator Voltage Scale 1
PLL range Parameters:	
PLL1 clock Input range	Between 8 and 16 MHz
PLL2 input frequency range	Between 8 and 16 MHz
PLL1 clock Output range	Wide VCO range
PLL2 clock Output range	Wide VCO range

7.9. RTC

mode: Activate Clock Source

mode: Activate Calendar

7.9.1. Parameter Settings:

General:

Hour Format	Hourformat 24
Asynchronous Predivider value	127
Synchronous Predivider value	255

Calendar Time:

Data Format	BCD data format
Hours	0
Minutes	0
Seconds	0
Day Light Saving: value of hour adjustment	Daylightsaving None
Store Operation	Storeoperation Reset

Calendar Date:

Week Day	Monday
Month	January
Date	1
Year	0

7.10. SDMMC1

Mode: SD 4 bits Wide bus

7.10.1. Parameter Settings:

SDMMC parameters:

Clock transition on which the bit capture is made	Rising transition
SDMMC Clock output enable when the bus is idle	Disable the power save for the clock
SDMMC hardware flow control	The hardware control flow is disabled
SDMMC clock divide factor	0
Is external transceiver present ?	no

7.11. SPI1

Mode: Transmit Only Master

7.11.1. Parameter Settings:

Basic Parameters:

Frame Format	Motorola
Data Size	**16 Bits ***
First Bit	MSB First

Clock Parameters:

Prescaler (for Baud Rate)	**8 ***
Baud Rate	**50.0 MBits/s ***
Clock Polarity (CPOL)	Low
Clock Phase (CPHA)	1 Edge

Advanced Parameters:

CRC Calculation	Disabled
NSSP Mode	**Disabled ***
NSS Signal Type	Software
Fifo Threshold	Fifo Threshold 01 Data
Tx Crc Initialization Pattern	All Zero Pattern
Rx Crc Initialization Pattern	All Zero Pattern
Nss Polarity	Nss Polarity Low
Master Ss Idleness	00 Cycle
Master Inter Data Idleness	00 Cycle
Master Receiver Auto Susp	Disable
Master Keep Io State	Master Keep Io State Disable
IO Swap	Disabled

7.12. SYS

Timebase Source: SysTick

7.13. TIM2

Clock Source : Internal Clock

7.13.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**15999 ***
Counter Mode	Up
Counter Period (AutoReload Register - 32 bits value)	0
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection TRGO	Reset (UG bit from TIMx_EGR)

7.14. TIM6

mode: Activated

7.14.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	0
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Trigger Event Selection	Reset (UG bit from TIMx_EGR)

7.15. TIM7

mode: Activated

7.15.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	0
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Trigger Event Selection	Reset (UG bit from TIMx_EGR)

7.16. TIM17

mode: Activated

Channel1: PWM Generation CH1

7.16.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	0
Internal Clock Division (CKD)	No Division
Repetition Counter (RCR - 8 bits value)	0
auto-reload preload	Disable

Break And Dead Time management - BRK Configuration:

BRK State	Disable
BRK Polarity	High
BRK Filter (4 bits value)	0
BRK Sources Configuration	
- Digital Input	Disable
- COMP1	Disable
- COMP2	Disable
- DFSDM	Disable

Break And Dead Time management - Output Configuration:

Automatic Output State	Disable
Off State Selection for Run Mode (OSSR)	Disable
Off State Selection for Idle Mode (OSSI)	Disable
Lock Configuration	Off

PWM Generation Channel 1:

Mode	PWM mode 1
Pulse (16 bits value)	0
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High
CH Idle State	Reset

7.17. USART1

Mode: Asynchronous

7.17.1. Parameter Settings:

Basic Parameters:

Baud Rate	**57600 ***
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable
ClockPrescaler	clock /1
Fifo Mode	Disable
Txfifo Threshold	1 eighth full configuration
Rxfifo Threshold	1 eighth full configuration

Advanced Features:

Auto Baudrate	Disable
TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

7.18. USB_OTG_FS

Mode: Device_Only

7.18.1. Parameter Settings:

Speed	Full Speed 12MBit/s
Enable internal IP DMA	Disabled
Low power	Disabled
Battery charging	Disabled
Link Power Management	Disabled
Use dedicated end point 1 interrupt	Disabled
VBUS sensing	Disabled
Signal start of frame	Disabled

*** User modified value**

8. System Configuration

8.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
ADC1	PA7	ADC1_INP7	Analog mode	No pull-up and no pull-down	n/a	JOYPAD_X
	PC5	ADC1_INP8	Analog mode	No pull-up and no pull-down	n/a	JOYPAD_Y
DCMI	PE4	DCMI_D4	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PE5	DCMI_D6	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PE6	DCMI_D7	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PA4	DCMI_HSYNC	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PA6	DCMI_PIXCLK	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PC6	DCMI_D0	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PC7	DCMI_D1	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PD3	DCMI_D5	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PB7	DCMI_VSYNC	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PE0	DCMI_D2	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PE1	DCMI_D3	Alternate Function Push Pull	No pull-up and no pull-down	Low	
I2C2	PB10	I2C2_SCL	Alternate Function Open Drain	No pull-up and no pull-down	Low	
	PB11	I2C2_SDA	Alternate Function Open Drain	No pull-up and no pull-down	Low	
QUADSPI	PE2	QUADSPI_BK1_IO2	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PA1	QUADSPI_BK1_IO3	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PB2	QUADSPI_CLK	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PD11	QUADSPI_BK1_IO0	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PD12	QUADSPI_BK1_IO1	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PB6	QUADSPI_BK1_NCS	Alternate Function Push Pull	No pull-up and no pull-down	Low	
RCC	PH0-OSC_IN (PH0)	RCC_OSC_IN	n/a	n/a	n/a	
	PH1-OSC_OUT (PH1)	RCC_OSC_OUT	n/a	n/a	n/a	
SDMMC1	PC8	SDMMC1_D0	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PC9	SDMMC1_D1	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PC10	SDMMC1_D2	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PC11	SDMMC1_D3	Alternate Function Push Pull	No pull-up and no pull-down	Very High	

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
	PC12	SDMMC1_CK	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD2	SDMMC1_CMD	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
SPI1	PA5	SPI1_SCK	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PD7	SPI1_MOSI	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
TIM17	PB9	TIM17_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	
USART1	PB14	USART1_TX	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PB15	USART1_RX	Alternate Function Push Pull	No pull-up and no pull-down	Low	
USB_OTG_FS	PA11	USB_OTG_FS_DM	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PA12	USB_OTG_FS_DP	Alternate Function Push Pull	No pull-up and no pull-down	Low	
GPIO	PC13	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	SDCARD_CD
	PC15-OSC32_OUT	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PC0	GPIO_Output	Output Push Pull	No pull-up and no pull-down	**High ***	SPI1_CS
	PC1	GPIO_Output	Output Push Pull	No pull-up and no pull-down	**High ***	SPI1_RS
	PC2_C	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LCD_RESET
	PA9	GPIO_Input	Input mode	**Pull-up ***	n/a	BTN_HOME
	PD0	GPIO_Input	Input mode	**Pull-up ***	n/a	BTN_MENU
	PD4	GPIO_Input	Input mode	**Pull-up ***	n/a	BTN_SELECT
	PD6	GPIO_Input	Input mode	**Pull-up ***	n/a	BTN_START
	PB5	GPIO_Input	Input mode	**Pull-up ***	n/a	BTN_B
	PB8	GPIO_Input	Input mode	**Pull-up ***	n/a	BTN_A

8.2. DMA configuration

DMA request	Stream	Direction	Priority
USART1_RX	DMA1_Stream0	Peripheral To Memory	Low
SPI1_TX	DMA1_Stream1	Memory To Peripheral	Low
ADC1	DMA1_Stream2	Peripheral To Memory	Low

USART1_RX: DMA1_Stream0 DMA request Settings:

Mode:	**Circular ***
Use fifo:	Disable
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Byte
Memory Data Width:	Byte

SPI1_TX: DMA1_Stream1 DMA request Settings:

Mode:	Normal
Use fifo:	Disable
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	**Half Word ***
Memory Data Width:	**Half Word ***

ADC1: DMA1_Stream2 DMA request Settings:

Mode:	**Circular ***
Use fifo:	Disable
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Half Word
Memory Data Width:	Half Word

8.3. BDMA configuration

nothing configured in DMA service

8.4. MDMA configuration

nothing configured in DMA service

8.5. NVIC configuration

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Pre-fetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	0	0
System tick timer	true	0	0
DMA1 stream0 global interrupt	true	0	0
DMA1 stream1 global interrupt	true	0	0
DMA1 stream2 global interrupt	true	0	0
SPI1 global interrupt	true	0	0
PVD and AVD interrupts through EXTI line 16	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		
ADC1 and ADC2 global interrupts	unused		
TIM2 global interrupt	unused		
I2C2 event interrupt	unused		
I2C2 error interrupt	unused		
USART1 global interrupt	unused		
SDMMC1 global interrupt	unused		
TIM6 global interrupt, DAC1_CH1 and DAC1_CH2 underrun error interrupts	unused		
TIM7 global interrupt	unused		
DCMI global interrupt	unused		
FPU global interrupt	unused		
DMA2D global interrupt	unused		
QUADSPI global interrupt	unused		
USB On The Go FS End Point 1 Out global interrupt	unused		
USB On The Go FS End Point 1 In global interrupt	unused		
USB On The Go FS global interrupt	unused		
TIM17 global interrupt	unused		
HSEM1 global interrupt	unused		

*** User modified value**

9. Software Pack Report