IA-860m

Hardware Reference Guide

BittWare
a molex company

IA-860m
Hardware Reference Guide

Document Revision: 03-Dec-2025
Hardware Revision: 3/4

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The RF port connections on this product are for installation within the same building structure and indoor use only.

Please note that blowing fuses or making permanent changes to FPGA logic are considered as changes under the BittWare terms and conditions and can affect warranty. Please contact BittWare for further details.

Country of Origin

The IA-860m's Country of Origin is the United States of America.

Compliance

The *IA-860m* product is **Industrial (Class A) electromagnetic wave suitability equipment** and is intended for use in industrial, business, and commercial environments. In a residential environment this device might cause radio interference, which may require the user to take adequate corrective measures. It has been tested against the following specifications,

- FCC (USA) 47CFR15.107 / 47CFR15.109
- CE (Europe) EN55032:2015 + A1:2020 / EN55035:2017
- UKCA (United Kingdom) BS EN55032:2015 + A1:2020 / BS EN55035:2017
- ICES (Canada) ICES-003 Issue 7
- Safety: CB Test Certified EN IEC 62368-1:2020+A11:2020 / BS EN IEC 62368-1:2020+A11:2020 / CSA/UL 62368-1:2019 with national differences for EU Group, United States and Canada
- RoHS compliant

Federal Communications Commission (FCC) statement

This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense

This device complies with Part 15 of the FCC rules. Operation is subject to the following two conditions: (1) this device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation

CAN ICES-3 (A)/NMB-3 (A)

If further information is needed regarding REACH or conflicting minerals, please contact the Molex Compliance Group.

Contents

List of Figures

List of Tables

1 Introduction

1.1 About this Guide

This Hardware Reference Guide describes the components and interfaces on the Rev. 3 and 4 IA-860m.

1.2 Revision History

1.2.1 Board Revisions

The table below lists the hardware revisions for the IA-860m and the differences between them.

Table 1: Hardware revisions

Release Date	Hardware Revision	Notes/Changes
20-Dec-2023	0	Early Access Unit release
	1	Updated PCB that incorporates Rev 0 fixes and workarounds · Significant FPGA configuration time improvement with new BMC version
15-Sep-2024	2	New release of PCB Major BMC release
12-Dec-2024	3	New release of PCB Major BMC release
24-Apr-2025	4	New release of PCB BMC update Added backplate Production silicon FPGA

1.2.2 Document Revisions

The table below lists the revision history of this document.

Table 2: Document revisions

Release Date	Document Revision	Notes/Changes
20-Dec-2023	0.0	Early Access Unit release
30-Apr-2024	1.0	Updates throughout for complete first release
12-Jul-2024	1.1	Update to clock circuitry diagram
03-Jan-2025	3.0	Update for Hardware Revision 3 Update QSFP-DD pinouts Remove M.2 feature
13-Jan-2025	3.1	Added USB-C part number to Table 4 Added "QSFP_" to bank 12A net names in Table 11 Updated clock source to include _0 and capitalized signal names in Table 23
24-Jan-2025	3.2	Remove references to SSD
26-Mar-2025	3.3	Add instructions for handling connectors and cabling
15-Apr-2025	3.4	Updated USB and JTAG interface diagrams
24-Apr-2025	4.0	Updates for Rev 4 hardware

15-May-2025	4.1	Updated FTDI blaster instructions to include udev rule information
02-Jul-2025	4.2	Updated clock signal names (SDM_OSC_CLK_1, USR_CLK_3A, U1PPS) in Table 24
30-Jul-2025	4.3	Add compliance information
05-Sep-2025	4.4	Correct USB pico-lock connector part number
09-Sep-2025	4.5	Update JTAG usage details
03-Dec-2025	4.6	Correct FPGA temperature sensor locations (Figure 11)

1.3 Related Documentation

Refer to the following documents (available on the BittWare developer site) for more information about the IA-860m:

- IA-860m Getting Started Guide
- IA-860m BMC Reference Guide
- IA-860m FPGA Developer Reference Guide
- IA-860m SDK and CSP Reference Guide
- Altera Agilex FPGA documentation

1.4 Abbreviations & Definitions

- BMC Board Management Controller
- CSP Card Support Package
- CvP Configuration Via Protocol
- DDR Double Data Rate
- FPGA Field Programmable Gate Array
- Gb Gigabit
- GB Gigabyte
- I2C Inter-IC bus (standard)
- IO Input/Outputs
- IP Intellectual Property
- JTAG Joint Test Action Group (boundary scan standard)
- LED Light Emitting Diode
- MCTP Management Component Transfer Protocol
- MT/s Mega Transfers per second
- PLDM Platform Level Data Model
- POF Programmer Object File
- PR Partial Reconfiguration
- QSFP Quad Small Form-factor Pluggable
- QSFP-DD QSFP Double Density
- SDRAM Synchronous Dynamic Random-Access Memory
- SOF SRAM Object File
- SPI Serial Peripheral Interface
- PROM Programmable Read-Only Memory
- QSPI Quad Serial Peripheral Interface
- TCXO Temperature Compensated Xtal (crystal) Oscillator
- VID Voltage Identification

1.5 Contacting BittWare

BittWare is dedicated to providing customers with superior technical support:

- **BittWare Developer Site:** The BittWare Developer Site provides online access to our technical support resources. Go to developer.bittware.com to register for an account. Once you have set up an account, you will have access to BITTS (the BittWare Issue Tracking and Technical Support site), BittWare product documentation, software downloads, release notes, and examples. When you are logged into the Developer Site, follow the "Issue Tracking" link at the top right of the screen to access BITTS.
- **BittWare's website:** Our website at www.bittware.com provides a variety of literature, including whitepapers, datasheets, and articles.
- **Phone**: You can also call us directly at +1 (603) 226 0404 between the hours of 8:30 a.m.– 5:00 p.m. (US Eastern Time) or +44 (0) 1236 373500 between the hours of 8:30 a.m. – 5:00 p.m. (UK GMT).

1.6 Customer Feedback

Thank you for using BittWare products. We appreciate you choosing BittWare for your FPGA development.

If you have a few minutes to spare, we would love to hear from you about your experience with our products or our staff. We know your time is valuable; we would be grateful for any comment at all.

- Please email us at support@bittware.com for any type of feedback
- Or, let us know about a recent Technical Support inquiry at http://koch.link/bwsupportfeedback

2 Board Overview

The IA-860m is a full length, dual-width PCIe Gen5 x16 card with an Altera Agilex 7 M-Series FPGA. The FPGA features 32GB of HBM2e and is connected to three QSFP-DD ports and an MCIO port. The IA-860m supports both active (liquid) and passive cooling options.

2.1 Key Features

- **Form Factor:** Dual width, standard-height (111.15 mm), full-length (312 mm)
- **FPGA:** Altera Agilex AGMF039 FPGA (core speed grade -2, XCVR speed grade(-1 & -2)
- **Network I/O:** 3 QSFP-DD ports supporting 400/200/100/40/10 Gb Ethernet
    - Supports 3x 400GbE, 6x 200/100/50/25/10GbE
    - Supports 12x 100GbE with breakout cables
- **Additional I/O:**
    - MCIO x8 connector supporting 2x Gen4 x4 root complexes
    - GPIO connector
    - 1PPS and external reference clock
- **Memory Banks:**
    - 40-bit DDR4 for HPS
    - 32 GB HBM2e in FPGA
- **FPGA Configuration:**
    - Power-on FPGA configuration from flash, dual image
    - USB-Blaster II Interface for FPGA JTAG access[1]
- **Board Management Controller (BMC 3.0):**
    - Voltage, current, temperature monitoring
    - Power sequencing and reset
    - Field upgrades
    - FPGA configuration and control
    - Clock configuration
    - Low bandwidth BMC-FPGA comms with SPI link
    - USB 2.0
    - PLDM support
    - Card-level security (future)
    - RTC with battery backup option[2]
    - Link from HPS to FPGA HPS UART
- **USB connectivity:**
    - USB access to BMC, USB-UART

1 Requires optional cable (external USB Blaster pod) and is not an integrated/on-card USB blaster II implementation.

2 Battery backup is not a default option. Please contact BittWare for details.

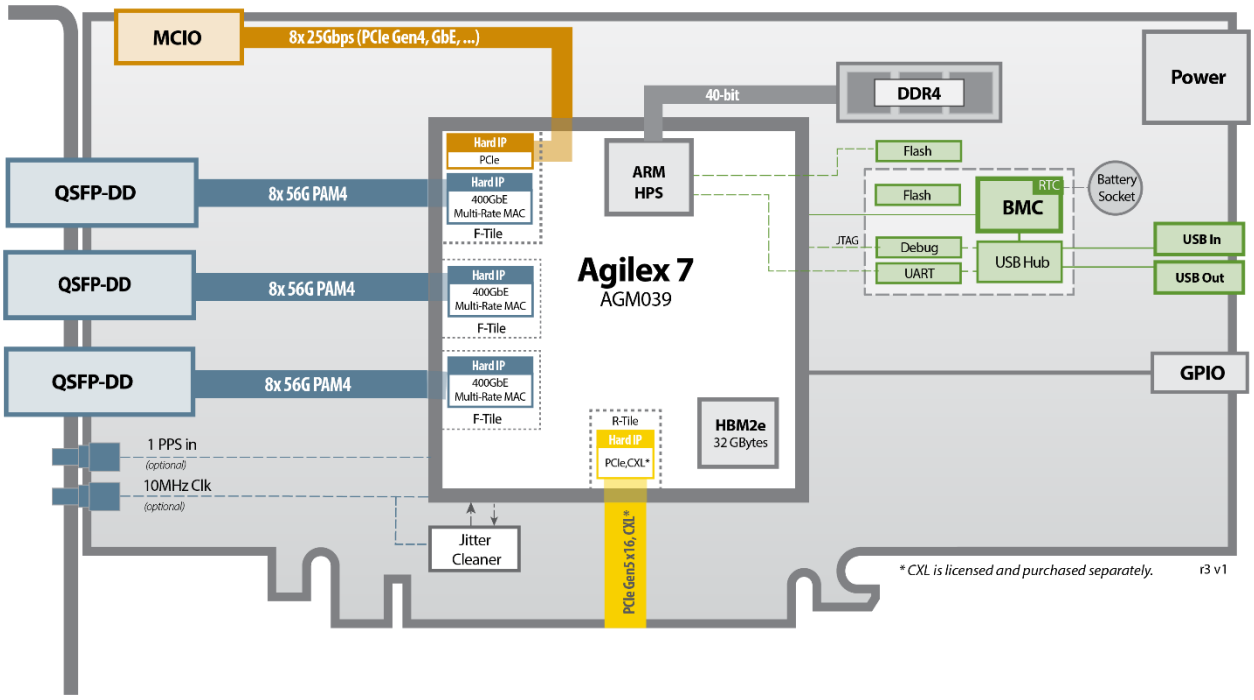
- USB daisy chaining

- **User clocks**
- **User LEDs**

2.2 Block Diagram

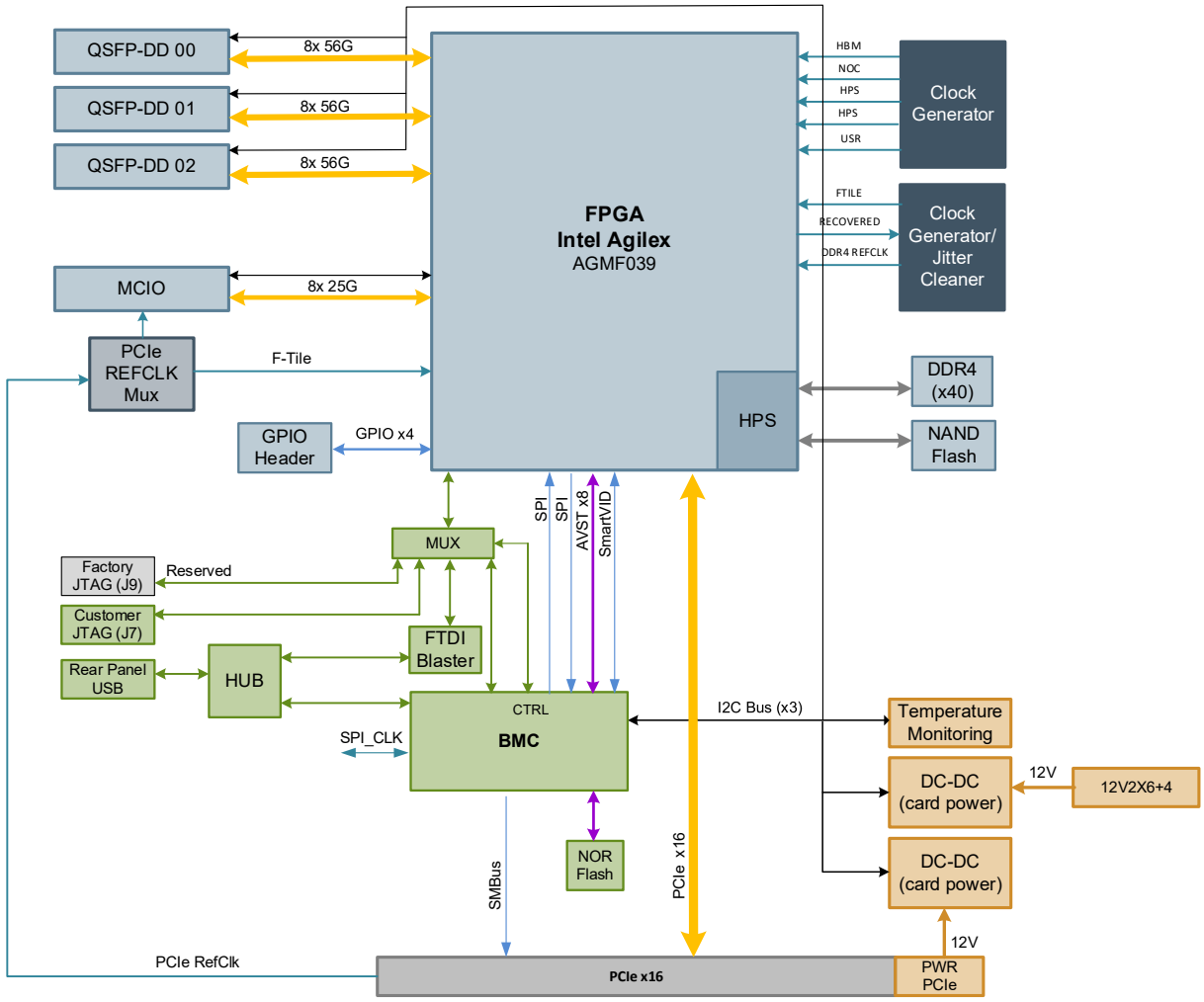
The diagram below shows the key functional features of the IA-860m. The FPGA is used to implement the PCIe Gen5, QSFP-DD, and Board Management Controller interfaces while leaving ample room for user applications. The board is also designed to efficiently handle cooling for higher powered FPGA applications while maintaining high throughput.

Figure 1: IA-860m Block Diagram



Note: Refer to the images in the Board Layout section for actual component and connector locations.

Figure 2: IA-860m Functional Block Diagram



2.3 Board Layout

This section shows where the main components on the IA-860m are located. Each of these is described in more detail later in this document. Refer to the Mechanical section for full card configuration.

Figure 3: Top View

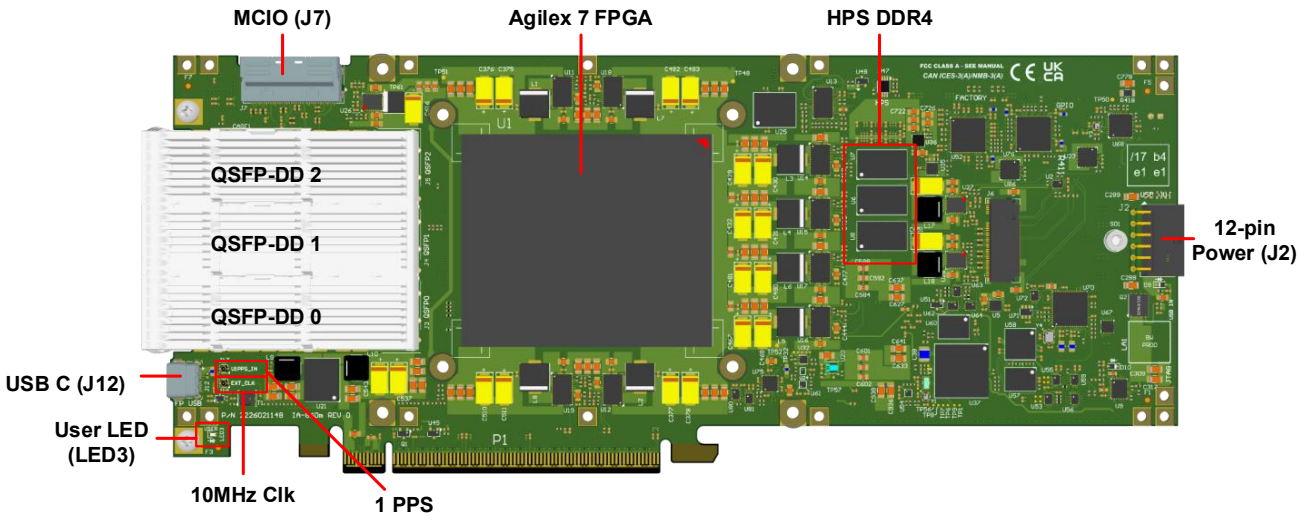
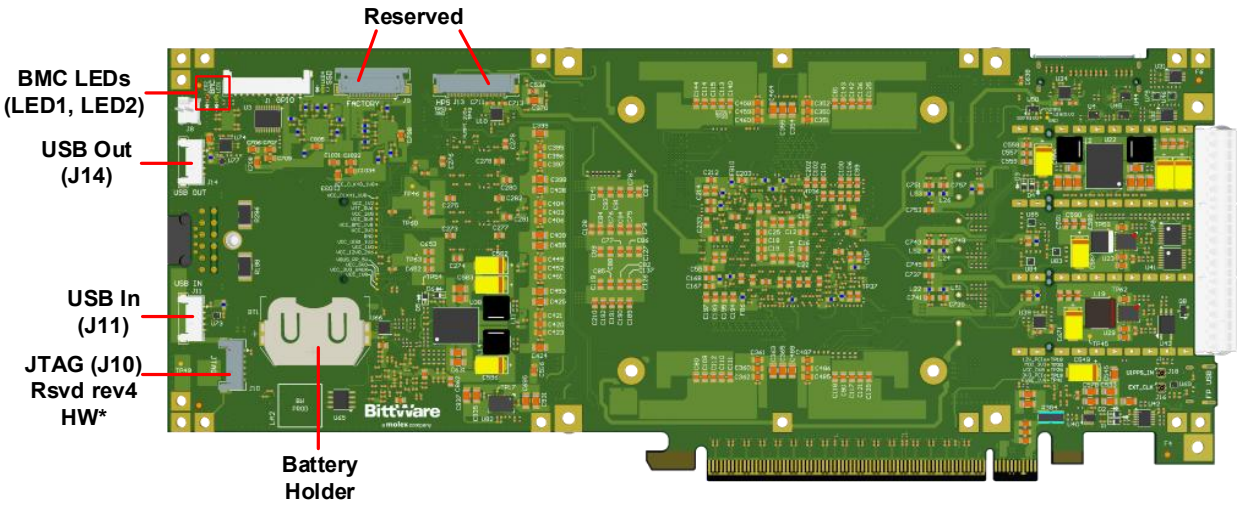


Figure 4: Bottom View



* J10 is reserved on Rev 4 cards. The connector is deprecated because JTAG via FTDI is enabled by default on Rev 4 hardware.

2.4 Key Components

The tables below list the manufacturer and part number of the board's key components and connectors.

Table 3: Component List

Component	Part Number	Manufacturer
Agilex FPGA	AGM**F039**R47A**1E2**VR0 NPI Engineering Silicon AGM**F039**R47A**1E2V** (Production) Default part	Altera
BMC configuration Flash (x2)	MT25QU02GCBB8E12-0SIT	Micron
HPS NAND flash	MT29F4G08ABBDAH4-IT:D	Micron
DDR4 (HPS)	MT40A1G16TB-062E IT:F	Micron
I/O expander	TCA9554PWR	Texas Instruments
Microcontroller	MIMXRT1165CVM5A	NXP
MAC ID PROM	AT24C02D-SSHM-T	Microchip Technology
USB hub	USB2534I-1080AENTR	Microchip Technology
USB to UART	FT4232HQ-REEL	FTDI
Hot swap controller	LTC4281IUFD#PBF	Analog Devices
24MHz crystal	XRCGB24M000F3M00R0	Murata Manufacturing
12MHz clock	NX3225SA-12.000M-STD-CSR-1	NDK
32.768KHz crystal	FX135A-327	Fox Electronics
Clock generator (x2)	SIT95148AI-A00000-X	SiTime
Clock buffer	PI6CB33202ZDIEX	DIODES

Table 4: Connector List

Connector	Part Number	Manufacturer
QSFP-DD (CAGE0, CAGE1, CAGE2)	2027180100	Molex
GPIO (J1)	50405041291	Molex
Power (J2)	10160920-1240100LF	Amphenol
QSFP-DD (J3, J4, J5)	524373071	Molex
MCIO (J7)	G97R22332HR	Amphenol
JTAG (J10)	5040500691	Molex
USB in (J11) USB out (J14)	5040500591	Molex
USB-C (J12)	201267-0005	Molex
Ext. clock (J15) 1 PPS (J17)	RECE.20369.001E.01	TAOGLAS

2.5 Programmable Devices

The following table describes the programmable non-volatile devices on the IA-860m.

Device	Description	Programming Method(s)	Usage
BMC	Local microcontroller, flash based	BittWare factory-programmed	Stores code and configuration options. Clock configuration stored in local flash. FRU data.
Configuration flash	FPGA boot configuration	USB or PCIe (via BMC), or pre-programmed	256MB configuration space. Currently supporting single default flash image. The BMC supports multiple images and fallback
MAC ID and serial number PROM	Card ID information	Base MAC ID factory programmed	The FPGA will read the base MAC ID and can use 24 sequential addresses. The serial number can be read and used for software feature licensing. The MAC PROM is programmed at BittWare's factory with card unique information. For more information about the content of the MAC PROM, and how to access its content, see VPD EPROM
SiT95148 clock generators	Jitter cleaner	Written by BMC during power-up sequence	Stored in BMC, user writable with host side utility. Host side utility supported from SDK 2023.3 and newer. Note there are two of these clock generators, one for transceiver clocks and jitter cleaning, the second for System clocks

Letter of Volatility: Please contact BittWare support if you need a letter of volatility for this board.

2.6 Board Options and Variants

This Hardware Reference Guide describes a default hardware configuration of the IA-860m. Keep in mind that your board may be configured differently.

The part number breakdown is described below. Note that not all options are available, and options may be added or removed in the future. Contact BittWare for the latest information. Refer to the Getting Started Guide and the bw_card_list command to find your card's part number.

IA-860i-a-bbbbbbb-9-de-f-gh-ij-k-l-m

Description	Letter	Option	Description
Board	a	S	S-Standard
FPGA	bbbbbbb	F391E2C F391E2V F391E2W F392E2C	F391E2C - AGMF039R47A1E2VR0, C0 F-Tile F391E2V - AGMF039R47A1E2V F391E2W - AGMF039R47A1E2VR0, B0 F-Tile F392E2C - AGMF039R47A2E2VR0, C0 F-Tile
Oscillator Configuration	d	S	S - Standard
Clock Configuration	e	0	0 - Standard
Timing	f	0 C X	0 - None C - Front Panel Connections X - Onboard Circuits Only
QSFP Configuration	g	3	3 - Three QSFPs
MCIO Configuration	h	0 2	0 - No MCIO populated 2 - Two MCIO (Configured as PCIe Root Port)
Heat Sink Configuration	i	2 L	2 - Passive Heatsink L - Liquid Cooled
Mechanical Configuration	j	2	2 - Two-Slot
Flash Configuration	k	0	0 - Default
Miscellaneous Configuration	l	0-9, A-Z	Reserved
Environmental Assembly	m	9	9-RoHS

2.7 Development Tools, Example Designs, and IP

BittWare offers several soft deliverables to help customers develop their FPGA applications:

- **The BittWare Software Development Kit (SDK)** is a cross-platform collection of drivers, libraries, modules, and utilities that aid you in debugging and developing applications using BittWare PCIe cards. The SDK is free for 1 year, then requires a yearly maintenance fee.
- **The BittWare Card Support Package (CSP) for the SDK** contains card specific FPGA Gateware and Software to develop on your FPGA cards. The CSP contains several items specific to your FPGA card:
    - Card Test (previously known as Built-In Self-Test, or BIST)
    - Card documentation
    - BittWare gateware and software example designs
    - Software utilities
- **Altera Quartus Prime Pro licenses** –License, downloads, documentation, and support are available at Altera.com.
- **Altera FPGA IP cores** – Many FPGA IP blocks are available as part of Altera Quartus Prime Pro; however, some others are add-on purchases. Downloads, documentation, and support are available at Altera.com.

BittWare also works very closely with FPGA IP developers for solutions based on DPDK, NVMe, etc. Contact your BittWare sales representative for more information at https://www.bittware.com/contact/.

2.8 TeraBox Server Integration

When it comes to development, TeraBox servers are delivered pre-integrated with your choice of BittWare FPGA accelerators. The TeraBox servers are pre-configured with your choice of operating system and FPGA development tools. This allows you to develop and deploy quicker with reduced risk and cost.

TeraBox servers are also deployment-ready for mission-critical applications. BittWare can take care of qualification testing as well as branding. TeraBox servers can be configured to include your host-based application as well as pre-loaded FPGA bitstreams executables, which translates to the servers being ready to run as soon as your customer receives them.

BittWare supports a variety of leading server vendors. As part of Molex, we can handle global supply chain and logistics. We can cater to a range of application environments such as data center and at the edge. Lastly, through OEM programs, you have the option of purchasing selected TeraBox servers directly from server vendors such as Dell, HPE, and Lenovo.

For more information, contact your BittWare Sales representative or visit https://www.bittware.com/fpga/servers-systems/.

3 Board Setup

3.1 Handling, Unpacking, and Shipping Tips

Warning! The IA-860m contains electro-static discharge (ESD) sensitive devices. Be sure to follow the standard handling procedures for ESD sensitive devices, taking proper precautions to ground yourself and the work area before removing the board from its static shielding bag. If you fail to follow proper handling procedures, you could damage the board.

3.1.1 ESD Handling Tips

Effective ESD control and proper ESD handling will maintain the reliability of your BittWare products. Please follow the guidelines listed below to avoid ESD damage to the IA-860m.

- Transport the board only in ESD shielding bags or shielding containers.
- Do not remove the board from its static shielding bag when outside an EPA (ESD Protected Area).
- Wear a grounding wrist strap when handling the board. BittWare also recommends using foot/heel straps in combination with static dissipative flooring.
- When handling the board, hold it by its edges, being careful not to touch any of its components.
- All work benches should be properly grounded and have a conductive surface to eliminate ESD. Placing the board on top of the static shielding bag does not offer any ESD protection.

NOTE: For more information on development of an ESD Control program, contact BittWare or refer to ANSI/ESD S20.20-2007.

3.1.2 Unpacking the IA-860m

To unpack the card:

1. Observe all precautions described in the ESD Handling Tips above to prevent damage from electro-static discharge (ESD).
2. Carefully remove the card from the shipping box. Save the box and packing materials in case you need to reship the card.
3. Carefully examine the card, checking for damage. If the board is damaged, do not install it. Contact BittWare technical support.

3.1.3 Handling Instructions for Connectors and Cabling

QSFP/QSFP-DD Insertion Instructions:

1. Before handling QSFP/QSFP-DD modules, ensure you are following proper electrostatic discharge (ESD) precautions to prevent damage.
2. Remove the QSFP/QSFP-DD module from its protective packaging and remove any dust cover if present.
3. Hold the QSFP/QSFP-DD module between your thumb and forefinger, ensuring correct orientation with the keying on the module aligning with the keying on the cage.
4. Gently insert the QSFP/QSFP-DD module into the cage, making sure it is right side up and correctly aligned. If resistance is felt, do not force the module; double-check the alignment and try again.
5. Apply even pressure until the module clicks into place, indicating it is fully seated. The maximum insertion force should not exceed 90 N as per QSFP-DD MSA limits.

QSFP/QSFP-DD Removal Instructions:

1. To remove a QSFP/QSFP-DD module, first secure the cable or module within your hand.
2. Pull the latch release away from the cage until the module is released from the cage's latching mechanism.
3. Once unlatched, gently pull the QSFP/QSFP-DD module straight out of the cage. The maximum extraction force should not exceed 50 N as per QSFP-DD MSA limits.

Additional Notes:

- QSFP/QSFP-DD modules are keyed to prevent incorrect insertion. If resistance is encountered, ensure the module is not upside down and that it is aligned correctly before reinserting.
- The insertion and removal cycles for a QSFP/QSFP-DD module are rated for 50 cycles as defined by the QSFP-DD MSA.

3.1.4 Shipping the IA-860m

Should you need to ship the IA-860m back to BittWare, please pack it in its original packaging to avoid damage during shipping.

If you are shipping the card as part of an integrated server, it is your responsibility to ensure that the bracket, packaging, and shipping materials are adequate to prevent damage during shipment. When BittWare provides systems pre-integrated into a server, we ship the integrated product on a pallet to minimize the chance of damage. We recommend this method for customer shipments of integrated systems as well.

3.1.5 Hot Surface Warning

When the IA-860m is operational, the card generates heat. The heat is dispersed using various heatsinks and the rear stiffening frame. Take care on any IA-860m exposed metal surface as it may be too hot to touch.

3.2 Where to find:

- **Installation Instructions**: To get started with your board, we recommend following the installation procedure in the IA-860m Getting Started Guide. The Getting Started Guide is available on the Developer Site on the product page for the IA-860m.
- **Development Tools**: The BittWare SDK is a suite of development tools that provides the main interface between the IA-860m and the host system. When your maintenance is active, you can download the SDK latest version and view the SDK documentation on the SDK Support Center section of the Developer Site.
- **FPGA Card Test, Examples, and Software Utility**: These items are available in the IA-860m Card Support Package for the BittWare SDK. A variety of examples and reference designs are available for you to use as a starting point. You can download these from the IA-860m product page on the BittWare Developer Site.
- **Card Documentation:** All card documentation is available for download on the IA-860m product page on the BittWare Developer Site.

Note: The latest versions of the Software Developer Kit and the Card Support Package are only available to customers with an active SDK maintenance contract.

3.3 Warranty

This section outlines the handling guidelines that are allowed within the warranty. Always follow the ESD Handling Tips (see ESD Handling Tips). Do not move or replace any component that was installed by BittWare (DIMMs, cables, etc.) without reaching out to BittWare support. The support team will ensure these parts are replaced safely to avoid any possible damage to the card; in many cases an RMA will be required. Moving these components without recommendation from the support team will void the warranty of the card.

Other components that were not preinstalled (QSFPs, cables, etc.) can be moved or replaced.

For any clarification on operations allowed under the warranty, please reach out to BittWare. See Contacting BittWare for instructions on how to contact BittWare Support to ask technical questions.

3.4 RMA – Returning your product to BittWare

Before BittWare issues an RMA, we will attempt to fix any issues remotely. We also capture as much debugging information as possible to help our production team replicate the issue at our factory. This process ensures a quicker resolution, and in many cases avoids having to return the card back to BittWare.

RMA resolution time varies depending on the issue and the amount of investigation, retest, and rework required. The lead time for replacement parts and the availability of our rework factory also impacts the RMA resolution time. We can estimate the RMA resolution time when we receive the RMA board at our factory.

See Contacting BittWare for instructions on how to contact BittWare Support to request an RMA.

3.5 Card Test

The IA-860m is delivered preprogrammed with a Card Test application that verifies the key features of the product. Refer to the BittWare *IA-860m Getting Started Guide* for instructions on how to run the Card Test application. The Card Test is a useful example of how to use all the features of the IA-860m and is available for download on the BittWare Developer Site.

The Card Test design demonstrates how to use all board features and should be used by HDL developers as the main reference and documentation. The Card Test is an example design which instantiates Altera IP blocks as required for the IA-860m hardware. The Card Test contains IP to access the features of the Board Management Controller (BMC), the Altera PCIe Hard IP, etc.

3.6 FPGA Configuration

The IA-860m can automatically load an FPGA design from Flash at power on. There are several ways to program the FPGA:

JTAG Chain using external USB-Blaster or Blaster II – The IA-860m does not incorporate an embedded USB-Blaster II, unlike previous BittWare IA series products. You will need an external Intel/Altera USB programming pod to access the FPGA JTAG. Connecting to the board via USB pod allows access to the JTAG chain with Quartus Programmer. Using this method, you can reconfigure the FPGA directly. The JTAG chain also provides debug access to the board and enables the use of various JTAG-based debug utilities such as Intel/Altera's Signal Tap Logic Analyzer and System Console.

User Flash Interface – The on-board 2Gb configuration flash, for FPGA configuration, can be programmed over USB with the FPGA user application image currently. Support is being added to allow programming of the configuration flash via the FPGA design if it includes the **BittWare BMC3 IP** block. After you have reprogrammed the flash, the FPGA will be configured with the updated design at the next power cycle or after you launch a soft reconfigure request.

The Intel/Altera Quartus tools cannot be used to program the flash as the FPGA is not directly attached to the flash on the IA-860m. You will need to use the SDK bw_bmc_fpga_load utility to program the Flash.

The current tested method of programming the flash is via USB (by using a .rbf file).

For details on FPGA configuration, refer to the IA-860m FPGA Developer Guide.

4 FPGA

4.1 User FPGA Supported Devices

The following is a list of FPGA devices that this card supports:

Table 5: Supported FPGA Devices

Part Number	Description
AGMF039R47A1E2VR0 (engineering silicon)	Altera Agilex AGMF039 in a R47A(4700A) package Core speed grade -2 XCVR speed grade -1 HPS 32GB HBM2e
AGMF039R47A1E2V (default; production silicon)	Altera Agilex AGMF039 in a R47A(4700A) package Core speed grade -2 XCVR speed grade -1 HPS 32GB HBM2e
AGMF039R47A2E2VR0 (engineering silicon)	Altera Agilex AGMF039 in a R47A(4700A) package Core speed grade -2 XCVR speed grade -2 HPS 32GB HBM2e

4.2 FPGA Implementation Details

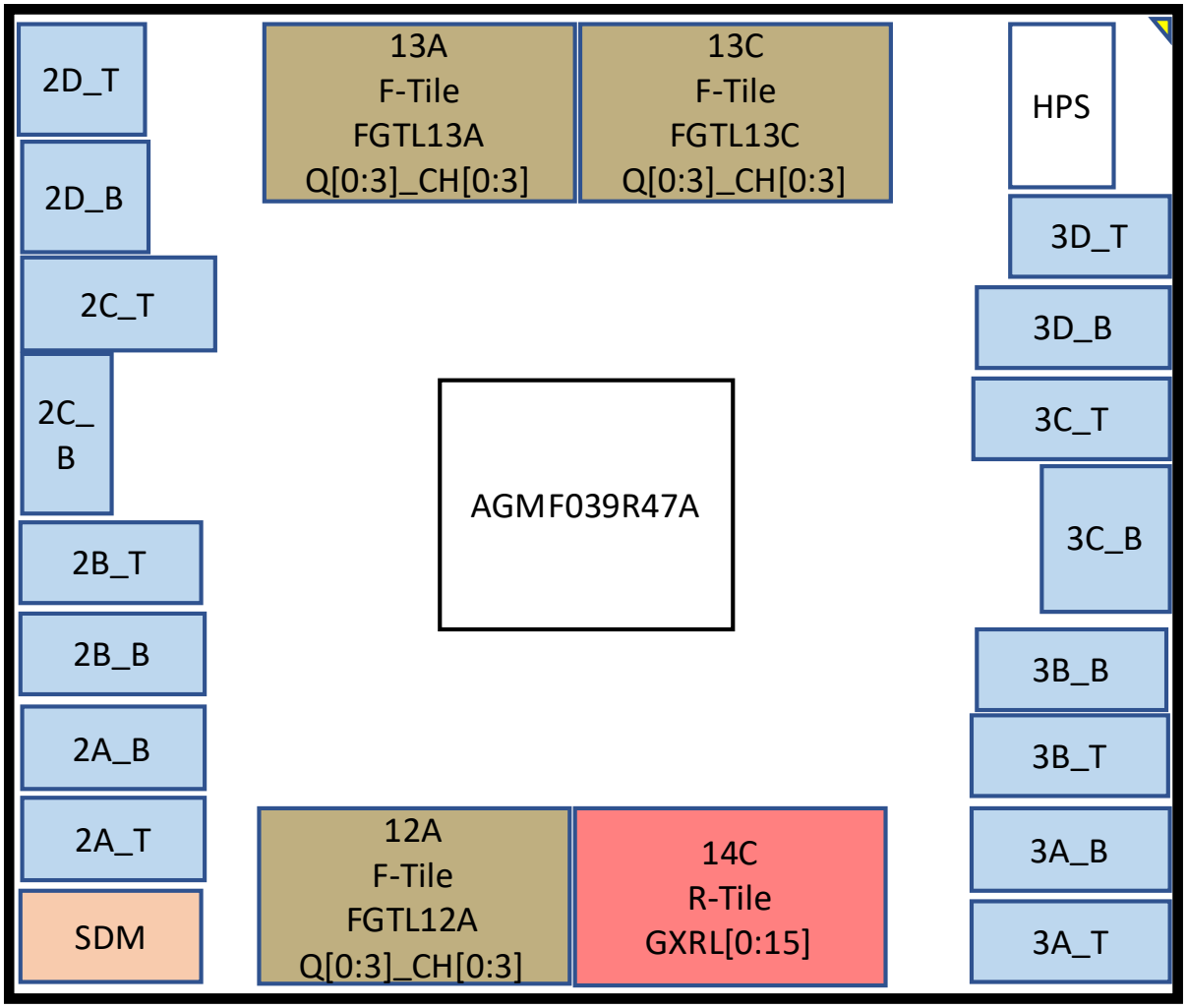
4.2.1 FPGA Bank Usage

The FPGA banks are powered by the supplies given in Table 6. FPGA core voltage (V_{core}) is 0.81V by default and adjusted automatically to the appropriate VID level by the BMC.

Table 6: FPGA Voltage Settings

Signals	Bank	Bank IO Voltage
CXL16/PCIe x16	14C	0.9V/1.0V/1.8V
FPGA Configuration I/O	SDM	1.8V
HPS	HPS	1.8V
LEDS, SPI & Misc	2A	1.2V
MCIO	13A	0.8V/1.0V/1.8V
QSFP0, 1 and, 2	12A,13A,13C	0.8V/1.0V/1.8V

Figure 5: FPGA Bank Usage



4.2.2 FPGA Hard IP Usage

The IA-860m uses the following IP on the FPGA:

Table 7: FPGA Hard IP

Hard IP	Usage	Tile
Multi-rate hard MAC+FEC for 10/25/100/200/400GbE	3x QSFP-DD channels (1 hard IP per QSFP-DD)	F-tile
PCIe	x16 Gen5 interface (CXL support)	R-tile

Refer to the FPGA Developer Guide for details on the Hard IP mapping.

4.2.3 HPS

The Hard Processor System in the FPGA supports the following:

- Dedicated NAND flash
- Dedicated DDR4 (4GB x40 bits)
- UART
- Standard mode
- HPS JTAG accessible via FPGA JTAG

Refer to the FPGA Developer Guide for more detail.

Table 8: HPS Signal Connections

FPGA Pin	Signal Description	FPGA Block
T13	HPS_CLK	HPS
UART		
H9	HPS_UART_TXD	HPS
K3	HPS_UART_RXD	HPS
Flash		
U10	HPS_NAND_D0	HPS
U2	HPS_NAND_D1	HPS
T3	HPS_NAND_D2	HPS
P9	HPS_NAND_D3	HPS
N8	HPS_NAND_D4	HPS
P1	HPS_NAND_D5	HPS
P11	HPS_NAND_D6	HPS
N2	HPS_NAND_D7	HPS
T11	HPS_NAND_WE_L	HPS
T1	HPS_NAND_RE_L	HPS
T9	HPS_NAND_WP_L	HPS
P3	HPS_NAND_CLE	HPS
L8	HPS_NAND_ALE	HPS
U6	HPS_NAND_RB_L	HPS
K7	HPS_NAND_CE_L	HPS

5 PCIe Interface

5.1 Mechanical Details

5.1.1 PCIe Card Form Factor

The IA-860m is a standard-height, full-length, dual-width PCIe add-in card with a 16-lane electrical and 16-lane mechanical interface. The PCIe interface complies with the PCIe 5.0 specification. Note that elements of the PCI-SIG CEM6 specification have been incorporated in the IA-860m for improved future system compatibility.

5.1.2 PCIe Host Interface

The IA-860m card has a 16-lane mechanical and electrical PCIe 5.0 interface. The IA-860m does not feature a dedicated PCIe device for PCIe host transfers; the user FPGA design must include the Altera PCIe Hard IP core.

Altera supports multiple configurations of the PCIe core as part of QSYS. You can set up the Altera IP core for anything from 1 lane at PCIe 1.0 to 16 lanes at PCIe 5.0.

The PCIe interface capabilities and features:

- Host PCIe bandwidth up to 64 GB/s[3] (16 lanes at 32Gbps – PCIe 5.0)

5.1.3 PCIe Endpoint Characteristics

The card is preprogrammed with the Card Test when shipped from the BittWare factory. When connected to a PCIe host, the card will enumerate on the PCIe bus with the following details:

- PCI Vendor ID: 0x12BA
- PCI Device ID: 0x0076

The PCIe end-points properties are accessible with the `lspci` command on Linux or using the Windows Hardware Manager.

5.2 Interface Description

5.2.1 PCIe Enumeration

The PCIe specification requires that a PCIe endpoint be ready for PCIe enumeration within 100ms of the host system powering on. Agilex by default uses an autonomous HIP mode which brings up PCIe before the rest of the FPGA is configured. For FPGA cards, it means that the FPGA should be configured and out of reset within 100ms of power on. However, this requirement is more often widened by host servers and workstations effectively allowing the FPGA more time to complete its configuration.

[3] Maximum theoretical data rate for 16 lanes of PCIe 5.0; the actual host bandwidth depends on the host hardware (motherboard, chipset, processor, etc.), the PCIe IP settings, and the FPGA design itself.

5.2.2 SMBus Features

The BMC supports MCTP over SMBus on the PCIe interface. This is enabled on all cards with BMC firmware release 0.8.0 and later.

5.2.3 PCIe Reset Requirements

Since the IA-860m is a PCIe card, it is a slave to a host processor that is the root complex of the PCIe bus. Therefore, the reset for this board comes through the PCIe bus from the host.

The mechanism that supports a reliable initialization of the firmware and software running on the IA-860m is as follows:

1. The board powers up and supplies are sequenced by the BMC, after which the board comes out of reset.
2. When the power supplies are stable, the BMC LED (LED1) blinks green, the configuration logic is released, and the FPGA configuration starts.
3. The BMC then programs the clock chip.
4. After FPGA configuration, PCIe training and reset should occur.
5. The release of the PCIe reset by the host also deactivates the global reset to the internal FPGA design.
6. After PCIe enumeration, a soft reset comes from the PCIe core to the rest of the internal FPGA logic to start the firmware.

5.2.4 PCIe Pinout

Table 9 shows the FPGA pins used for the PCIe interface.

Table 9: FPGA Pins used for Host PCIe (x16) Interface

FPGA Pin	Signal Description	Tile
CG68	PCIe Host Lane 0 RX (P)	Bank 14C
CH69	PCIe Host Lane 0 RX (N)	Bank 14C
CC68	PCIe Host Lane 1 RX (P)	Bank 14C
CD69	PCIe Host Lane 1 RX (N)	Bank 14C
BW68	PCIe Host Lane 2 RX (P)	Bank 14C
BY69	PCIe Host Lane 2 RX (N)	Bank 14C
BV65	PCIe Host Lane 3 RX (P)	Bank 14C
BU66	PCIe Host Lane 3 RX (N)	Bank 14C
BR68	PCIe Host Lane 4 RX (P)	Bank 14C
BT69	PCIe Host Lane 4 RX (N)	Bank 14C
BP65	PCIe Host Lane 5 RX (P)	Bank 14C
BN66	PCIe Host Lane 5 RX (N)	Bank 14C
BL68	PCIe Host Lane 6 RX (P)	Bank 14C
BM69	PCIe Host Lane 6 RX (N)	Bank 14C
BK65	PCIe Host Lane 7 RX (P)	Bank 14C
BJ66	PCIe Host Lane 7 RX (N)	Bank 14C
BG68	PCIe Host Lane 8 RX (P)	Bank 14C

BH69	PCIe Host Lane 8 RX (N)	Bank 14C
BF65	PCIe Host Lane 9 RX (P)	Bank 14C
BE66	PCIe Host Lane 9 RX (N)	Bank 14C
BC68	PCIe Host Lane 10 RX (P)	Bank 14C
BD69	PCIe Host Lane 10 RX (N)	Bank 14C
BB65	PCIe Host Lane 11 RX (P)	Bank 14C
BA66	PCIe Host Lane 11 RX (N)	Bank 14C
AW68	PCIe Host Lane 12 RX (P)	Bank 14C
AY69	PCIe Host Lane 12 RX (N)	Bank 14C
AV65	PCIe Host Lane 13 RX (P)	Bank 14C
AU66	PCIe Host Lane 13 RX (N)	Bank 14C
AR68	PCIe Host Lane 14 RX (P)	Bank 14C
AT69	PCIe Host Lane 14 RX (N)	Bank 14C
AP65	PCIe Host Lane 15 RX (N)	Bank 14C
AN66	PCIe Host Lane 15 RX (P)	Bank 14C
CK65	PCIe Host Lane 0 TX (P)	Bank 14C
CG62	PCIe Host Lane 0 TX (N)	Bank 14C
CF65	PCIe Host Lane 1 TX (P)	Bank 14C
CC62	PCIe Host Lane 1 TX (N)	Bank 14C
CB65	PCIe Host Lane 2 TX (P)	Bank 14C
BW62	PCIe Host Lane 2 TX (N)	Bank 14C
BR62	PCIe Host Lane 3 TX (P)	Bank 14C
BL62	PCIe Host Lane 3 TX (N)	Bank 14C
BG62	PCIe Host Lane 4 TX (P)	Bank 14C
BF59	PCIe Host Lane 4 TX (N)	Bank 14C
BC62	PCIe Host Lane 5 TX (P)	Bank 14C
BB59	PCIe Host Lane 5 TX (N)	Bank 14C
AW62	PCIe Host Lane 6 TX (P)	Bank 14C
AV59	PCIe Host Lane 6 TX (N)	Bank 14C
AR62	PCIe Host Lane 7 TX (P)	Bank 14C
AP59	PCIe Host Lane 7 TX (N)	Bank 14C
CJ66	PCIe Host Lane 8 TX (P)	Bank 14C
CH63	PCIe Host Lane 8 TX (N)	Bank 14C
CE66	PCIe Host Lane 9 TX (P)	Bank 14C
CD63	PCIe Host Lane 9 TX (N)	Bank 14C
CA66	PCIe Host Lane 10 TX (P)	Bank 14C
BY63	PCIe Host Lane 10 TX (N)	Bank 14C
BT63	PCIe Host Lane 11 TX (P)	Bank 14C
BM63	PCIe Host Lane 11 TX (N)	Bank 14C
BH63	PCIe Host Lane 12 TX (P)	Bank 14C

BE60	PCIe Host Lane 12 TX (N)	Bank 14C
BD63	PCIe Host Lane 13 TX (P)	Bank 14C
BA60	PCIe Host Lane 13 TX (N)	Bank 14C
AY63	PCIe Host Lane 14 TX (P)	Bank 14C
AU60	PCIe Host Lane 14 TX (N)	Bank 14C
AT63	PCIe Host Lane 15 TX (N)	Bank 14C
AN60	PCIe Host Lane 15 TX (P)	Bank 14C

6 External Interfaces

6.1 Overview

Table 10: External Interface Summary

Feature	Ref Des	Width	Max Rating	Spec(s)
PCIe	P1	x16	Gen5 (32Gbps)	PCI Express Base Specification Revision 5.0, Version 1.0
GPIO	J10	x1	2Mbps	1.2V at FPGA and 3.3V at connector
QSFP-DD	J3 (QSFP0) J4 (QSFP1) J5 (QSFP2)	x8	28G NRZ or 56G PAM4	
MCIO	J7	2x4 or 1x8	16G/25G	PCI Express Base Specification Revision 4 / Serial-Lite (25G)
JTAG[4]	J10	x1	16Mbps	
USB in	J11	x1	480Mbps	USB 2.0
USB out	J14	x1	480Mbps	USB 2.0
1PPS	J17	x1	1 Hz	LVTTL (2.5V to 3.3V) Pulse per Second
RefClk	J15	x1	10MHz	200mV to 3V3 pk-pk

6.2 QSFP-DDs

The IA-860m features three QSFP-DD ports. The QSFP-DD high-speed interfaces are directly driven from IP within the user FPGA design. Altera provides IP cores for multiple high-speed protocols compatible with the IA-860m which all have their own reference clock requirements. The IA-860m is populated with an on-board frequency clock device which, by default, feeds a 156.25 MHz clock to the dedicated F-tile global clock FPGA pins.

6.2.1 Supported Speeds

A range of protocols can be implemented using Altera's IP cores. These IP cores may require different reference clock frequencies. The IP Library contains several pre-set files and automated rule checks that allow you to quickly target the FPGA with multiple network protocols.

BittWare allocates 24 dedicated MAC addresses per IA-860m. These addresses are programmed in the ID PROM. The BMC controls access to the QSFP-DDs control/status signals.

The FPGA supports three QSFP-DD interfaces connected to three F-tiles. Each F-tile on the IA-860m can support the following protocols with hard IP:

- 1x 400GbE-8
- 2x 200GbE-4
- 4x 100GbE-2
- 8x 10/25/50GbE-1
- PAM4 supported (up to 53.125 Gbps)

[4] JTAG is not built into the card. The IA-860m requires an external JTAG debugging pod.

- NRZ supported (up to 25.78156 Gbps)

For QSFP-DD module power classes, the supported configurations are as follows: up to three modules at Power Class 5 or up to two modules at Power Class 7. To ensure optimal QSFP-DD thermal performance, it is recommended that the airflow direction be set to the reverse airflow direction, as detailed in 12.2.

6.2.2 QSFP-DD Clocking

Each FTILE clock connects to that F-tile's global clock network.

Table 11: F-tile Clock Connections

FPGA Pin	Clock Signal	FPGA Bank
DK59	FTILE12A_QSFP_REFCLK_P	Bank 12A
DJ60	FTILE12A_QSFP_REFCLK_N	Bank 12A
DE14	FTILE13A_QSFP_REFCLK_P	Bank 13A
DF13	FTILE13A_QSFP_REFCLK_N	Bank 13A
BW14	FTILE13C_QSFP_REFCLK_P	Bank 13C
BY13	FTILE13C_QSFP_REFCLK_N	Bank 13C

6.2.3 FPGA to QSFP Pin Mapping

Each QSFP connects to an FPGA F-tile bank:

- QSFP0 connects to F-tile Bank 12A
- QSFP1 connects to F-tile bank 13A
- QSFP2 connects to F-tile Bank 13C.

These are designed for up to 28Gbps NRZ or 56Gbps PAM4[5] encoded signaling rate. Quads 2 and 3 of the F-tiles are used for connections to the QSFP-DDs. The traces are designed to meet the OIF CEI-28G-VSR specification requirements. The Altera QSF constraints file is the point of reference for pin mappings; however, *Table 12: QSFP-DD 0* Pinout Table illustrates how the QSFP-DD spec pin naming correlates to the design naming.

Table 12: QSFP-DD 0 Pinout Table

Signal	Direction to FPGA	FPGA Pin	QSFP pin
QSFP0_RX_P0	Input	CL68	18
QSFP0_RX_N0	Input	CM69	17
QSFP0_RX_P1	Input	CR68	21
QSFP0_RX_N1	Input	CT69	22
QSFP0_RX_P2	Input	CW68	15
QSFP0_RX_N2	Input	CY69	14
QSFP0_RX_P3	Input	DC68	24
QSFP0_RX_N3	Input	DD69	25
QSFP0_RX_P4	Input	DG68	56
QSFP0_RX_N4	Input	DH69	55
QSFP0_RX_P5	Input	DK65	59
QSFP0_RX_N5	Input	DJ66	60

5 The QSFPs are tested to 25G and 53G.

QSFP0_RX_P6	Input	DL68	53
QSFP0_RX_N6	Input	DM69	52
QSFP0_RX_P7	Input	DP65	62
QSFP0_RX_N7	Input	DN66	63
QSFP0_TX_P0	Output	CL62	37
QSFP0_TX_N0	Output	CM63	36
QSFP0_TX_P1	Output	CP65	2
QSFP0_TX_N1	Output	CN66	3
QSFP0_TX_P2	Output	CR62	34
QSFP0_TX_N2	Output	CT63	33
QSFP0_TX_P3	Output	CV65	5
QSFP0_TX_N3	Output	CU66	6
QSFP0_TX_P4	Output	CW62	75
QSFP0_TX_N4	Output	CY63	74
QSFP0_TX_P5	Output	DB65	40
QSFP0_TX_N5	Output	DA66	41
QSFP0_TX_P6	Output	DC62	72
QSFP0_TX_N6	Output	DD63	71
QSFP0_TX_P7	Output	DF65	43
QSFP0_TX_N7	Output	DE66	44

Table 13: QSFP-DD 1 Pinout Table

Signal	Direction to FPGA	FPGA Pin	QSFP pin
QSFP1_RX_P0	Input	ED5	18
QSFP1_RX_N0	Input	EC4	17
QSFP1_RX_P1	Input	EA2	21
QSFP1_RX_N1	Input	EB1	22
QSFP1_RX_P2	Input	DY5	15
QSFP1_RX_N2	Input	DW4	14
QSFP1_RX_P3	Input	DU2	24
QSFP1_RX_N3	Input	DV1	25
QSFP1_RX_P4	Input	DT5	56
QSFP1_RX_N4	Input	DR4	55
QSFP1_RX_P5	Input	DN2	59
QSFP1_RX_N5	Input	DP1	60
QSFP1_RX_P6	Input	DM5	53
QSFP1_RX_N6	Input	DL4	52
QSFP1_RX_P7	Input	DJ2	62
QSFP1_RX_N7	Input	DK1	63
QSFP1_TX_P0	Output	EA8	37
QSFP1_TX_N0	Output	EB7	36
QSFP1_TX_P1	Output	DY11	2
QSFP1_TX_N1	Output	DW10	3
QSFP1_TX_P2	Output	DU8	34
QSFP1_TX_N2	Output	DV7	33
QSFP1_TX_P3	Output	DT11	5
QSFP1_TX_N3	Output	DR10	6
QSFP1_TX_P4	Output	DN8	75
QSFP1_TX_N4	Output	DP7	74
QSFP1_TX_P5	Output	DM11	40
QSFP1_TX_N5	Output	DL10	41

QSFP1_TX_P6	Output	DJ8	72
QSFP1_TX_N6	Output	DK7	71
QSFP1_TX_P7	Output	DH11	43
QSFP1_TX_N7	Output	DG10	44

Table 14: QSFP-DD 2 Pinout Table

Signal	Direction to FPGA	FPGA Pin	QSFP pin
QSFP2_RX_P0	Input	BL2	18
QSFP2_RX_N0	Input	BK1	17
QSFP2_RX_P1	Input	BG2	21
QSFP2_RX_N1	Input	BF1	22
QSFP2_RX_P2	Input	BH5	15
QSFP2_RX_N2	Input	BJ4	14
QSFP2_RX_P3	Input	BC2	24
QSFP2_RX_N3	Input	BB1	25
QSFP2_RX_P4	Input	BD5	56
QSFP2_RX_N4	Input	BE4	55
QSFP2_RX_P5	Input	AW2	59
QSFP2_RX_N5	Input	AV1	60
QSFP2_RX_P6	Input	AY5	53
QSFP2_RX_N6	Input	BA4	52
QSFP2_RX_P7	Input	AR2	62
QSFP2_RX_N7	Input	AP1	63
QSFP2_TX_P0	Output	BR8	37
QSFP2_TX_N0	Output	BP7	36
QSFP2_TX_P1	Output	BL8	2
QSFP2_TX_N1	Output	BK7	3
QSFP2_TX_P2	Output	BH11	34
QSFP2_TX_N2	Output	BJ10	33
QSFP2_TX_P3	Output	BG8	5
QSFP2_TX_N3	Output	BF7	6
QSFP2_TX_P4	Output	BD11	75
QSFP2_TX_N4	Output	BE10	74
QSFP2_TX_P5	Output	BC8	40
QSFP2_TX_N5	Output	BB7	41
QSFP2_TX_P6	Output	AY11	72
QSFP2_TX_N6	Output	BA10	71
QSFP2_TX_P7	Output	AW8	43
QSFP2_TX_N7	Output	AV7	44

6.2.4 QSFP-DD Control Signals

QSFP-DD control signals are connected to the BMC. These signals can be managed one of two ways:

- Via I^2C reads and writes from the BMC
- Via virtual pins implemented by the BittWare Card Management IP Block – *See the IA-860m FPGA Developer's Reference Guide for more information*

Table 15: QSFP-DD Control Signals

Signal Name	Description	Direction to Module	Connected to
I2C_MISC_SCL (QSFP0)	I^2C Clock	Input	BMC Pin – L13(GPIO_AD_24)
I2C_MISC_SDA (QSFP0)	I^2C Data	Bidirectional	BMC Pin – M15 (GPIO_AD_25)
I2C_PSU_SCL (QSFP2)	I^2C Clock	Input	BMC Pin – P5(GPIOLPSR_09)
I2C_PSU_SDA (QSFP2)	I^2C Data	Bidirectional	BMC Pin – U8(GPIO_LPSR_08)
I2C_QSFP_SCL (QSFP2)	I^2C Clock	Input	BMC Pin – D11 (GPIO_DISP_B1_02)
I2C_QSFP_SDA (QSFP2)	I^2C Data	Bidirectional	BMC Pin – E11 (GPIO_DISP_B1_03)
QSFP0_PRESNT_L	Module installed	Output	BMC via I2C_QSFP_to the GPIO Expander
QSFP0_INT_L	Interrupt	Output	
QSFP0_LP	Low Power Mode	Input	
QSFP0_RST_L	Reset	Input	
QSFP2_PRESNT_L	Module installed	Output	
QSFP2_INT_L	Interrupt	Output	
QSFP2_LP	Low Power Mode	Input	
QSFP2_RST_L	Reset	Input	
QSFP2_PRESNT_L	Module installed	Output	
QSFP2_INT_L	Interrupt	Output	
QSFP2_LP	Low Power Mode	Input	
QSFP2_RST_L	Reset	Input	

6.2.5 Cage and Connector

A double density cage permits up to 8 high-speed links to external devices. This format allows both standard x4 modules and cables in addition to the octal versions. This connector is the same width as a standard cage but adds two more rows which makes it deeper than the quad cage.

- The cage is a TE Connectivity 2342886-3 for 1x3, or a Molex 2031433357 for 1x1
- The connector is a Molex 202718-0100

6.2.6 Validated Cables and Transceiver Settings

The BittWare developer site will maintain a per-product list of internally validated hardware including pluggable transceiver modules and cables and supported peripheral or storage features where appropriate. The developer site product page will also provide any relevant information on test methodology for these validated modules.

6.3 MCIO

The IA-860m has a x8 Mini Cool Edge IO (MCIO) connector for PCIe expansion. The connector is on the top edge of the board. It is a right-angle receptacle (Amphenol PN: G97R22332HR), compatible with vertical 74-contact MCIO cables.

6.3.1 PCIe Root Ports

This connector supports a x8 card to card connection running at line rates up to 25G NRZ. The MCIO can also be configured as two PCIe Gen4 x4 root ports.

6.3.2 Shared I2C Bus

The MCIO shares a common I2C bus with other devices. To avoid a conflict, refrain from using the following 7-bit addresses: 0x20, 0x57, 0x71, and 0x72.

6.3.3 Connector Pinout

The MCIO pinout tables document the default configuration with the card as a root complex.

Table 16: MCIO Connector Pinout

MCIO Signal	Direction To FPGA	FPGA Pin Location	FPGA Signal Name	MCIO pin	MCIO PCIe Function
MCIO_RX_P0	Input	CP1	MCIO_RX_P0	A2	PERp0
MCIO_RX_N0	Input	CN2	MCIO_RX_N0	A3	PERn0
MCIO_RX_P1	Input	CR4	MCIO_RX_P1	A5	PERp1
MCIO_RX_N1	Input	CT5	MCIO_RX_N1	A6	PERn1
MCIO_BP_TYPEA	Output	FM51	MCIO1V2_BP_TYPEA	A8	
MCIO_CWAKEA	Input	FL52	MCIO1V2_CWAKEA	A9	
MCIO_CLKOUT0_P				A11	
MCIO_CLKOUT0_N				A12	
MCIO_RX_P2	Input	CV1	MCIO_RX_P2	A14	PERp2
MCIO_RX_N2	Input	Cu2	MCIO_RX_N2	A15	PERn2
MCIO_RX_P3	Input	CW4	MCIO_RX_P3	A17	PERp3
MCIO_RX_N3	Input	CV5	MCIO_RX_N3	A18	PERn3
MCIO_RX_P4	Input	DB1	MCIO_RX_P4	A20	PERp4
MCIO_RX_N4	Input	DA2	MCIO_RX_N4	A21	PERn4
MCIO_RX_P5	Input	DC4	MCIO_RX_P5	A23	PERp5
MCIO_RX_N5	Input	DD5	MCIO_RX_N5	A24	PERn5
MCIO_BP_TYPEB	Output	FV57	MCIO_1V2_BP_TYPEA	A26	
MCIO_CWAKEB	Input	FU58	MCIO_1V2_CWAKEB	A27	
MCIO_CLKOUT1_P				A30	
MCIO_CLKOUT_N				A29	
MCIO_RX_P6	Input	DF1	MCIO_RX_P6	A32	PERp6
MCIO_RX_N6	Input	DE2	MCIO_RX_N6	A33	PERn6
MCIO_RX_P7	Input	DG4	MCIO_RX_P7	A35	PERp7
MCIO_RX_N7	Input	DH5	MCIO_RX_N7	A36	PERn7
MCIO_TX_P0	Output	CL10	MCIO_TX_P0	B2	PETp0
MCIO_TX_N0	Output	CM11	MCIO_TX_N0	B3	PETn0
MCIO_TX_P1	Output	CP7	MCIO_TX_P1	B5	PETp1
MCIO_TX_N1	Output	CN8	MCIO_TX_N1	B6	PETn1
MCIO_I2C0_SCL	Output	FC56	MCIO_1V2_I2C0_SCL	B8	
MCIO_I2C0_SDA	Output	FB55	MCIO_1V2_I2C0_SDA	B9	
MCIO_PERSTA	Output	K11	MCIO_1V8_PERSTA	B11	
MCIO_CPRSNTA	Output	FR52	MCIO_1V2_CPRSNTA	B12	
MCIO_TX_P_2	Output	CR10	MCIO_TX_P_2	B14	PETp2
MCIO_TX_N_2	Output	CT11	MCIO_TX_N_2	B15	PETn2
MCIO_TX_P_3	Output	CV7	MCIO_TX_P_3	B17	PETp3
MCIO_TX_N_3	Output	Cu8	MCIO_TX_N_3	B18	PETn3
MCIO_TX_P_4	Output	CW10	MCIO_TX_P_4	B20	PETp4
MCIO_TX_N_4	Output	CY11	MCIO_TX_N_4	B21	PETn4
MCIO_TX_P_5	Output	DB7	MCIO_TX_P_5	B23	PETp5
MCIO_TX_N_5	Output	DA8	MCIO_TX_N_5	B24	PETn5
MCIO_I2C1_SCL	Output	FV55	MCIO_1V2_I2C1_SCL	B26	
MCIO_I2C1_SDA	Output	FU56	MCIO_1V2_I2C1_SDA	B27	
MCIO_PERSTB	Output	T7	MCIO_1V8_PERSTB	B29	
MCIO_CPRSNTB	Input	GA58	MCIO_1V2_CPRSNTB	B30	

MCIO Signal	Direction To FPGA	FPGA Pin Location	FPGA Signal Name	MCIO pin	MCIO PCIe Function
MCIO_TX_P_6	Output	DC10	MCIO_TX_P_6	B32	PETp6
MCIO_TX_N_6	Output	DD11	MCIO_TX_N_6	B33	PETn6
MCIO_TX_P_7	Output	DF7	MCIO_TX_P_7	B35	PETp7
MCIO_TX_N_7	Output	DE8	MCIO_TX_N_7	B36	PETn7

6.3.4 Validated MCIO Cables

A list of any validated cables is available on the BittWare developer site (see also section 6.2.6).

6.3.5 MCIO Clocking

The MCIO is clocks are HSCL 100Mhz sourced from clock chip with no SSC. See Clocking for more detail.

6.3.6 MCIO Sideband Access

The MCIO sideband signals are connected to the FPGA fabric via buffers. The PRESTN signal is connected to the HPS bank to allow for PCIe enumeration when an NVME drive is fitted.

Table 17: MCIO Sideband Signal Connections

Designator	Device	VCCA	VCCB	Signal	Direction
U2	SN74AVC	VCC_1V8	VCC_3V3	M2_PEWAKE_L	A to B
				M2_CLKREQ_L	B to A
		FPGA HPS	MCIO	M2_PERST_L	A to B
U4	SN74AVC	VCC_1V8	VCC_3V3	MCIO_PERSTA	A to B
		FPGA HPS	MCIO	MCIO_PERSTB	A to B
U44	SN74AVC	VCC_1V2	VCC_3V3	MCIO_BP_TYPEA	A to B
				MCIO_CWAKEA	B to A
		FPGA IO	MCIO	MCIO_CPRSNTA	B to A
U45	SN74AVC	VCC_1V2	VCC_3V3	MCIO_BP_TYPEB	A to B
				MCIO_CWAKEB	B to A
		FPGA IO	MCIO	MCIO_CPRSNTB	B to A
U53	SN74AVC	VCC_BMC_1V8	VCC_1V2	FPGA_IG_SPI_SCK	A to B
				FPGA_IG_SPI_PCS0	A to B
		BMC	FPGA IO	FPGA_IG_SPI_MOSI	A to B
				FPGA_IG_SPI_MISO	B to A
U55	SN74AVC	VCC_BMC_1V8	VCC_1V2	FPGA_EG_SPI_SCK	B to A
				FPGA_EG_SPI_PCS0	B to A
		BMC	FPGA IO	FPGA_EG_SPI_MOSI	B to A

				FPGA_EG_SPI_MISO	A to B
U56	SN74AVC	VCC_BMC_1V8	VCC_1V2	FPGA_TO_BMC_IRQ	B to A
				BMC_TO_FPGA_IRQ	A to B
		BMC	FPGA IO	FPGA_RST_L	A to B
				BMC_IF_PRESENT_L	B to A
U59	SN74AVC	VCC_BMC_1V8	VCC_3V3	2X6_SENSE0	BMC Controlled
				2X6_SENSE1	B to A
		BMC	PCIE POWER/LED	BMC_LED_G_L	A to B
				BMC_LED_R_L	A to B
U63	SN74AVC	VCC_1V8	VCC_3V3	BMC_FPGA_TCK	B to A
				BMC_FPGA_TDI	B to A
		SDM	BMC	BMC_FPGA_TDO	A to B
				BMC_FPGA_TMS	B to A
U72	SN74AVC	VCC_1V8	VCC_3V3	HPS_UART_RXD	B to A
		FPGA HPS	FTDI	HPS_UART_TXD	A to B
U80	SN74AVC	VCC_1V2	VCC_3V3	EXT_LT_GPIO0	B to A
				EXT_LT_GPIO1	B to A
		FPGA IO	LVDS GPIO	EXT_LT_GPIO2	A to B
U81	SN74AVC	VCC_1V2	VCC_3V3	FPGA_LED_R_L	A to B
		FPGA IO	LED	FPGA_LED_R_L	A to B

6.4 GPIO

Four GPIO channels are connected to the FPGA. The direction of the four GPIO lines are controlled via the FPGA; each has a maximum data rate of 2Mbps, shown in Table 18 and Figure 6. The voltage level is 1.2V at the FPGA and 3.3V at the connector.

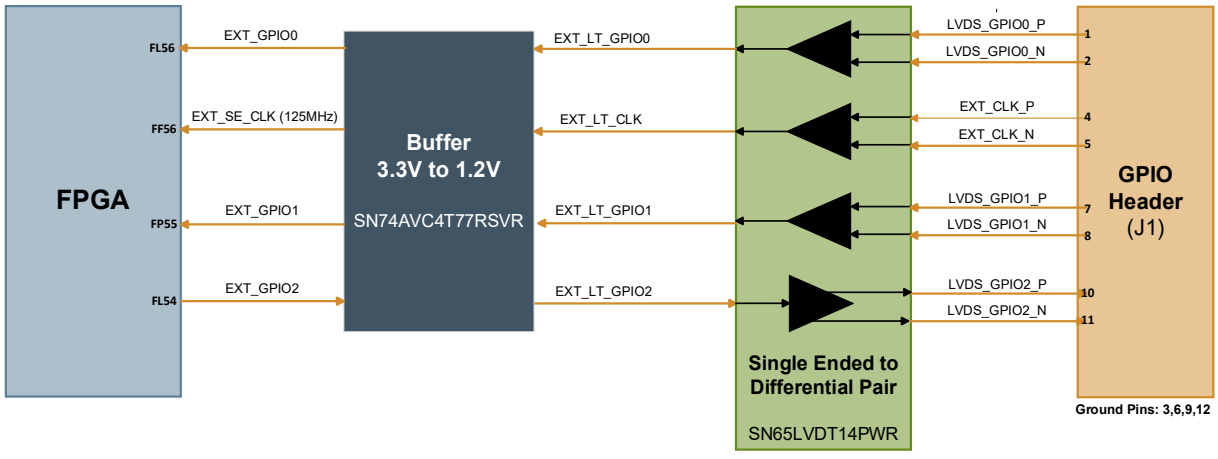
A single-row 12-way Molex Pico-Lock connector (J1) is located on the secondary side of the PCB (Figure 4). Connection to it is made using Molex Pico-Lock housing P/N 50405041291; visit the Molex website at www.molex.com for suitable connector crimp options.

Figure 6 shows the GPIO connections of the FPGA.

Table 18: GPIO Connector & Signal Mapping

Connector Pin	Schematic Name	FPGA Pin	FPGA Signal Name
1	EXT_GPIO0_P	FL56	EXT_GPIO0
2	EXT_GPIO0_N		
3	GND	N/A	N/A
4	EXT_CLK_P	FF56	EXT_SE_CLK
5	EXT_CLK_N		
6	GND	N/A	N/A
7	EXT_GPIO1_P	FP55	EXT_GPIO1
8	EXT_GPIO1_N		
9	GND	N/A	N/A
10	EXT_GPIO2_P	FL54	EXT_GPIO2
11	EXT_GPIO2_N		
12	GND	N/A	N/A

Figure 6: FPGA GPIO Connections



6.5 External Interface Connections

This section describes the connection standards that must be used when connecting to external interfaces on the card. These are described through this document but are summarised in this section for completeness.

Table 19: J10 JTAG Interface

Interface	Board Reference	Pin Name	Connection
JTAG	J10 pin 1	Power Supply	3.3V for external POD access
	J10 pin 2	TCK	3.3V
	J10 pin 3	TDI	3.3V
	J10 pin 4	TDO	3.3V
	J10 pin 5	TMS	3.3V
	J10 pin 6	Ground	0V

Table 20: J11 USB In Rear Panel Interface

Interface	Board Reference	Pin Name	Connection
USB	J11 pin 1	Power Supply	5V for external POD access
	J11 pin 2	USB_N	3.3V (USB)
	J11 pin 3	USB_P	3.3V (USB)
	J11 pin 4	Ground Shield	0V
	J11 pin 5	Ground	0V

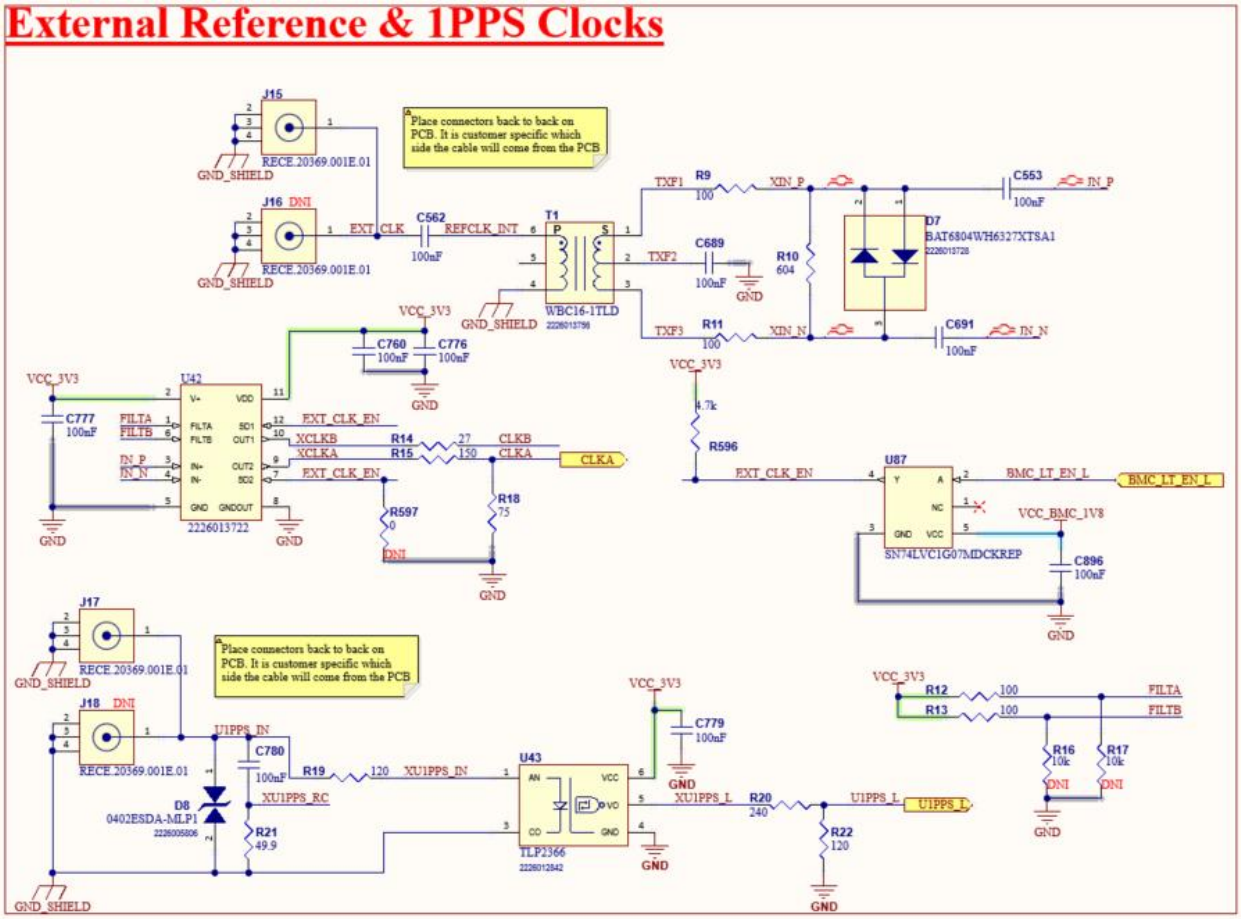
Table 21: J14 USB Out Interface

Interface	Board Reference	Pin Name	Connection
USB	J14 pin 1	Power Supply	5V for external POD access
	J14 pin 2	USB_N	3.3V (USB)
	J14 pin 3	USB_P	3.3V (USB)
	J14 pin 4	Ground Shield	0V
	J14 pin 5	Ground	0V

Table 22: J15 and J17 External Reference Clock Connections

Interface	Board Reference	Pin Name	Connection
External reference Clock (see Figure 7)	J15 pin 1	EXT_CLK	10 MHz reference clock into 50ohm load. The input circuit can be found at https://www.analog.com/media/en/reference-design-documentation/design-notes/dn514f.pdf
External 1PPS Clock (see Figure 7)	J17 pin 1	U1PPS_IN	Input on state: 4.5mA (min), 15mA (max) Input on state (Vf): 1.45V (min), 1.85V (max) Input off state: 0.8v (max)

Figure 7: External Reference Clocks Circuit



7 Memory

7.1 HBM2e

The FPGA has two integrated HBM2e memory stacks in the package. Each DRAM stack contains the following:

- 16 GB density per stack (totalling 32 GB density per device)
- 410 GBps memory bandwidth per stack, 820 GBps total aggregate memory bandwidth per device
- 8 independent channels, each 128 bits wide, or 16 independent pseudo channels, each 64 bits wide (in a pseudo channel mode)
- Data transfer rates up to 3.2 Gbps, per signal, between core fabric and HBM2e DRAM memory

Altera® Agilex™ M-Series devices can interface directly from the fabric to the HBM2e or through the hardened memory NoC.

7.2 DDR4

7.2.1 HPS DDR4

The IA-860m has a discrete bank of DDR4-2666 for the Hard Processor System (HPS) in the FPGA. The bank is 4GB x40 (x32 + 8-bit ECC).

7.2.2 Clocking the DDR4 Banks

The Altera DDR4 SDRAM IP is supplied with 133.3333 MHz reference clocks as detailed in Table 23.

Table 23: DDR4 Reference Clocks

Source	FPGA Pin	FPGA Signal Name	I/O Standard
SiT95148_0	Y25	HPS_DDR4_REFCLK_P[0]	LVDS18
SiT95148_0	W24	HPS_DDR4_REFCLK_N[0]	LVDS18

7.3 Flash

The 2Gb Flash is used for storing FPGA configuration images. Multiple images can be stored into this flash, dependent upon design size and compression. The flash includes a fallback, user, and factory image scheme. There are two ways in which the flash can be programmed: via USB or PCI. Refer to the IA-860m Getting Started Guide and the SDK documentation for more detail on programming options. Note that in the current release, the USB path is the supported mechanism. For instructions on generating a .rbf file, refer to the FPGA Developer Guide. *The Altera Quartus tools are not a supported method of programming the flash on the IA-860m.*

8 Clocking

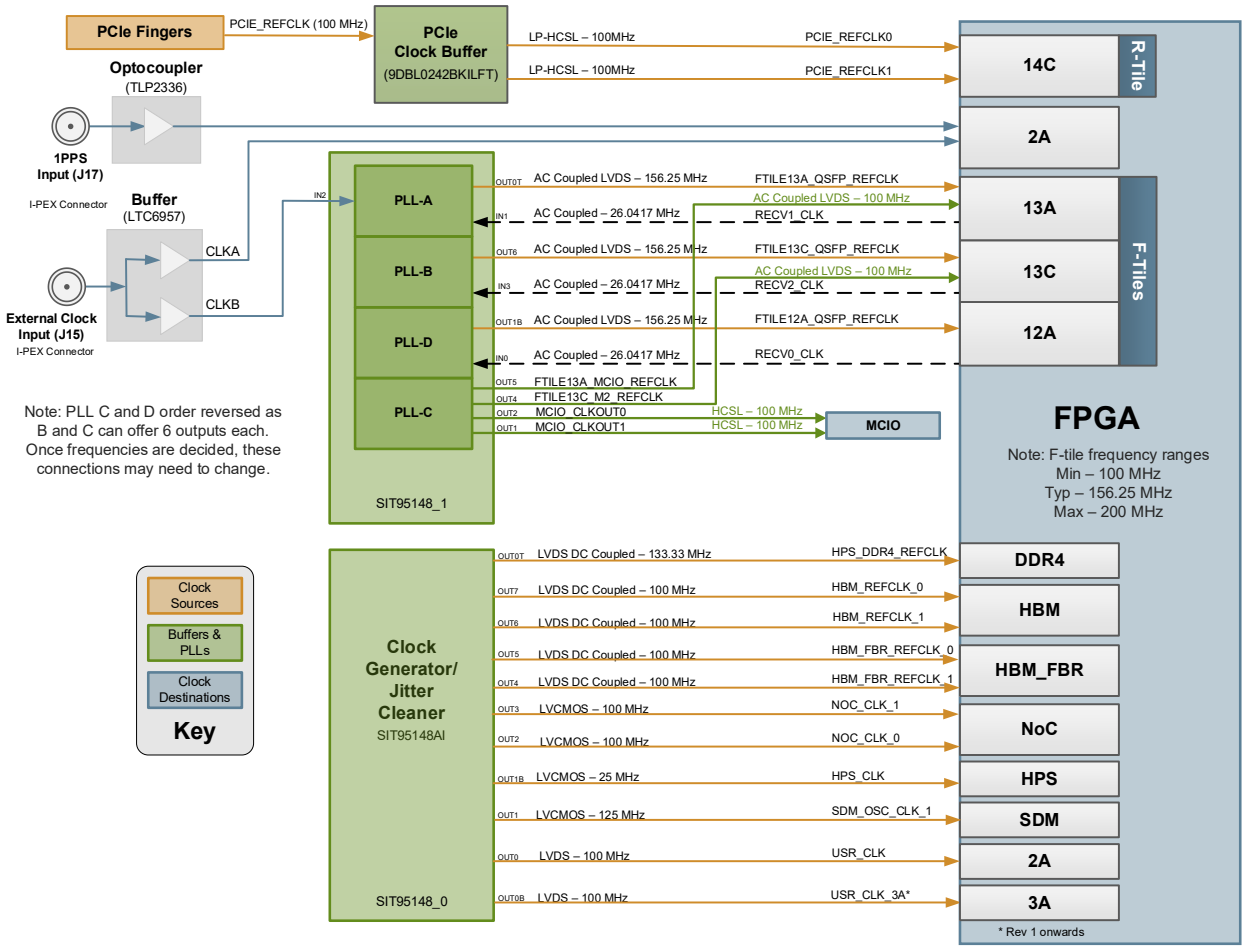
8.1 Clock Circuitry

The clocking circuit on this board provides flexible and quality clock sources to the FPGA and associated circuitry without adding significant cost. Figure 8 illustrates the clock design.

The following clocks sources are available to the FPGA design:

- PCIe clocks
- User clocks
- Memory and general FPGA clocks
- Network clocks
- HPS clock
- 1PPS external synchronization input
- External clock input

Figure 8: Clock Circuitry



8.2 Programmable Clock

The SiTime SIT95148 is a high-performance eleven-output MEMs jitter cleaner and clock synthesizer used to generate the user, DDR4 and network clocks. The SiT95148 integrates a high accuracy MEMS resonator which eliminates the need for an external quartz device.

The SiT95148 is programmed by the BMC via its SPI interface on power-up to the settings described in this section. The device can also be reprogrammed by the user. The Card Support Package design demonstrates how to program the SiT95148 using a configuration file generated through the SiTime Cascade utility.

8.3 Clock Sources

Table 24: Clock Functions and Frequencies

Ref	Clock Source	Schematic Name	Freq. (MHz)	Standard
1	SIT95148_0	HPS_DDR4_REFCLK	133.3333	LVDS18 DC
2	SIT95148_0	HBM_REFCLK0	100	LVDS18 DC
3	SIT95148_0	HBM_REFCLK1	100	LVDS18 DC
4	SIT95148_0	HBM_FBR_REFCLK0	100	LVDS18 DC
5	SIT95148_0	HBM_FBR_REFCLK1	100	LVDS18 DC
6	SIT95148_0	NOC_CLK_1	100	LVCMOS
7	SIT95148_0	NOC_CLK_0	100	LVCMOS
8	SIT95148_0	SDM_OSC_CLK_1	125	LVCMOS
9	SIT95148_0	USR_CLK	100	LVDS18 DC
10	SIT95148_0	HPS_CLK	25	LVCMOS
11	SIT95148_0	USR_CLK_3A	100	LVDS18 DC
12	FPGA	RECV0_CLK	26.0417*	Altera
13	FPGA	RECV1_CLK	26.0417*	Altera
14	FPGA	RECV2_CLK	26.0417*	Altera
15	SIT95148_1	FTILE13A_QSFP_REFCLK	156.25	LVDS33 AC
16	SIT95148_1	FTILE13C_QSFP_REFCLK	156.25	LVDS33 AC
17	SIT95148_1	FTILE13A_MCIO_REFCLK	100	LVDS33 AC
18	SIT95148_1	FTILE13C_M2_REFCLK	100	LVDS33 AC
19	SIT95148_1	M2_REFCLK	100	HCSL 1V8
20	SIT95148_1	MCIO_CLKOUT0	100	HCSL 1V8
21	SIT95148_1	MCIO_CLKOUT1	100	HCSL 1V8
22	SIT95148_1	FTILE12A_QSFP_REFCLK	156.25	LVDS33 AC
23	EXT_CLK	CLKA	10	LVCMOS
24	EXT_CLK	CLKB	10	LVCMOS
25	PCIE	PCIE_REFCLK	100	HSCL-LP
26	BUFFER	PCIE_REFCLK0	100	HSCL-LP
27	BUFFER	PCIE_REFCLK1	100	HSCL-LP
28	1PPS_CLK	U1PPS	1Hz	

*Frequency of recovered clock is design dependent.

8.3.1 PCIe Clock

The PCIe clock is brought to the card via the PCIe finger. The clock is fixed at 100 MHz and is provided by the host motherboard. This clock is then buffered through a 1:2 buffer (PI6CB33202ZDIEX) used throughout the IA-860m for any PCIe bus interfaces.

The Altera PCIe IP must use these reference clocks. Each output uses the 1.8V HCSL I/O standard. See the PCIe standard specification for more information.

8.3.2 User Clocks

An on-board clocking circuit feeds two 100 MHz LVDS DC coupled clock signal to the FPGA. This clock is for general clocking of the fabric. It is not recommended that this clock is changed from its default frequency; however, if this is required contact BittWare for details.

The 25MHz clock for the Hard Processor System in the FPGA is sourced from the SiT95148 synthesizer.

8.3.3 DDR4 Clock

The Altera DDR4 SDRAM IP is supplied with 133.3333 MHz reference clocks sourced from the SiT95148 synthesizer. (See also Clocking the DDR4 Banks.)

8.3.4 HBM Clock

Four LVDS DC coupled clocks are provided for use with HBM, sourced from the SiT95148 synthesizer.

8.3.5 Network Clock

The QSFP-DD modules are driven from dedicated FPGA transceivers. These transceivers require a dedicated reference clock pin to use the cleanest clock source and support high I/O standards with tight jitter tolerances.

The SiT95148 can be configured to generate its outputs (the transceiver reference clocks for the QSFP-DDs) from a combination of its inputs - either on-chip MEMS or a recovered clock from the FPGA. The SiT95148 can be configured so the MEMS is the sole input to the PLLs within the clock chip.

Network Power-on Clock (From SiT95148)

The QSFP-DD bank is fed by one of the SiT95148's LVDS coupled clock output signals. The SiT95148 outputs 156.25 MHz by default at power-on.

Network Recovered Clock

The QSFP-DD bank is fed by one of the SiT95148's LVDS output clocks. The SiT95148 can be used to recover the network clock from the QSFP-DD. In this scenario the FPGA F-Tile outputs a recovered clock which is fed into the SiT95148 input. This is then routed through the clock chip to the FPGA's QSFP clock input.

8.4 Timestamp and Synchronization

The IA-860m includes 1PPS and 10MHz reference clock inputs, these are sourced from SSMB connectors on front panel.

8.4.1 1 PPS Input

The 1PPS signal can be used to provide a means of synchronizing the FPGA timing to an external timing signal. It is an optocoupled input and supports levels of 5.5V. It uses an IPEX MHF3 connector on the PCB that can be wired to a connector directly accessible from the PCIe faceplate (as a board configuration option).

FPGA signal name: U1PPS

8.4.2 External Clock Input

The 10 MHz external clock input can be used to synchronize the FPGA timing to an external timing signal. The clock input can be a sine wave that is 1.41Vpp down to 100mVpp into a 50Ω load or up to 5V. It uses an IPEX MHF3 connector on the PCB that can be wired to a connector directly accessible from the PCIe faceplate (as a board configuration option).

The external clock is buffered and is connected to an input of the SiT95148 jitter cleaner and clock generator as well as to the FPGA fabric.

FPGA signal name: CLKA

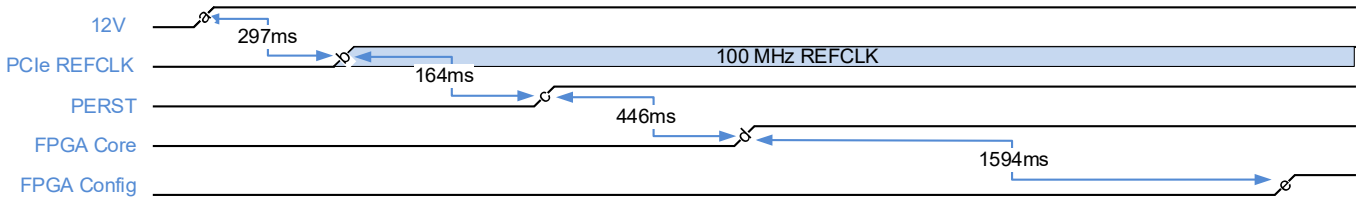
8.5 Start Up Sequence

The IA-860m operates on the PCIe bus. TPVPERL is defined in PCIe CEM to be a minimum of 100ms from 3.3V/12 volts being stable to when PERST# is de-asserted. Note this is a minimum time as defined in the specification. The IA-860m configuration is based on the use of its AVSTx8 interface,

The Agilex series FPGA configuration bitstreams includes PCIe default to activating the PCI HIP Autonomous mode. This mode means that in the period between the initial FPGA section of the bitstream and the completion of the bitstream load when the device enters user mode, the PCIe HIP will return retry requests for configuration TLPs. This extends the PCIe enumeration window timing.

The IA-860m startup timing is shown in Figure 9. The clock files used to program the clock chip are available on the developer site. For more information, refer to the BMC Reference Guide.

Figure 9 IA-860m Start Up Timing[6]



[6] This is an indication of the startup timing. It may change depending on your BMC firmware version, the host system, and the size of the bitstream.

9 Card Management

9.1 BMC

The IA-860m features an advanced system monitoring subsystem like those typically found on today's server platforms. At the heart of the board's monitoring system lies a Board Management Controller (BMC 3.0), which accepts PLDM commands. The BMC provides a wealth of features, including control of power and resets, monitoring of board sensors, FPGA boot loader, voltage overrides, configuration of programmable clocks, access to I^2C bus components, field upgrades, and PLDM messaging. Access to the BMC is via PCIe or USB. The BittWare SDK also provides utilities and libraries for communicating with the BMC components at a higher, more abstract level, allowing developers to remotely monitor the health of the board. Refer to the BMC Reference Guide for more detail.

The IA-860m makes use of the next generation BittWare BMC architecture, BMC 3.0. This is an enhanced BMC implementation compared to previous generation BittWare products, but initial features and capabilities are similar in form for customers. Future features will add capabilities such as security and the ability to stream FPGA configuration via the USB as examples.

9.1.1 Features and Block Diagram

The BMC subsystem is used to control:

- Power and reset sequencing
- Board support peripherals (such as programmable clock synthesizers)
- MCTP/PLDM support

From an environmental perspective, the BMC provides via PLDM:

- Power supply monitoring
- Current monitoring
- Power supply failure logging (volatile and error persistence logging)
- Power consumption and temperature monitoring (FPGA, QSFP28/QSFPDD modules temperatures)
- Over temperature trip protection (FPGA blanks) and logging (volatile and error persistence logging)

This environmental information is accessed via the software board monitor utility which runs over the USB connection.

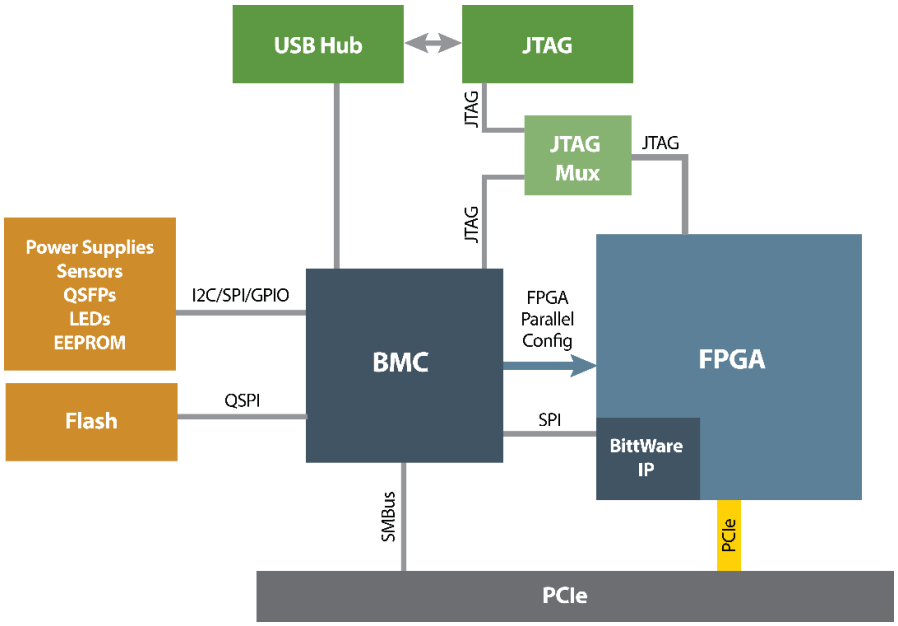
The BMC monitors the FPGA and the board temperature along with voltage, current, and power. The BMC has access to several on-board sensors and implements a shutdown if levels are too high. For a complete list of these sensors and their shutdown values, refer to the *BMC Reference Guide for IA-860m*.

The BMC also provides card-level security features[7]:

- BMC Root of Trust
- BMC and FPGA secure boot
- BMC and FPGA secure upgrade
- Key management

[7] Security capabilities will be added in future soft updates of the BMC 3.0.

Figure 10 BMC 3.0 Block Diagram



9.1.2 BMC Security Features

The BMC 3.0 on the IA-860m includes card-level security features such as key management and signed firmware images. Security is customer-configurable, which allows you to implement the level of security you need for your application. **Security capabilities will be added in future updates of the BMC 3.0.**

The BMC functions as a Root of Trust and can be extended to provide security features around the FPGA and flash. The FPGA bitstream storage in the flash is behind the BMC, accessible via BittWare SDK utilities. All I2C peripherals are accessible only through the BMC instead of directly from the FPGA to the I2C bus. The BMC can also be configured to disable external JTAG access.

9.1.3 RTC and Battery Backup

A real-time clock is implemented in the BMC and is connected to a socket for a backup battery on the card. Note that battery is not fitted by default.

9.1.4 Temperature & Power Limits

The BMC monitors the temperature and power of the board and will initiate controlled shutdown if certain thresholds are exceeded. Standard action is described below:

Table 25: Temperature and Power Thresholds

	Warning	Critical	Fatal
FPGA Over Temperature	87.5C	95C	100C
PCB Over Temperature	75C	80C	85C
QSFP Over Temperature	65C	70C	
Under Temperature	6C	5C	2C
FPGA Core Current	225A	240A	
PCIe Fingers 12V Input Power	63	66	93.75

PCIE External 12V Input Power	270W	300W	320W

The thresholds in the table above are as of BMC 0.9.0. The SDK provides commands to get and set the sensor thresholds: bwbmc_get_sensor_thresholds and bwbmc_set_sensor_thresholds. Refer to the SDK documentation for details.

9.1.5 BMC Utilities

The SDK contains a library for communicating with the BMC via any available data path, including USB or BMC-over-PCIe. Refer to the *BittWare SDK User's Guide* for a list of features and description of the library functions.

The SDK has the following utilities for working with the BMC:

- **bw_bmc_upgrade**: View BMC information, update firmware, reboot the BMC
- **bw_card_monitor**: monitor sensors on the card
- **bw_bmc_configure**: various capabilities, including reboot the BMC
- **bw_bmc_clock_programmer**: read and write clock programs, reprogram clocks
- **bw_bmc_file_ultility**: file access for BMC 3.0
- **bw_bmc_fpga_load**: access configuration flash, view fpga tables
- **bw_bmc_get_logs**: access BMC 3.0 logs

9.1.6 Handling Unused FPGA Pins

Access to the BMC and its associated peripheral devices is possible from the FPGA design. If a user FPGA design does not connect to the BMC, the design must disable access to the FPGA-to-BMC interface by pulling the following pins high:

Pin Name	Location
BMC_IF_PRESENT_N	FM59

The default Quartus settings for unused pins are to tri-state with a weak-pull up. There is no requirement to drive any of the other unused pins to a specific level if the pins listed above are correctly driven.

9.1.7 FPGA Access to the BMC

You can access the BMC via USB and from within your FPGA IP.

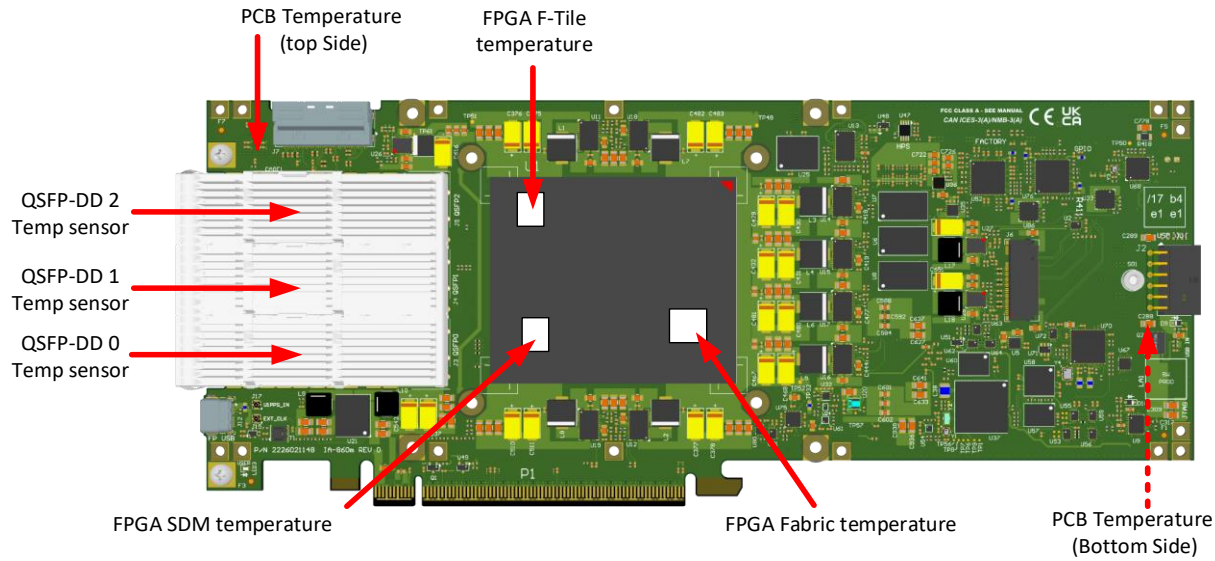
For USB access to the BMC, a rear panel USB C connector is provided for general monitoring and control. The USB interface provides JTAG access to the FPGA and flash via a USB-Blaster-II (driver installed as part of the Quartus installation). An FPGA-driven UART is also provided. See the Error! Reference source not found. section (driver available on the FTDI website).

For FPGA IP access to the BMC, refer to the *FPGA Developer Reference Guide*.

9.2 Thermal Sensors

The card contains several thermal sensors for monitoring FPGA and board temperatures. FPGA temperature sensing diode locations shown are approximate.

Figure 11: IA-860m Temperature Sensor Locations



9.3 I²C Devices

The BMC's hardware I²C ports are directly connected to multiple devices using several dedicated I²C lines. All local devices and the QSFP-DDs support 100 kHz operation.

9.3.1 PCIe I²C

An I²C port is routed to the PCIe fingers from the BMC. This interface is used for system-level monitoring and control via PLDM. It is an isolated interface since in some systems, the signals may be active.

9.3.2 QSFP I²C

An I²C port is routed to each QSFP-DD from the BMC. This interface is used for communicating to the QSFP for monitoring and control. Each QSFP-DD is on a different I2C. The QSFP-DD I2C is isolated from other devices on the bus through a level translator that's enable is controlled by the BMC.

9.3.3 Power Supply I²C

An I²C port is routed to the power supply and the monitoring circuits from the BMC. This interface is used for system level monitoring and control through protocols such as PLDM.

9.3.4 Miscellaneous I²C

An I²C port is routed to other sensor, power, and clock devices. This interface is used for various purposes.

Figure 12: I²C Device Diagram

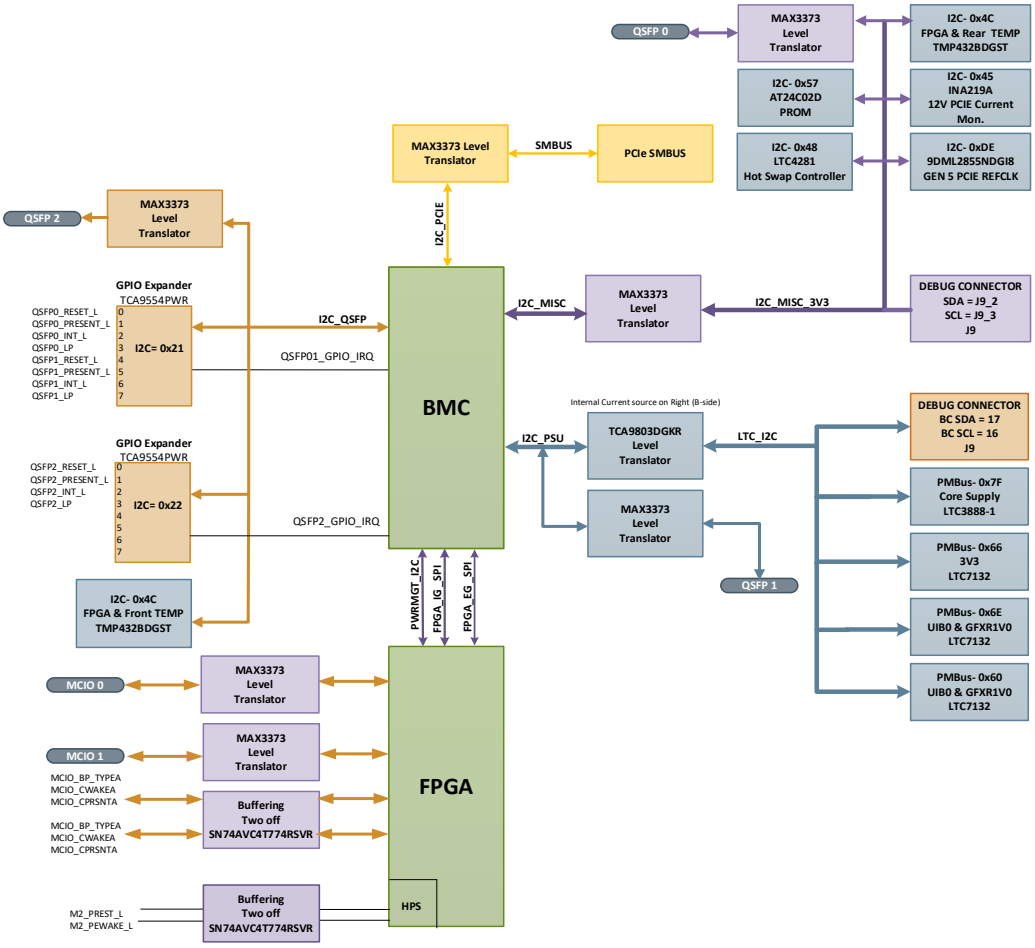


Table 26: FPGA-to-BMC I²C Signals

Signal Name	FPGA Pin
PWRMGT_SDA (SmartVID)	EY65
PWRMGT_SCL (SmartVID)	FH65

Table 27: I²C Addresses

Device	I²C Bus	I²C Address (hex)	Device Part Number	I2C Master
3.3V PCIe Current Monitor	I2C_PSU (LTC_I2C)	0x66	LTC7132	BMC
Core Supply	I2C_PSU (LTC_I2C)	0x7F	LTC3888	BMC
UIB0 & GFXR1V0	I2C_PSU (LTC_I2C)	0x6E	LTC7132	BMC
UIB0 & GFXR1V0	I2C_PSU (LTC_I2C)	0x60	LTC7132	BMC
12V PCIe Current Monitor	I2C_MISC	0x45	INA219A	BMC
Hot Swap Controller	I2C_MISC	0x48	LTC4281	BMC
Temperature Sensor (Rear PCB, FPGA Fabric & FPGA FTILE)	I2C_MISC	0x4C	TMP432	BMC
PCIE Clock Buffer	I2C_MISC	0xDE	9DML2855NDG18	BMC
BittWare ID PROM	I2C_MISC	0x57	AT24C02D (16-Kbit – 2048 x 8)	BMC
QSFP0 & 1 GPIO Expander	I2C_QSFP	0x20	TCA9554	BMC
Temperature Sensor (Front PCB & FPGA SDM)	I2C_QSFP	0x4C	TMP432	BMC
QSFP2 GPIO Expander	I2C_QSFP	0x22	TCA9554	BMC
QSFP-DD0	I2C_MISC	0x50	User defined	BMC
QSFP-DD1	I2C_QSFP	0x50	User defined	BMC
QSFP-DD2	I2C_QSFP	0x50	User defined	BMC
MCIO0	I2C QSFP	External	User defined	BMC
MCIO1	I2C_QSFP	External	User defined	BMC

9.3.5 VPD EPROM

The EPROM is reserved for VPD (Vital Product Data) information and BittWare board information. The EPROM is programmed by BittWare at the time of shipment and then configured to be read-only. The I^2C address for this chip is 0x57; see the “Device Addressing” section of the Atmel AT24C16C datasheet for further details.

The PROM is read-only. For customer production deployments, BittWare can pre-program customer-specific information in the reserved locations of the PROM or enable customers to write these locations.

*Table 28: **ID PROM Data***

Address (hex)	Contents
0x57	BittWare fields
0x50-0x56	Not used

9.3.6 FRU PROM (EEPROM)

The EEPROM is embedded in the BMC. The data format is defined in https://www.dmtf.org/sites/default/files/standards/documents/DSP0257_1.0.0.pdf.

9.4 SmartVID

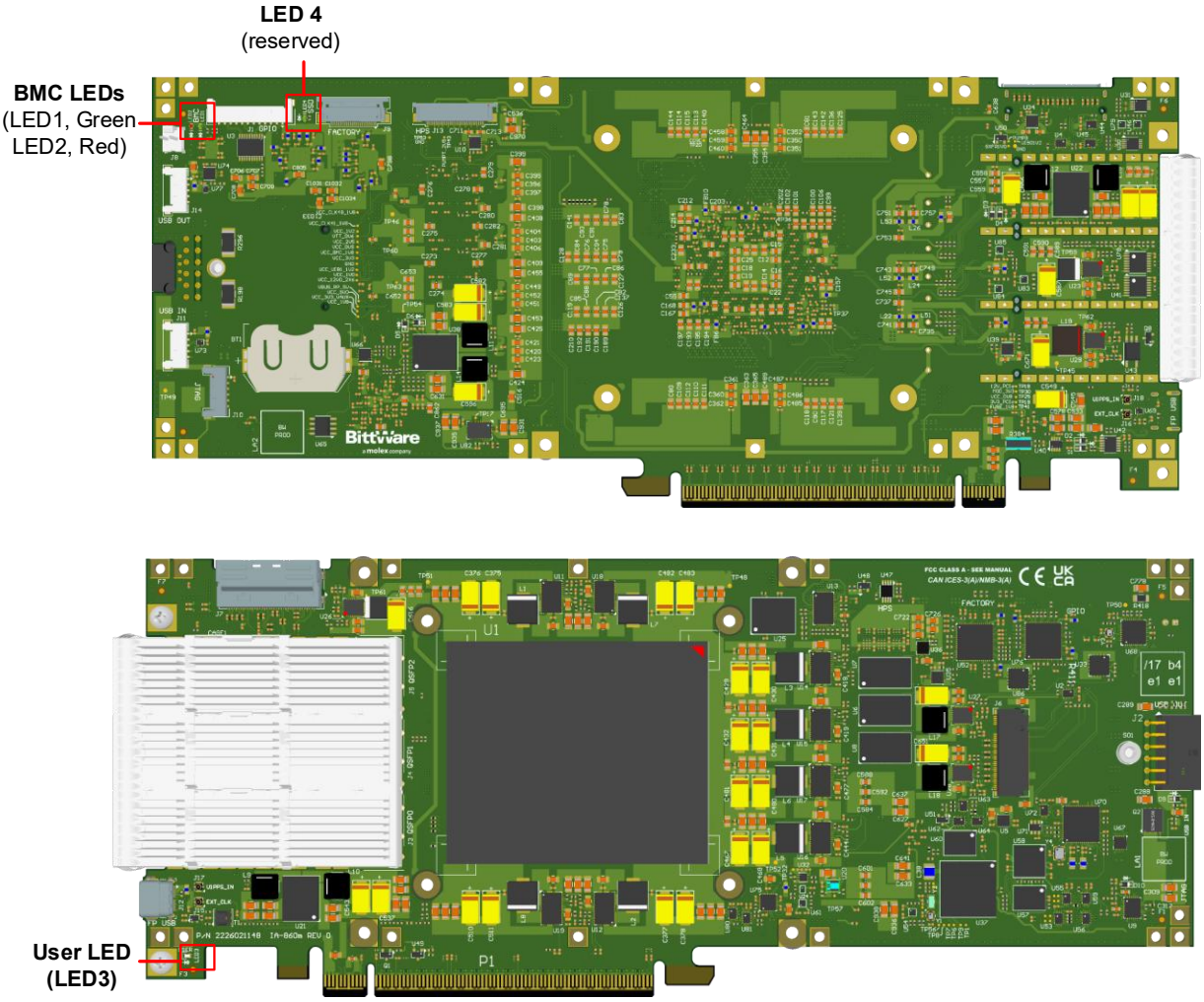
The Agilex FPGA on the IA-860m employs SmartVID to compensate for process variation by using voltage adaptation. The use of SmartVID is mandatory and requires certain entries in the Quartus Settings File (QSF). Please refer to the IA-860m *FPGA Developer Reference Guide* for details.

Altera Agilex Power Management User Guide:
https://www.intel.com/content/dam/www/programmable/us/en/pdfs/literature/hb/agilex/ug-ag-pwr.pdf

9.5 LEDs

The IA-860m has four LEDs. The BMC uses LED1 and LED2 for reporting its status, the user FPGA can drive LED3.

Figure 13: LED locations



9.5.1 BMC Status LEDs

The two LEDs in the following table are either red or green and define the BMC behavior.

Table 29: BMC Status LEDs

LED Behavior Description	LED1 (GREEN)	LED2 (RED)
Power Start- at initial power-on	Blink @2Hz	Blink @2Hz
Power Off Ready- Board is powered off via the BMC	OFF	Blink @2Hz
Power On- Board is powered on and ready	Blink @2Hz	OFF
Power Off Fault- Fault on card and the BMC has powered down board supplies	OFF	Blink @2Hz
Power Off User- User manually powered down board supplies	ON	Blink @2Hz
Bootloader- User placed board into bootloader mode	OFF	Blink @0.5Hz
JTAG Mode- BMC is set up for JTAG programming	Blink @2Hz	Blink @2Hz
Factory Reset - Clears user FPGA and clock loads	Flash 2x	Flash 2x

9.5.2 FPGA User LEDs

The user has access to two LEDs driven directly from the FPGA. Table 30 lists the signal names for these User LEDs. Figure 13 shows their locations.

Table 30: FPGA User LEDs

LED	Signal	FPGA Pin	Color	Behavior
LED3	FPGA_LED_G FPGA_LED_R	E25 D26	Green Red	Active Low Active Low

9.6 Jumpers

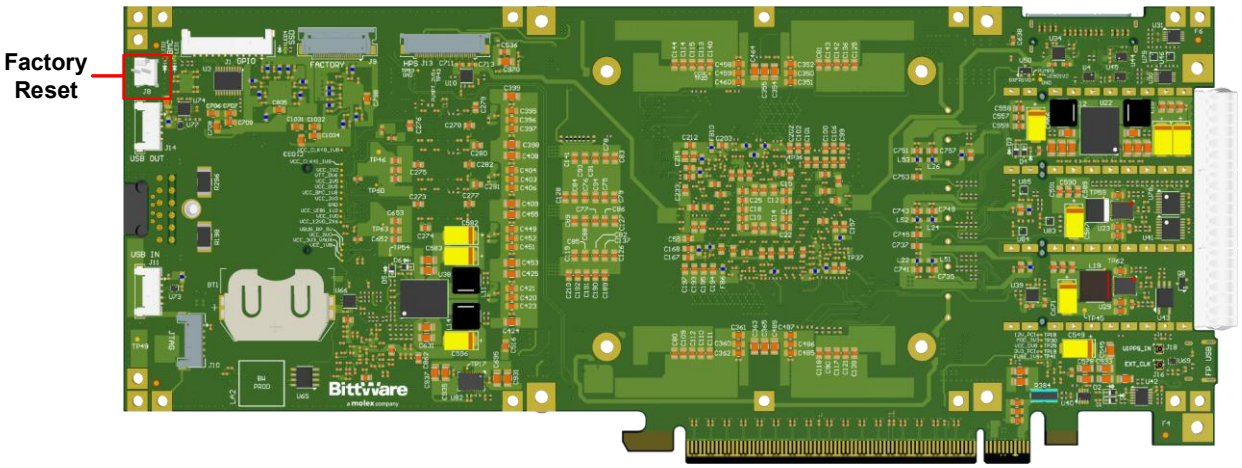
Jumpers on the IA-860m are for factory use only.

9.7 Factory Reset

To set the board set back to its factory default,

1. Short the two J8 holes together using a jumper or equivalent.
2. Power cycle the card.
3. Wait for the BMC to come up (should show Factory Reset LED pattern).
4. Remove the short from J8.

Figure 14: IA-860m Factory Reset



10 USB

The IA-860m features multiple USB devices which are all accessible (through a USB hub) from the rear panel connector J11, connected to a BittWare cable, or from the USB C connector (J12) on the front panel. See Accessories for more information on cables and accessories for the IA-860m.

Note: For more information on deployment solutions in a BittWare TeraBox FPGA server, visit the TeraBox section on the BittWare website or contact your BittWare Sales representative for more information.

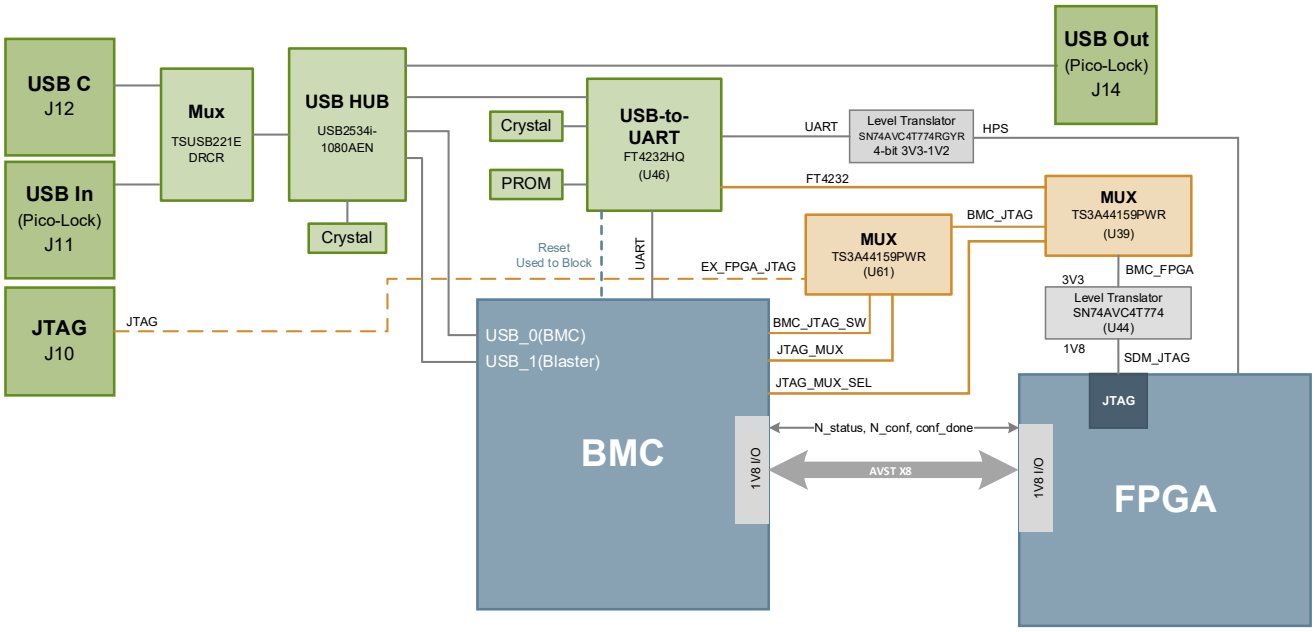
The USB connector gives access to the following USB devices:

1. Breakout header for external USB-Blaster pod access for JTAG access to the FPGA
2. BMC for access to control and status port (see BMC)
3. An FPGA user-controller UART

10.1 Board Features Accessible via USB

The USB ports provide access to the BMC, USB UART, and USB Blaster (via external header). The USB connector is routed to the upstream port, a USB 2.0 hub, which in turn connects to the downstream devices. One downstream device is the BMC, which is a USB 2.0 compatible device. Secondly, an FTDI USB to UART converter provides a connection to HPS UART and BMC UART.

Figure 15: USB Interface



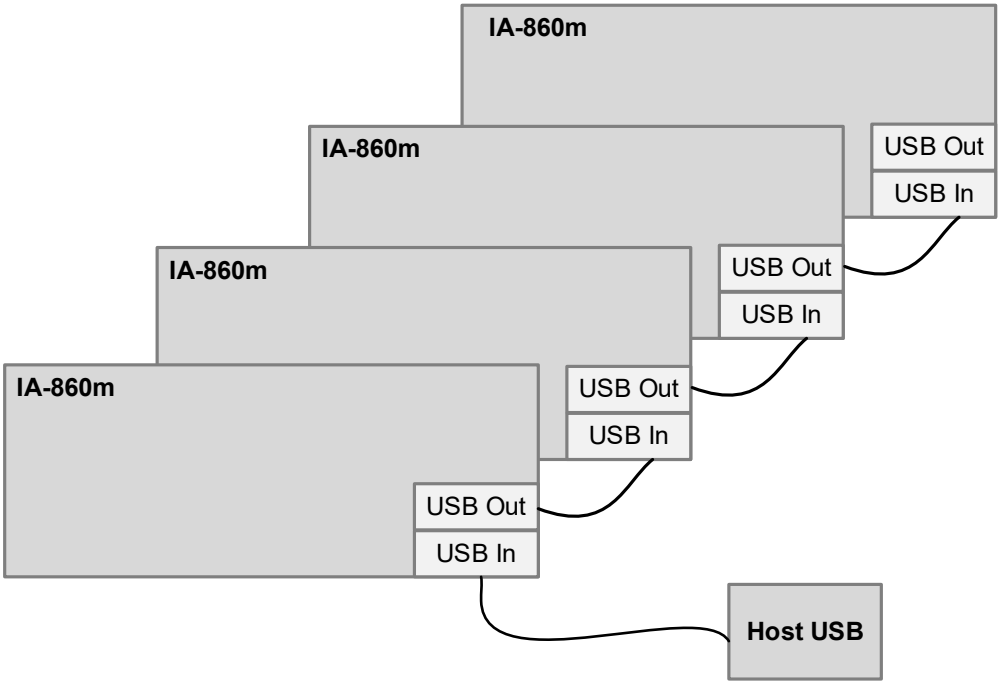
10.2 USB Connectors

The front panel features a USB C header (J12 – see Figure 3: Top View) below the QSFP cages. Two Pico-Lock connectors (Molex 504050-0591) are on the rear panel for daisy chaining.

The front panel USB is multiplexed with the USB IN connector (J11) on the rear. A USB OUT connector (J14) on the rear of the board allows USB traffic to be routed out of the USB hub on the IA-860m and connect to another IA-860m downstream. A daisy chain of up to four IA-860m cards can be formed as illustrated below.

Note: The Pico-Lock connectors are not part of the USB standard. See Accessories for cable options for the IA-860m.

Figure 16: USB Daisy Chain



10.3 JTAG Utilities

The breakout cable (see Accessories) and external header (J10) allows for external Intel/Altera blaster pod access(hardware rev0 to rev 3) that provides access to the FPGA JTAG chain and allows you to reprogram the FPGA using the Quartus Programmer Tool. The user JTAG chain consists of the USB-to-JTAG device, through the BMC and to the FPGA.

Note, the integrated USB blaster 3 hardware is not supported with all revisions of the IA-860m. The IA-860m rev 4 hardware enables the embedded FTDI USB blaster circuit at factory programming which can remove the need for the external breakout and external USB blaster II pod use for JTAG debug.

Note: On rev4 IA-860m hardware the physical J10 Pico-Lock header that was previously used to enable use of an external USB Blaster II pod is now deprecated and considered a reserved header on rev4 hardware and later.

Intel/Altera provides several other debug tools which use the JTAG chain:

- Signal Tap II Logic Analyzer
- Transceiver Toolkit
- External Memory Interface Toolkit
- In-System Sources and Probes Editor

Refer to Altera's documentation for details on using these tools.

Please note that the embedded FTDI based USB Blaster 3 feature, enabled in IA-860m rev4 hardware, is officially supported as of Quartus Prime Pro 25.1 release. If required BittWare can provide a path for Quartus 24.3 or 24.3.1 versions but earlier versions of Quartus are not supported. Please also note that Quartus support is currently limited, by validation, to Linux only.

Note: for installation on Linux, refer to "Intel/Altera FPGA Download Cable (formerly USB-Blaster) Driver for Linux" on the Altera website.

The Quartus installation folder includes the USB-Blaster II drivers.

10.3.1 JTAG Connector

Connector J10 is a Pico-Lock connector that provides external access to the FPGA JTAG chain using a BittWare breakout cable. See Accessories for cable options for the IA-860m. Note that this J10 header is only recommended for use on PCB hardware revisions rev 0 to rev3. **For rev4 hardware please make use of the integrated USB Blaster 3.**

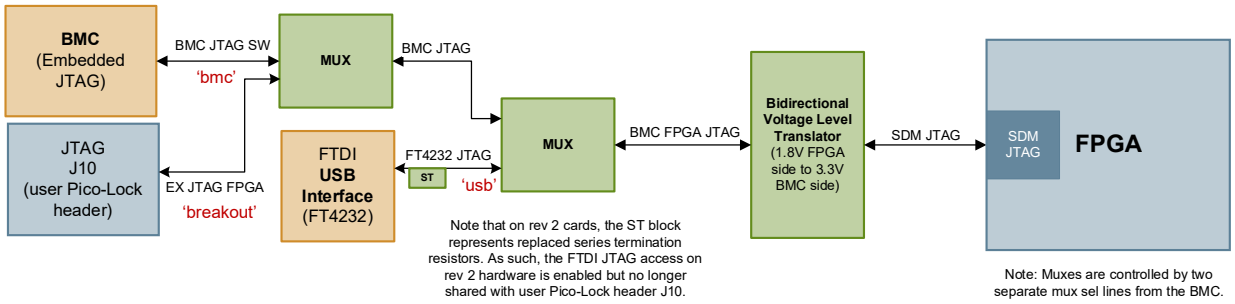
Table 31: JTAG Connector Pinout

Pin	Signal
1	VCC_3V3
2	FT4232_TCk
3	FT4232_TDI
4	FT4232_TDO

5	FT4232_TMS
6	GND

10.3.2 JTAG Chain

Figure 17 JTAG Chain



Note that for rev 1,2,and 3 IA-860m units JTAG debug access is only supported via external Intel/Altera USB Blaster II pod hardware via the J10 Pico-Lock JTAG header when shipped from the factory. There is an option for manual enablement of a new FTDI based USB embedded blaster feature but this is not a factory tested feature at those hardware revisions. Please contact BittWare support for further details.

For rev 4 IA-860m units, the embedded USB Blaster 3 FTDI option is enabled through pre-programming at the factory side. This provides an embedded USB blaster device that is accessed via the USB input headers on the IA-860m and removes the need for an external Intel/Altera Blaster II pod via the J10 header.

Note in the above diagram, the 'bmc', 'breakout', 'usb' denote the JTAG mux settings.

JTAG chain mux control

The above diagram illustrates the different JTAG chains that exist on IA-860m hardware. To allow JTAG chain access the mux control needs set correctly based on the revision of hardware.

- **IA-860m rev 0,1** : 'usb'
  - (default where FTDI path is shared with J10 Pico-Lock header).
  - For these revisions of hardware, the embedded USB Blaster 3 is not enabled and so a physical USB Blaster II pod needs to be connected via the J10 Pico-Lock header and adapter cable set.
- **IA-860m rev 2,3 :** 'breakout
  - (default is breakout to the J10 Pico-Lock header)
  - For these revisions of hardware, the embedded USB Blaster 3 is not enabled and so a physical USB Blaster II pod needs to be connected via the J10 Pico-Lock header and adapter cable set.
- **IA-860m rev 4 : '**usb'
  - (default is usb,for FTDI access)
  - For rev4 hardware, these cards have the FTDI embedded USB Blaster 3 circuit enabled at the factory programming time and this path is now the recommended JTAG debug path. The external J10 Pico-Lock header that was intended for external USB Blaster II pod support is now considered deprecated and should be considered a reserver header on rev4 and later IA-860m hardware.

The JTAG mux can be set via new effecter as required:

```
bw_bmc_pldm_effecter -i USB set --name "JTAG Mux" -v usb
```

or

```
bw_bmc_pldm_effecter -i USB set --name "JTAG Mux" -v breakout
```

Note the JTAG mux setting of bmc is considered a reserved setting.

10.3.3 System Device Permission Files

The FTDI USB Blaster option requires some additional udev rule files to be created or modified. It is expected that over time Altera will work this into their standard instructions. For now, the following is documented here.

Rule File to Allow Access to Blaster on Linux Systems

To allow access to the USB blaster device on Linux systems, suitable udev rule files need to be in place. The existing Intel/Altera USB blaster documentation includes the details required for existing Blaster generation 1 and 2 pods in the /etc/udev/rules.d/51-usbblaster.rules named file. BittWare supplies a reference udev fileset that extends these and adds some additional BittWare-specific modification to handle the shared nature of the quad FTDI device as it is also used for UART features. :

Note: The BittWare developer site contains these files for use and for reference. The section here is to document what was added or defined in these files. Recommendation is to simply copy the supplied udev rule files into /etc/udev/rules.d/ and the supplied script into /usr/local/bin/. Ensure the script has executable permissions set also once copied into the /usr/local/bin/ location.

Three files are included in the udev reference set:

- 51-usbblaster.rules
  Copy this file into /etc/udev/rules.d/
- 99-bw-ftdi.rules
  Copy this file into /etc/udev/rules.d/
- unbind-ftdi.sh
  Copy this file into /usr/local/bin/

```
#/etc/udev/rules.d/51-usbblaster.rules

#USB-Blaster

ACTION=="add", SUBSYSTEM=="usb", ENV{DEVTYPE}=="usb_device",
ATTR{idVendor}=="09fb", ATTR{idProduct}=="6001", MODE="0666"

ACTION=="add", SUBSYSTEM=="usb", ENV{DEVTYPE}=="usb_device",
ATTR{idVendor}=="09fb", ATTR{idProduct}=="6002", MODE="0666"

ACTION=="add", SUBSYSTEM=="usb", ENV{DEVTYPE}=="usb_device",
ATTR{idVendor}=="09fb", ATTR{idProduct}=="6003", MODE="0666"

#USB-Blaster II
```

```
ACTION=="add", SUBSYSTEM=="usb", ENV{DEVTYPE}=="usb_device",
ATTR{idVendor}=="09fb", ATTR{idProduct}=="6010", MODE="0666"

ACTION=="add", SUBSYSTEM=="usb", ENV{DEVTYPE}=="usb_device",
ATTR{idVendor}=="09fb", ATTR{idProduct}=="6810", MODE="0666"

# USB-Blaster III

ACTION=="add", SUBSYSTEM=="usb", ENV{DEVTYPE}=="usb_device",
ATTR{idVendor}=="09fb", ATTR{idProduct}=="6024", MODE="0666"
```

Rule File for FTDI Specifics

It is also required to create an additional rule file for the FTDI specifics.In this case, we are using it to add some additional helper SYMLINKS to better map through the FTDI ports used for both BMC and HPS UART comms. Create and add the file contents for /etc/udev/rules.d/ 99-bw-ftdi.rules

```
#/etc/udev/rules.d/99-bw-ftdi.rules

#This is a secondary udev rule file for handling the shared port nature of
the FTDI4232H device

#that is used for both the integrated USB blaster III function and also a
number of serial comms

#interfaces. It also creates symlinks for these serial ports for both BMC
shell and HPS UART paths.

# First bind the FT4232H with custom blaster IDs to the standard ftdi_sio
driver (VID:09fb PID:6024)

ACTION=="add", ATTR{idVendor}=="09fb", ATTR{idProduct}=="6024",
RUN+="/sbin/modprobe ftdi_sio", RUN+="/bin/sh -c 'echo 09fb 6024 >
/sys/bus/usb-serial/drivers/ftdi_sio/new_id'"

# BittWare use port 0 (ABUS) for the JTAG function on single FPGA products
and port 1 (BBUS) on some dual FPGA products. This file relates to the port
0 only case.

# Unbind interface 0 to prevent /dev/ttyUSB0 ftdi_sio use and binding (ABUS
FPGA JTAG)

ACTION=="add", SUBSYSTEM=="usb", ATTRS{idVendor}=="09fb",
ATTRS{idProduct}=="6024", ATTR{bInterfaceNumber}=="00",
RUN+="/usr/local/bin/unbind-ftdi.sh %p"

# Create symlinks for BMC and HPS uart interfaces using combination of tty
prefix and board serial number identifier.

# Note that these are symlinks only and the underlying dev port can still
be used i.e. /dev/ttyUSB1 for interface number 01.

ACTION=="add", SUBSYSTEM=="tty", ATTRS{idVendor}=="09fb",
ATTRS{idProduct}=="6024", ENV{ID_USB_INTERFACE_NUM}=="01",
SYMLINK+="ttyBMC-%E{ID_SERIAL_SHORT}"

ACTION=="add", SUBSYSTEM=="tty", ATTRS{idVendor}=="09fb",
ATTRS{idProduct}=="6024", ENV{ID_USB_INTERFACE_NUM}=="03",
SYMLINK+="ttyHPS-%E{ID_SERIAL_SHORT}"
```

Note: Please ensure that the unbind-ftdi.sh script file has executable permissions once copied into the /usr/local/bin/ folder. Recommended permissions as 755 : “sudo chmod 0755 unbind-ftdi.sh”

```
#/usr/local/bin/unbind-ftdi.sh

#!/bin/bash

DEVICE_PATH="$1"

LOGFILE="/var/tmp/devicePath.log"

echo "$(date) DEVICE_PATH=$DEVICE_PATH" > "$LOGFILE"

UNBIND_PATH=$(basename "$DEVICE_PATH")

if [[ -n "$UNBIND_PATH" ]]; then

DRIVER_PATH="/sys/bus/usb/drivers/ftdi_sio/unbind"

if [[ -e "$DRIVER_PATH" ]]; then

echo "$UNBIND_PATH" > "$DRIVER_PATH"

echo "Unbound $UNBIND_PATH at $(date)" >> "$LOGFILE"

else

echo "$(date) Driver path $DRIVER_PATH not found" >> "$LOGFILE"

fi

else

echo "$(date) Could not extract unbind path from $DEVICE_PATH" >>
"$LOGFILE"

fi
```

Note: Once these udev rules files and Quartus patch has been installed the system should be rebooted or immediately applied using command for example “udevadm control --reload-rules && udevadm trigger”.

Debug Information

Note: This section contains some important debug information for a situation we have observed in early support and testing that is being investigated and has been reported to Altera also already.

We have seen an issue where a udev change reclaims and then blocks the Blaster device. If you see an error around being unable to lock the device, please use the USB device path to unbind it manually again to allow access.

Note the example device address below may not match your configuration. The path may be shown in the JTAG tools or dmesg output but the simplest is to make use of the udevadm command i.e.

```
$ udevadm info --name=/dev/ttyUSB0 | grep DEVPATH
```

```
returns
```

```
E: DEVPATH=/devices/pci0000:c0/0000:c0:07.1/0000:cc:00.4/usb1/1-2/1-2.1/1-2.1.4/1-2.1.4:1.0/ttyUSB0/tty/ttyUSB0
```

```
sudo bash -c "echo 1-2.1.4:1.0 > /sys/bus/usb/drivers/ftdi_sio/unbind"
```

```
sudo killall jtagd
```

Then try accessing via jtag tools again. BittWare is investigating further to the cause of this udev behavior.

10.3.4 Controlling FTDI USB Blaster 3 JTAG Speed

The FTDI USB Blaster 3 firmware currently defaults to a 1Mhz speed. JTAG speed can be controlled via parameter settings either in Quartus GUI tools or via jtagconfig console commands (the example below sets speed to 15Mhz for TCK):

```
jtagconfig --setparam 1 JtagClockAutoAdjust 0
```

```
jtagconfig --setparam 1 JtagClock 15M
```

```
jtagconfig --getparam 1 JtagClock
```

11 Power

11.1 Power Specifications

The IA-860m board is designed to support a typical operating power consumption of 300W. The standard Fan/Heatsink COTS solution supports 300 Watts cooling with an ambient inlet temperature up to 35C. Under these conditions the FPGA die temperature will typically be kept below an operating junction temperature of 85C.

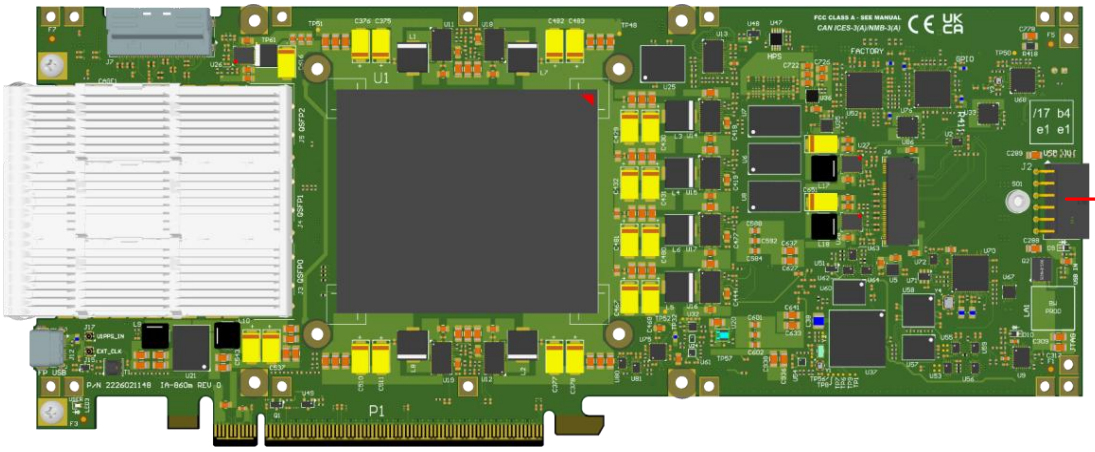
You can read the FPGA fabric temperature via the BMC and estimate the power required by the FPGA using Intel/Altera's EPE tool available on the Intel website.

11.2 Power Requirements

Power requirements for the IA-860m are application-specific. The card power draw might go from low, if the FPGA is unconfigured, to medium when the FPGA is programmed with an FPGA design. FPGA designs with high resource utilization, high toggle rate, and high clock frequency will increase the card power draw, which might approach the card's max power.

11.3 Power Sources

The IA-860m is powered from the host motherboard PCIe slot power supplies and an external PCIe 12V power supply. The card will not power up without the external 12V power supply.



11.3.1 12-Pin Power Connector

The pinout for the 12-pin connector (12V 2x6 Amphenol 10160920-1240100LF) is shown in the following image and table:

Figure 18: 12V_2x6 External Power Connector

Table 32: 12-pin Auxiliary Power Connector Receptacle Side Pinout [8]

Pin	Signal	Pin	Signal	Pin	Signal
1	+12V	7	GND	S1	12V_2X6_CARD_PWR_STABLE
2	+12V	8	GND	S2	12V_2X6_CARD_CBL_PRES_L
3	+12V	9	GND	S3	X12V_2X6_SENSE0
4	+12V	10	GND	S4	X12V_2X6_SENSE1
5	+12V	11	GND		
6	+12V	12	GND		

11.4 Power Monitoring

As noted in the Card Management section, the BMC monitors the power supplies in real time. You can use the SDK's BMC utility to read the values, or you can use MCTP/PLDM, as described in the *BMC Reference Guide for IA-860m*. The BMC Reference Guide also lists the sensors that the BMC is monitoring.

[8] Pinout source: PCIe Specification Revision 1.0

12 Mechanical

12.1 Chassis Requirements

12.1.1 PCI Express

The IA-860m is capable of PCIe Gen5 with 16 lanes. The card requires a x16 PCIe slot for mechanical compatibility. Note that the IA-860m mechanicals are designed against PCIe CEM6.

12.1.2 PCIe Bracket

The card ships with a PCIe faceplate bracket matching the card configuration. The example below shows the dual-slot faceplate for a card configured with three QSFP-DDs.

Figure 19: PCIe Faceplate (Standard Configuration)

12.1.3 Mechanical Configuration

The IA-860m has an extender bracket that converts it from a GPU length card to a full length CEM6 compliant form factor. The following images show the GPU and CEM6 configurations.

Figure 20 Full-Length CEM6 Configuration, side view

Figure 21 GPU-Length Configuration, side view

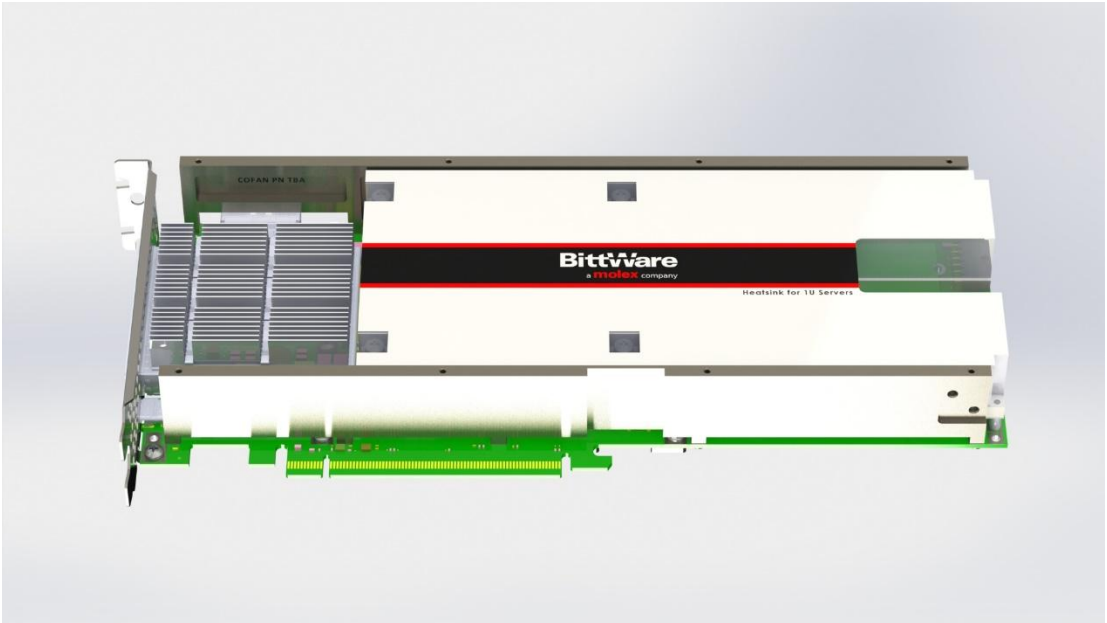
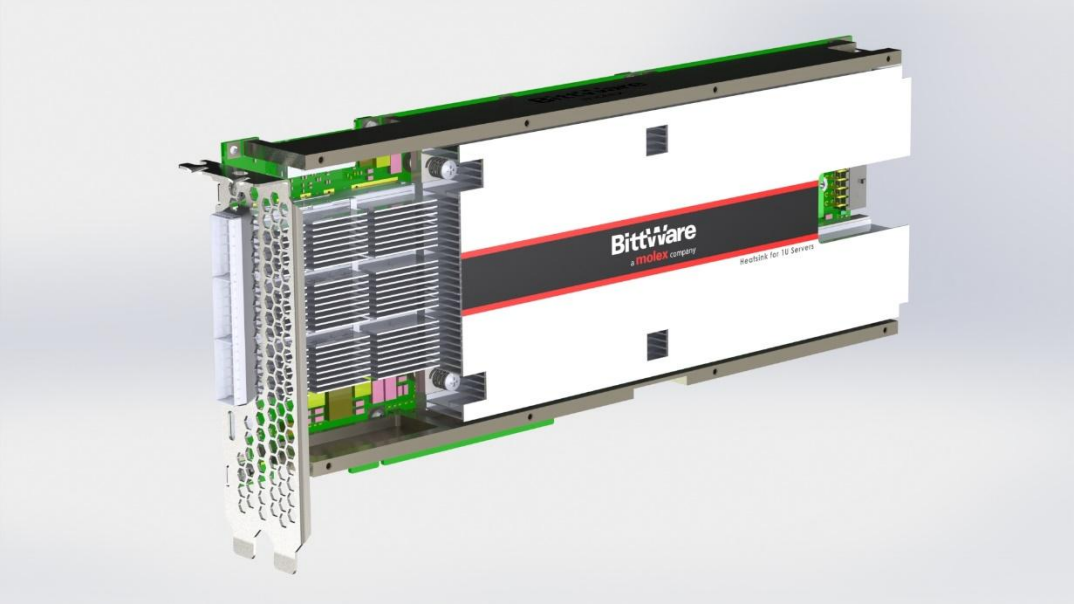


Figure 22 GPU-Length Configuration, angle view



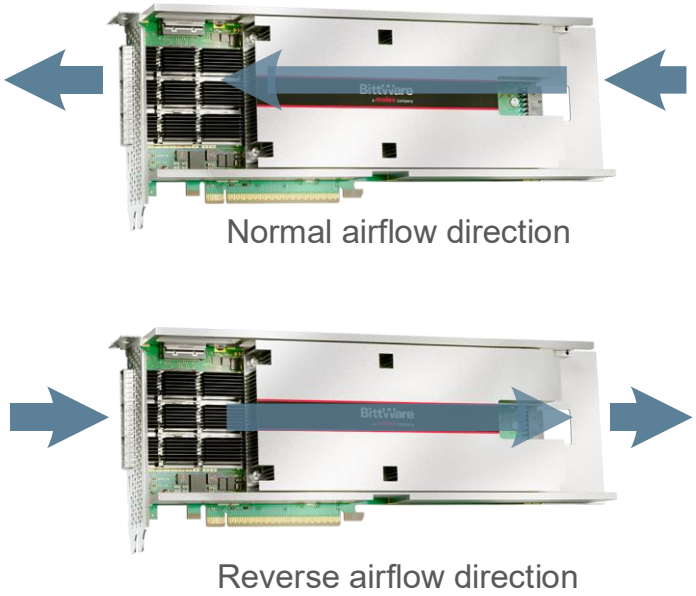
12.2 Air Flow

The IA-860m is fitted with a passive heatsink. Be sure that the installation has sufficient airflow and that the power consumption is limited to keep the card within its operating temperature limits. The BMC monitors the FPGA temperature. Refer to your card's BMC Reference Guide for details about sensor limits.

Note: As of this publishing date, we do not yet have wind tunnel data for this card. We will publish characterization data for the heatsink solution in a future update.

Be sure to provide adequate cooling for the IA-860m using either of the two methods shown below.

Figure 23: IA-860m Airflow Methods



BittWare cards can operate at high temperatures depending on the power draw of the application in the FPGA. The Board Management Controller will power down the card to prevent damage if components reach above a certain temperature threshold. Monitor the temperature of your card to ensure it is running consistently within the supported temperature range. If the card powers down suddenly, this is often an indication that the BMC powered down due to overheating. BittWare recommends altering the card cooling to address this. The factors that affect the thermal performance of a card are:

- Power consumption of the card/FPGA
- Ambient temperature
- Airflow through the heatsink

Power consumption and ambient temperature are typically static. Therefore, if a card is overheating, BittWare recommends ensuring the chassis fans are oriented to blow through the card heatsink and altering fan speed to increase airflow through the heatsink.

Note: BittWare has seen issues cooling cards in desktop and workstation environments. This is due to the typical placement of fans relative to the card heatsink. If a desktop chassis must be used, additional fans will likely be required to adequately cool the card. This can be additional chassis fans positioned to blow through the heatsink or standalone desk fans oriented to move air over the FPGA.

See BittWare's Lab and Open Bench Environment Card Cooling white paper for a how-to on BittWare's solution for cooling cards in an open-bench lab environment.

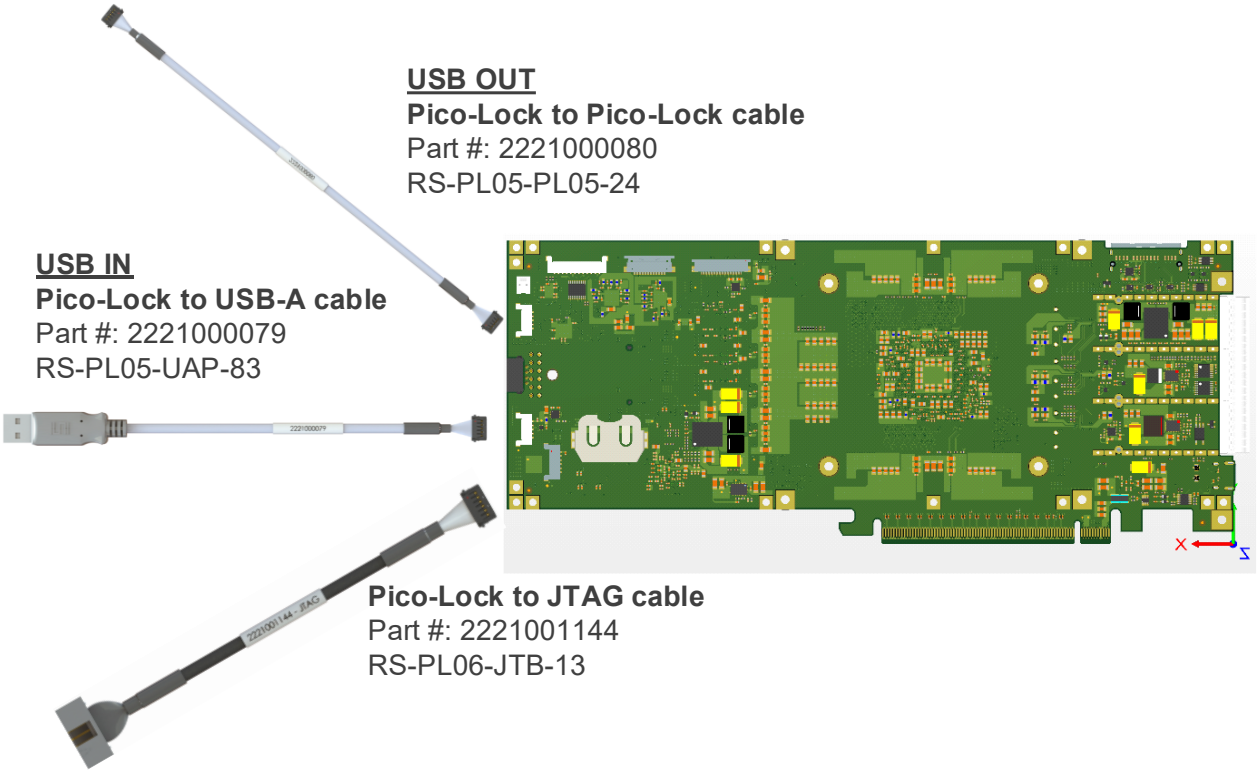
12.3 Card Dimensions

- Standard height: 111.15 (4.376)
- Full length: 312.00 (12.283in)
- Dual slot

13 Accessories

Three accessory cables are available for the IA-860m. The cables are purchased separately and are **not** included with the IA-860m.

Figure 24: Cable options for IA-860m



13.1 Pico-Lock to USB-A Cable

For **deployment**, BittWare recommends using a BittWare **Pico-Lock to USB A cable** which connects directly between the IA-860m and the host USB. The deployment cable only connects the USB path to the BittWare hardware. It does not allow access to the USB Blaster pod header. It allows access to the USB devices such as on-card BMC and FPGA flash programming paths via a host USB connection.

- **Part number**: 2221000079
- **Uses**:
  - Deployment
  - Accessing the BMC (FPGA programming, card health monitoring) ***This can also be done via PCIe***
  - Accessing the USB UART (FPGA UART and HPS UART)
- **Connects to**: J11 on the IA-860m

13.2 Pico-Lock to JTAG Cable

For **development**, you can purchase a custom BittWare Pico-Lock to JTAG cable which connects directly between the IA-860m and an Intel/Altera Blaster pod (*not included*).

- **Part number**: 2221001144
- **Uses**:
  - Development and debug
  - Using an Intel/Altera Blaster pod[9] via the JTAG Interface
  - Programming the FPGA using the Quartus Programmer Tool
- **Connects to**: J14 on the IA-860m

[9] The Intel Blaster is not included. For more information on Intel's FPGA download cables, see https://www.intel.com/content/www/us/en/products/details/fpga/development-kits/cables-adapters.html