```vhdl
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_ARITH.ALL;
use IEEE.STD_LOGIC_UNSIGNED.ALL;

entity Microprocessador is
   Port (
      Reset : in STD_LOGIC;
      CLK : in  STD_LOGIC
   );
end Microprocessador;

architecture Estructural of Microprocessador is

   constant CONST31 : std_logic_vector(4 downto 0) := "01111";
   constant CONST0 : std_logic_vector(4 downto 0) := "00000";
   signal l_sor1, l_sor2,e_reg,l_mem,e_mem,e_mar,l_mdr,e_mdr,e_ir,l_pc,e_pc,pc_sup,inc_pc,l_desp1,l_desp2,l_extsign,l_acc,e_acc,Tancar,z,c : STD_LOGIC;
   signal mux_dest : STD_LOGIC_VECTOR(1 DOWNTO 0);
   signal op_alu : STD_LOGIC_VECTOR(2 downto 0);
   signal rdest : STD_LOGIC_VECTOR (4 downto 0);
   signal Instruccio, DB3 , DB2, DB1 , Alu_op1, Alu_op2, Sortida_Extensio,Adresa_RAM, Resultat_ALU , Dades_RAM , Dades_Out_Ram, Dades_Out_MDR_Ram : STD_LOGIC_VECTOR( 31 downto 0);

begin

   -- Unitat de Control --
  uc: UnitatDeControl port map ( Reset,CLK ,Instruccio(31 downto 26),Instruccio (5 downto 0),z ,c ,l_sor1,l_sor2,e_reg,mux_dest,l_mem,e_mem,e_mar,l_mdr,e_mdr,e_ir,l_pc,e_pc, pc_sup,inc_pc,l_desp1,l_desp2,l_extsign,l_acc,e_acc,Tancar,op_alu);

  -- Registre d'Instruccio --
  ir: Latch32Bits port map ( CLK ,e_ir,RESET,DB3 ,Instruccio);

  mx: Mux4a1_5Bits port map ( mux_dest ,Instruccio(20 downto 16),Instruccio(15 downto 11) ,CONST31 ,CONST0, rdest );

  -- Banc de Registres --
  breg: BancRegistres port map ( Reset ,CLK ,e_reg  ,rdest ,DB3 ,l_sor1 ,Instruccio(25 downto 21) ,l_sor2 ,Instruccio(20 downto 16) ,DB1, DB2);

  pcs: PCSUP port map ( pc_sup ,DB1, Alu_op1 );

  pc: ComptadorPrograma port map ( Reset,CLK , inc_pc,l_pc , e_pc , DB3 ,DB1);

  d1: Desp25a0 port map ( l_desp2 , Instruccio(25 downto 0) , DB2 );

  d2: DespExtSign15a0 port map ( l_desp1 ,Sortida_Extensio ,DB2);

  exts: ExtensioDeSigne port map ( l_extsign ,Instruccio (15 downto 0) , DB2, Sortida_Extensio );

  alu: ALU32 port map ( op_alu , Alu_op1 ,DB2 , Resultat_ALU, z,c);

  acc: Acumulador port map (CLK ,l_acc , e_acc ,Resultat_ALU ,DB3);

  ma: RegistreMAR port map ( e_mar,DB1 , Adresa_RAM);

  mr: RAMSin port map ( CLK,e_mem ,l_mem ,Adresa_RAM(7 downto 2) ,Dades_RAM , Dades_Out_Ram);

  mdr: RegistreMDR port map ( CLK ,Reset ,e_mdr ,l_mdr ,l_mem ,DB2 ,Dades_Ram, Dades_Out_Ram ,DB3);

  enl:  EnllacBus port map ( Tancar , DB3 , DB1);

end Estructural;
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