Finite State Machine CheatSheet

```
module fsm_template(
    input logic reset_n, x_in, clk,
    output logic mealy, moore
    );
    reg [1:0] NS, PS;
    parameter [1:0] st_A=2b'00, st_B=2b'01, st_C=2b'10;

    always @ (negedge reset_n, posedge clk)
       if (reset_n == 0) PS <= st_A;
       else              PS <= NS;

    always @ (x_in, PS)
    begin
       mealy = 0; moore = 0;
       case(PS)

       st_A:
          begin
             moore = 1;
             if (x_in == 1)
             begin
                mealy = 0;
                NS = st_A;
             end
             else
             begin
                mealy = 1;
                NS = st_B;
             end
          end

       st_B:
          begin
             moore = 0;
             mealy = 1;
             NS = st_C;
          end

       st_C:
          begin
              moore = 1;
              if (x_in == 1)
              begin
                 mealy = 1;
                 NS = st_B;
              end
              else
              begin
                 mealy = 0;
                 NS = st_A;
              end
          end

       default: NS = st_A;
       endcase
    end  // always

endmodule
```

user-defined type for states

state register definition

assign all outputs to avoid latches

Moore outputs are function of state only

Mealy outputs are function of state and external input

illegal state recovery