FRVFM CheatSheets

## **Finite State Machine CheatSheet**

```
module fsm_template(
    input logic reset_n, x_in, clk,
                                                 user-defined type
    output logic mealy, moore
                                                    for states
    );
    reg [1:0] NS, PS;
    parameter [1:0] st A=2b'00, st B=2b'01, st C=2b'10;
    always @ (negedge reset_n, posedge clk)
       if (reset_n == 0) PS <= st A;
                                                       state register definition
                            PS <= NS;
    always @ (x_in, PS)
                                       assign all outputs
    begin
                                       to avoid latches
       mealy = 0; moore = 0;
       case(PS)
        st A:
                                         Moore outputs are
           begin
              moore = 1;
                                         function of state only
              if (x_in == 1)
              begin
                 mealy = 0;
                                              Mealy outputs are
                  NS = st_A;
                                              function of state
              end
                                              and external input
              else
                 mealy = 1;
                  NS = st_B;
                                                             FSM
              end
                                             reset n
                                                                        mealy
           end
                                                x_in
                                                                        moore
                                                 clk
        st B:
           begin
              moore = 0;
              mealy = 1;
                                                x_{in} mealy
              NS = st_C;
                                                             \overline{x_{in}} /mealy
           end
                                                                         st_B
                                                     st_A
        st_C:
                                           reset_n
           begin
                                                     moore
                                                                        moore
               moore = 1;
                if (x_in == 1)
                begin
                                                           x_in/mealy
                  mealy = 1;
                   NS = st B;
                end
                else
                                                              st_C
                                             \overline{x_{in}} / mealy
                begin
                                                                           −/mealy
                   mealy = 0;
                                                             moore
                   NS = st A;
                end
           end
        default: NS = st A;
                                            illegal state recovery
        endcase
    end // always
endmodule
```