1. Description

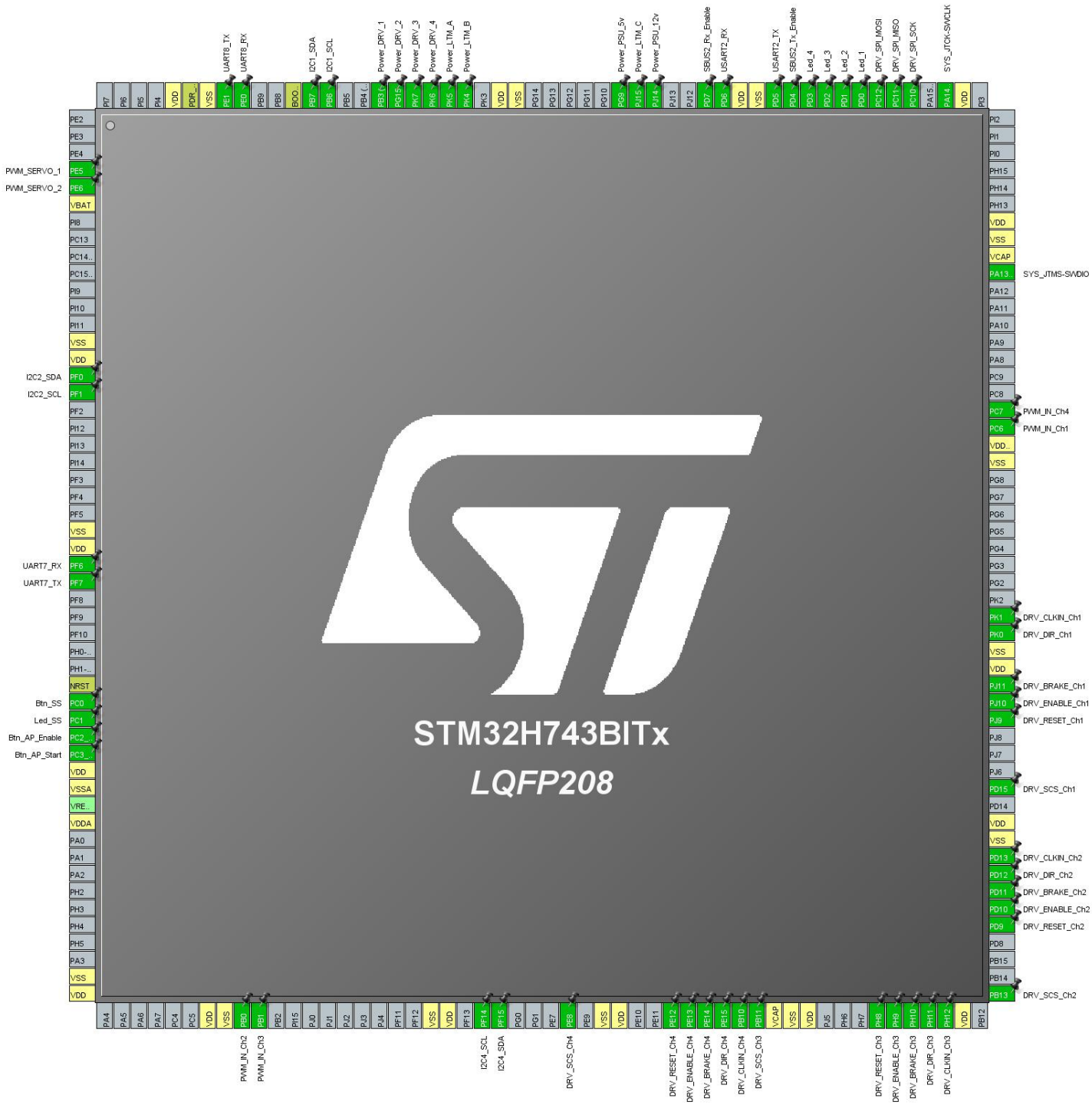
1.1. Project

Project Name	MiniCar_v2
Board Name	custom
Generated with:	STM32CubeMX 5.1.0
Date	07/23/2021

1.2. MCU

MCU Series	STM32H7
MCU Line	STM32H743/753
MCU name	STM32H743BITx
MCU Package	LQFP208
MCU Pin number	208

2. Pinout Configuration



3. Pins Configuration

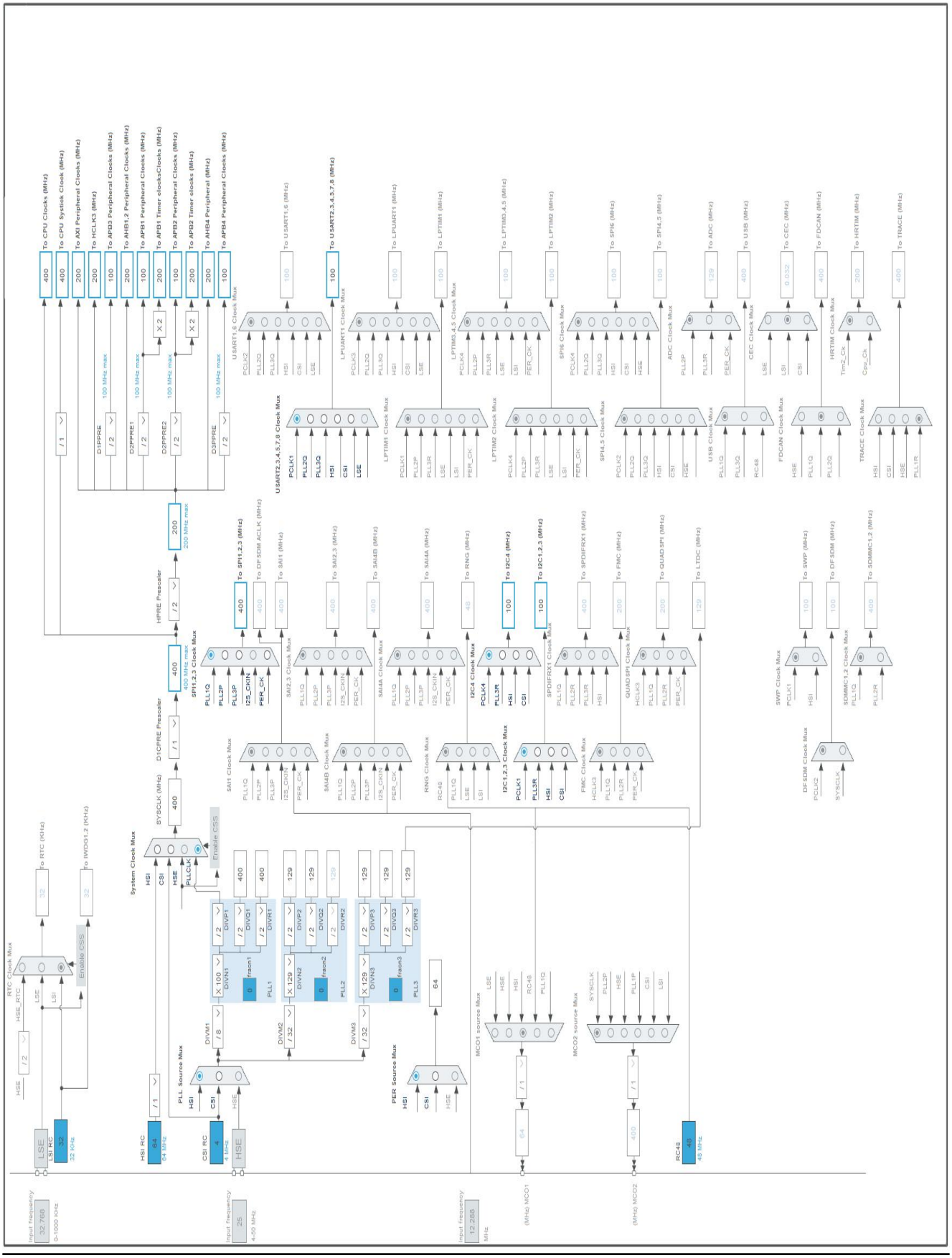
Pin Number LQFP208	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
4	PE5	I/O	TIM15_CH1	PWM_SERVO_1
5	PE6	I/O	TIM15_CH2	PWM_SERVO_2
6	VBAT	Power		
14	VSS	Power		
15	VDD	Power		
16	PF0	I/O	I2C2_SDA	
17	PF1	I/O	I2C2_SCL	
25	VSS	Power		
26	VDD	Power		
27	PF6	I/O	UART7_RX	
28	PF7	I/O	UART7_TX	
34	NRST	Reset		
35	PC0 *	I/O	GPIO_Input	Btn_SS
36	PC1 *	I/O	GPIO_Output	Led_SS
37	PC2_C *	I/O	GPIO_Input	Btn_AP_Enable
38	PC3_C *	I/O	GPIO_Input	Btn_AP_Start
39	VDD	Power		
40	VSSA	Power		
42	VDDA	Power		
51	VSS	Power		
52	VDD	Power		
59	VDD	Power		
60	VSS	Power		
61	PB0	I/O	TIM3_CH3	PWM_IN_Ch2
62	PB1	I/O	TIM3_CH4	PWM_IN_Ch3
72	VSS	Power		
73	VDD	Power		
75	PF14	I/O	I2C4_SCL	
76	PF15	I/O	I2C4_SDA	
80	PE8 *	I/O	GPIO_Output	DRV_SCS_Ch4
82	VSS	Power		
83	VDD	Power		
86	PE12 *	I/O	GPIO_Output	DRV_RESET_Ch4
87	PE13 *	I/O	GPIO_Output	DRV_ENABLE_Ch4
88	PE14 *	I/O	GPIO_Output	DRV_BRAKE_Ch4
89	PE15 *	I/O	GPIO_Output	DRV_DIR_Ch4

Pin Number LQFP208	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
90	PB10	I/O	TIM2_CH3	DRV_CLKIN_Ch4
91	PB11 *	I/O	GPIO_Output	DRV_SCS_Ch3
92	VCAP	Power		
93	VSS	Power		
94	VDD	Power		
98	PH8 *	I/O	GPIO_Output	DRV_RESET_Ch3
99	PH9 *	I/O	GPIO_Output	DRV_ENABLE_Ch3
100	PH10 *	I/O	GPIO_Output	DRV_BRAKE_Ch3
101	PH11 *	I/O	GPIO_Output	DRV_DIR_Ch3
102	PH12	I/O	TIM5_CH3	DRV_CLKIN_Ch3
103	VDD	Power		
105	PB13 *	I/O	GPIO_Output	DRV_SCS_Ch2
109	PD9 *	I/O	GPIO_Output	DRV_RESET_Ch2
110	PD10 *	I/O	GPIO_Output	DRV_ENABLE_Ch2
111	PD11 *	I/O	GPIO_Output	DRV_BRAKE_Ch2
112	PD12 *	I/O	GPIO_Output	DRV_DIR_Ch2
113	PD13	I/O	TIM4_CH2	DRV_CLKIN_Ch2
114	VSS	Power		
115	VDD	Power		
117	PD15 *	I/O	GPIO_Output	DRV_SCS_Ch1
121	PJ9 *	I/O	GPIO_Output	DRV_RESET_Ch1
122	PJ10 *	I/O	GPIO_Output	DRV_ENABLE_Ch1
123	PJ11 *	I/O	GPIO_Output	DRV_BRAKE_Ch1
124	VDD	Power		
125	VSS	Power		
126	PK0 *	I/O	GPIO_Output	DRV_DIR_Ch1
127	PK1	I/O	TIM1_CH1	DRV_CLKIN_Ch1
136	VSS	Power		
137	VDD33_USB	Power		
138	PC6	I/O	TIM3_CH1	PWM_IN_Ch1
139	PC7	I/O	TIM8_CH2	PWM_IN_Ch4
147	PA13 (JTMS/SWDIO)	I/O	SYS_JTMS-SWDIO	
148	VCAP	Power		
149	VSS	Power		
150	VDD	Power		
158	VDD	Power		
159	PA14 (JTCK/SWCLK)	I/O	SYS_JTCK-SWCLK	
161	PC10	I/O	SPI3_SCK	DRV_SPI_SCK
162	PC11	I/O	SPI3_MISO	DRV_SPI_MISO

Pin Number LQFP208	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
163	PC12	I/O	SPI3_MOSI	DRV_SPI_MOSI
164	PD0 *	I/O	GPIO_Output	Led_1
165	PD1 *	I/O	GPIO_Output	Led_2
166	PD2 *	I/O	GPIO_Output	Led_3
167	PD3 *	I/O	GPIO_Output	Led_4
168	PD4 *	I/O	GPIO_Output	SBUS2_Tx_Enable
169	PD5	I/O	USART2_TX	
170	VSS	Power		
171	VDD	Power		
172	PD6	I/O	USART2_RX	
173	PD7 *	I/O	GPIO_Output	SBUS2_Rx_Enable
176	PJ14 *	I/O	GPIO_Output	Power_PSU_12v
177	PJ15 *	I/O	GPIO_Output	Power_LTM_C
178	PG9 *	I/O	GPIO_Output	Power_PSU_5v
184	VSS	Power		
185	VDD	Power		
187	PK4 *	I/O	GPIO_Output	Power_LTM_B
188	PK5 *	I/O	GPIO_Output	Power_LTM_A
189	PK6 *	I/O	GPIO_Output	Power_DRV_4
190	PK7 *	I/O	GPIO_Output	Power_DRV_3
191	PG15 *	I/O	GPIO_Output	Power_DRV_2
192	PB3 (JTDO/TRACESWO) *	I/O	GPIO_Output	Power_DRV_1
195	PB6	I/O	I2C1_SCL	
196	PB7	I/O	I2C1_SDA	
197	BOOT0	Boot		
200	PE0	I/O	UART8_RX	
201	PE1	I/O	UART8_TX	
202	VSS	Power		
203	PDR_ON	Reset		
204	VDD	Power		

* The pin is affected with an I/O function

4. Clock Tree Configuration



5. Software Project

5.1. Project Settings

Name	Value
Project Name	MiniCar_v2.0
Project Folder	D:\STM\MiniCar_2\MiniCar_v2.0
Toolchain / IDE	MDK-ARM V5
Firmware Package Name and Version	STM32Cube FW_H7 V1.3.2

5.2. Code Generation Settings

Name	Value
STM32Cube Firmware Library Package	Copy all used libraries into the project folder
Generate peripheral initialization as a pair of '.c/.h' files	No
Backup previously generated files when re-generating	No
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No

6. Power Consumption Calculator report

6.1. Microcontroller Selection

Series	STM32H7
Line	STM32H743/753
MCU	STM32H743BITx
Datasheet	030538_Rev1

6.2. Parameter Selection

Temperature	25
Vdd	3.0

7. IPs and Middleware Configuration

7.1. CORTEX_M7

7.1.1. Parameter Settings:

Cortex Interface Settings:

CPU ICache	Disabled
CPU DCache	Disabled

Cortex Memory Protection Unit Control Settings:

MPU Control Mode	MPU NOT USED

7.2. I2C1

I2C: I2C

7.2.1. Parameter Settings:

Timing configuration:

I2C Speed Mode	Standard Mode
I2C Speed Frequency (KHz)	100
Rise Time (ns)	0
Fall Time (ns)	0
Coefficient of Digital Filter	0
Analog Filter	Enabled
Timing	**0x10C0ECFF ***

Slave Features:

Clock No Stretch Mode	Disabled
General Call Address Detection	Disabled
Primary Address Length selection	7-bit
Dual Address Acknowledged	Disabled
Primary slave address	0

7.3. I2C2

I2C: I2C

7.3.1. Parameter Settings:

Timing configuration:

I2C Speed Mode	Standard Mode

I2C Speed Frequency (KHz)	100
Rise Time (ns)	0
Fall Time (ns)	0
Coefficient of Digital Filter	0
Analog Filter	Enabled
Timing	**0x10C0ECFF ***

Slave Features:

Clock No Stretch Mode	Disabled
General Call Address Detection	Disabled
Primary Address Length selection	7-bit
Dual Address Acknowledged	Disabled
Primary slave address	0

7.4. I2C4

I2C: I2C

7.4.1. Parameter Settings:

Timing configuration:

I2C Speed Mode	Standard Mode
I2C Speed Frequency (KHz)	100
Rise Time (ns)	0
Fall Time (ns)	0
Coefficient of Digital Filter	0
Analog Filter	Enabled
Timing	**0x10C0ECFF ***

Slave Features:

Clock No Stretch Mode	Disabled
General Call Address Detection	Disabled
Primary Address Length selection	7-bit
Dual Address Acknowledged	Disabled
Primary slave address	0

7.5. RCC

7.5.1. Parameter Settings:

RCC Parameters:

TIM Prescaler Selection	Disabled

HSE Startup Timout Value (ms)	100
LSE Startup Timout Value (ms)	5000
CSI Calibration Value	16
HSI Calibration Value	16

System Parameters:

VDD voltage (V)	3.3
Flash Latency(WS)	2 WS (3 CPU cycle)

Power Parameters:

Power Regulatror Voltage Scale	Power Regulator Voltage Scale 1

PLL range Parameters:

PLL1 clock Input range	Between 8 and 16 MHz
PLL1 clock Output range	Wide VCO range

7.6. SPI3

Mode: Full-Duplex Master

7.6.1. Parameter Settings:

Basic Parameters:

Frame Format	Motorola
Data Size	**24 Bits ***
First Bit	MSB First

Clock Parameters:

Prescaler (for Baud Rate)	**64 ***
Baud Rate	**6.25 MBits/s ***
Clock Polarity (CPOL)	Low
Clock Phase (CPHA)	1 Edge

Advanced Parameters:

CRC Calculation	Disabled
NSSP Mode	Enabled
NSS Signal Type	Software
Fifo Threshold	Fifo Threshold 01 Data
Tx Crc Initialization Pattern	All Zero Pattern
Rx Crc Initialization Pattern	All Zero Pattern
Nss Polarity	Nss Polarity Low
Master Ss Idleness	00 Cycle
Master Inter Data Idleness	00 Cycle
Master Receiver Auto Susp	Disable
Master Keep Io State	Master Keep Io State Disable
IO Swap	Disabled

7.7. SYS

Debug: Serial Wire

Timebase Source: TIM13

7.8. TIM1

Clock Source : Internal Clock

Channel1: PWM Generation CH1

7.8.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**50 ***
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**100 ***
Internal Clock Division (CKD)	No Division
Repetition Counter (RCR - 16 bits value)	0
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection TRGO	Reset (UG bit from TIMx_EGR)
Trigger Event Selection TRGO2	Reset (UG bit from TIMx_EGR)

Break And Dead Time management - BRK Configuration:

BRK State	Disable
BRK Polarity	High
BRK Filter (4 bits value)	0
BRK Sources Configuration	
- Digital Input	Disable
- COMP1	Disable
- COMP2	Disable
- DFSDM	Disable

Break And Dead Time management - BRK2 Configuration:

BRK2 State	Disable
BRK2 Polarity	High
BRK2 Filter (4 bits value)	0
BRK2 Sources Configuration	
- Digital Input	Disable
- COMP1	Disable
- COMP2	Disable

- DFSDM	Disable

Break And Dead Time management - Output Configuration:

Automatic Output State	Disable
Off State Selection for Run Mode (OSSR)	Disable
Off State Selection for Idle Mode (OSSI)	Disable
Lock Configuration	Off

Clear Input:

Clear Input Source	Disable

PWM Generation Channel 1:

Mode	PWM mode 1
Pulse (16 bits value)	**10 ***
Fast Mode	Disable
CH Polarity	High
CH Idle State	Reset

7.9. TIM2

Channel3: PWM Generation CH3

7.9.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**50 ***
Counter Mode	Up
Counter Period (AutoReload Register - 32 bits value)	**100 ***
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection TRGO	Reset (UG bit from TIMx_EGR)

Clear Input:

Clear Input Source	Disable

PWM Generation Channel 3:

Mode	PWM mode 1
Pulse (32 bits value)	**10 ***
Fast Mode	Disable
CH Polarity	High

7.10. TIM3

Slave Mode: Reset Mode
Trigger Source: TI1FP1
Clock Source : Internal Clock
Channel1: Input Capture direct mode
Channel2: Input Capture indirect mode
Channel3: Input Capture direct mode
Channel4: Input Capture direct mode

7.10.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**200 ***
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**0xFFFE ***
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable
Slave Mode Controller	Reset Mode

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection TRGO	Reset (UG bit from TIMx_EGR)

Input Capture Channel 1:

Polarity Selection	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter (4 bits value)	0

Input Capture Channel 2:

Polarity Selection	**Falling Edge ***
IC Selection	Indirect
Prescaler Division Ratio	No division

Input Capture Channel 3:

Polarity Selection	**Falling Edge ***
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter (4 bits value)	0

Input Capture Channel 4:

Polarity Selection	**Falling Edge ***
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter (4 bits value)	0

7.11. TIM4

Clock Source : Internal Clock

Channel2: PWM Generation CH2

7.11.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**50 ***
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**10 ***
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection TRGO	Reset (UG bit from TIMx_EGR)

Clear Input:

Clear Input Source	Disable

PWM Generation Channel 2:

Mode	PWM mode 1
Pulse (16 bits value)	**10 ***
Fast Mode	Disable
CH Polarity	High

7.12. TIM5

Clock Source : Internal Clock

Channel3: PWM Generation CH3

7.12.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**50 ***
Counter Mode	Up
Counter Period (AutoReload Register - 32 bits value)	**100 ***
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)

Trigger Event Selection TRGO	Reset (UG bit from TIMx_EGR)

Clear Input:

Clear Input Source	Disable

PWM Generation Channel 3:

Mode	PWM mode 1
Pulse (32 bits value)	**10 ***
Fast Mode	Disable
CH Polarity	High

7.13. TIM6

mode: Activated

7.13.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**4999 ***
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**0xFFFE ***
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Trigger Event Selection	Reset (UG bit from TIMx_EGR)

7.14. TIM8

Slave Mode: Reset Mode

Trigger Source: TI2FP2

Clock Source : Internal Clock

Channel1: Input Capture indirect mode

Channel2: Input Capture direct mode

7.14.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**200 ***
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**0xFFFE ***
Internal Clock Division (CKD)	No Division
Repetition Counter (RCR - 16 bits value)	0

auto-reload preload	Disable
Slave Mode Controller	Reset Mode

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection TRGO	Reset (UG bit from TIMx_EGR)
Trigger Event Selection TRGO2	Reset (UG bit from TIMx_EGR)

Input Capture Channel 1:

Polarity Selection	**Falling Edge ***
IC Selection	Indirect
Prescaler Division Ratio	No division

Input Capture Channel 2:

Polarity Selection	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter (4 bits value)	0

7.15. TIM12

mode: Clock Source

7.15.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**49999 ***
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**0xFFFE ***
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

7.16. TIM15

mode: Clock Source

Channel1: PWM Generation CH1

Channel2: PWM Generation CH2

7.16.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**200 ***
Counter Mode	Up

Counter Period (AutoReload Register - 16 bits value)	**19999 ***
Internal Clock Division (CKD)	No Division
Repetition Counter (RCR - 8 bits value)	0
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

Break And Dead Time management - BRK Configuration:

BRK State	Disable
BRK Polarity	High
BRK Filter (4 bits value)	0
BRK Sources Configuration	
- Digital Input	Disable
- COMP1	Disable
- COMP2	Disable
- DFSDM	Disable

Break And Dead Time management - Output Configuration:

Automatic Output State	Disable
Off State Selection for Run Mode (OSSR)	Disable
Off State Selection for Idle Mode (OSSI)	Disable
Lock Configuration	Off

PWM Generation Channel 1:

Mode	PWM mode 1
Pulse (16 bits value)	**1640 ***
Fast Mode	Disable
CH Polarity	High
CH Idle State	Reset

PWM Generation Channel 2:

Mode	PWM mode 1
Pulse (16 bits value)	**1480 ***
Fast Mode	Disable
CH Polarity	High
CH Idle State	Reset

7.17. TIM16

mode: Activated

7.17.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**49999 ***
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**0xFFFE ***
Internal Clock Division (CKD)	No Division
Repetition Counter (RCR - 8 bits value)	0
auto-reload preload	Disable

7.18. TIM17

mode: Activated

7.18.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**1999 ***
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**9999 ***
Internal Clock Division (CKD)	No Division
Repetition Counter (RCR - 8 bits value)	0
auto-reload preload	Disable

7.19. UART7

Mode: Asynchronous

7.19.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable
Prescaler	clock /1
Fifo Mode	FIFO mode disable
Txfifo Threshold	1 eighth full configuration
Rxfifo Threshold	1 eighth full configuration

Advanced Features:

Auto Baudrate	Disable
TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

7.20. UART8

Mode: Asynchronous

7.20.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable
Prescaler	clock /1
Fifo Mode	FIFO mode disable
Txfifo Threshold	1 eighth full configuration
Rxfifo Threshold	1 eighth full configuration

Advanced Features:

Auto Baudrate	Disable
TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

7.21. USART2

Mode: Asynchronous

7.21.1. Parameter Settings:

Basic Parameters:

Baud Rate	**100000 ***
Word Length	**9 Bits (including Parity) ***
Parity	**Even ***
Stop Bits	**2 ***

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable
Prescaler	clock /1
Fifo Mode	Disable
Txfifo Threshold	1 eighth full configuration
Rxfifo Threshold	1 eighth full configuration

Advanced Features:

Auto Baudrate	Disable
TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

7.22. FREERTOS

Interface: CMSIS_V1

7.22.1. Config parameters:

API:

FreeRTOS API	CMSIS v1

Versions:

FreeRTOS version	9.0.0
CMSIS-RTOS version	1.02

Kernel settings:

USE_PREEMPTION	Enabled
CPU_CLOCK_HZ	SystemCoreClock

TICK_RATE_HZ	1000
MAX_PRIORITIES	7
MINIMAL_STACK_SIZE	128
MAX_TASK_NAME_LEN	16
USE_16_BIT_TICKS	Disabled
IDLE_SHOULD_YIELD	Enabled
USE_MUTEXES	Enabled
USE_RECURSIVE_MUTEXES	Disabled
USE_COUNTING_SEMAPHORES	Disabled
QUEUE_REGISTRY_SIZE	8
USE_APPLICATION_TASK_TAG	Disabled
ENABLE_BACKWARD_COMPATIBILITY	Enabled
USE_PORT_OPTIMISED_TASK_SELECTION	Enabled
USE_TICKLESS_IDLE	Disabled
USE_TASK_NOTIFICATIONS	Enabled

Memory management settings:

Memory Allocation	Dynamic
TOTAL_HEAP_SIZE	15360
Memory Management scheme	heap_4

Hook function related definitions:

USE_IDLE_HOOK	Disabled
USE_TICK_HOOK	Disabled
USE_MALLOC_FAILED_HOOK	Disabled
USE_DAEMON_TASK_STARTUP_HOOK	Disabled
CHECK_FOR_STACK_OVERFLOW	Disabled

Run time and task stats gathering related definitions:

GENERATE_RUN_TIME_STATS	Disabled
USE_TRACE_FACILITY	Disabled
USE_STATS_FORMATTING_FUNCTIONS	Disabled

Co-routine related definitions:

USE_CO_ROUTINES	Disabled
MAX_CO_ROUTINE_PRIORITIES	2

Software timer definitions:

USE_TIMERS	Disabled

Interrupt nesting behaviour configuration:

LIBRARY_LOWEST_INTERRUPT_PRIORITY	15
LIBRARY_MAX_SYSCALL_INTERRUPT_PRIORITY	5

7.22.2. Include parameters:

Include definitions:

vTaskPrioritySet	Enabled
uxTaskPriorityGet	Enabled
vTaskDelete	Enabled
vTaskCleanUpResources	Disabled
vTaskSuspend	Enabled
vTaskDelayUntil	Disabled
vTaskDelay	Enabled
xTaskGetSchedulerState	Enabled
xTaskResumeFromISR	Enabled
xQueueGetMutexHolder	Disabled
xSemaphoreGetMutexHolder	Disabled
pcTaskGetTaskName	Disabled
uxTaskGetStackHighWaterMark	Disabled
xTaskGetCurrentTaskHandle	Disabled
eTaskGetState	Disabled
xEventGroupSetBitFromISR	Disabled
xTimerPendFunctionCall	Disabled
xTaskAbortDelay	Disabled
xTaskGetHandle	Disabled

*** User modified value**

8. System Configuration

8.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
I2C1	PB6	I2C1_SCL	Alternate Function Open Drain	No pull-up and no pull-down	Low	
	PB7	I2C1_SDA	Alternate Function Open Drain	No pull-up and no pull-down	Low	
I2C2	PF0	I2C2_SDA	Alternate Function Open Drain	No pull-up and no pull-down	Low	
	PF1	I2C2_SCL	Alternate Function Open Drain	No pull-up and no pull-down	Low	
I2C4	PF14	I2C4_SCL	Alternate Function Open Drain	No pull-up and no pull-down	Low	
	PF15	I2C4_SDA	Alternate Function Open Drain	No pull-up and no pull-down	Low	
SPI3	PC10	SPI3_SCK	Alternate Function Push Pull	No pull-up and no pull-down	Low	DRV_SPI_SCK
	PC11	SPI3_MISO	Alternate Function Push Pull	No pull-up and no pull-down	Low	DRV_SPI_MISO
	PC12	SPI3_MOSI	Alternate Function Push Pull	No pull-up and no pull-down	Low	DRV_SPI_MOSI
SYS	PA13 (JTMS/SWDIO)	SYS_JTMS-SWDIO	n/a	n/a	n/a	
	PA14 (JTCK/SWCLK)	SYS_JTCK-SWCLK	n/a	n/a	n/a	
TIM1	PK1	TIM1_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	DRV_CLKIN_Ch1
TIM2	PB10	TIM2_CH3	Alternate Function Push Pull	No pull-up and no pull-down	Low	DRV_CLKIN_Ch4
TIM3	PB0	TIM3_CH3	Alternate Function Push Pull	No pull-up and no pull-down	Low	PWM_IN_Ch2
	PB1	TIM3_CH4	Alternate Function Push Pull	No pull-up and no pull-down	Low	PWM_IN_Ch3
	PC6	TIM3_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	PWM_IN_Ch1
TIM4	PD13	TIM4_CH2	Alternate Function Push Pull	No pull-up and no pull-down	Low	DRV_CLKIN_Ch2
TIM5	PH12	TIM5_CH3	Alternate Function Push Pull	No pull-up and no pull-down	Low	DRV_CLKIN_Ch3
TIM8	PC7	TIM8_CH2	Alternate Function Push Pull	No pull-up and no pull-down	Low	PWM_IN_Ch4
TIM15	PE5	TIM15_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	PWM_SERVO_1
	PE6	TIM15_CH2	Alternate Function Push Pull	No pull-up and no pull-down	Low	PWM_SERVO_2
UART7	PF6	UART7_RX	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PF7	UART7_TX	Alternate Function Push Pull	No pull-up and no pull-down	Low	
UART8	PE0	UART8_RX	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PE1	UART8_TX	Alternate Function Push Pull	No pull-up and no pull-down	Low	
USART2	PD5	USART2_TX	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PD6	USART2_RX	Alternate Function Push Pull	No pull-up and no pull-down	Low	
GPIO	PC0	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	Btn_SS

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
	PC1	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	Led_SS
	PC2_C	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	Btn_AP_Enable
	PC3_C	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	Btn_AP_Start
	PE8	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	DRV_SCS_Ch4
	PE12	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	DRV_RESET_Ch4
	PE13	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	DRV_ENABLE_Ch4
	PE14	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	DRV_BRAKE_Ch4
	PE15	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	DRV_DIR_Ch4
	PB11	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	DRV_SCS_Ch3
	PH8	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	DRV_RESET_Ch3
	PH9	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	DRV_ENABLE_Ch3
	PH10	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	DRV_BRAKE_Ch3
	PH11	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	DRV_DIR_Ch3
	PB13	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	DRV_SCS_Ch2
	PD9	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	DRV_RESET_Ch2
	PD10	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	DRV_ENABLE_Ch2
	PD11	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	DRV_BRAKE_Ch2
	PD12	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	DRV_DIR_Ch2
	PD15	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	DRV_SCS_Ch1
	PJ9	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	DRV_RESET_Ch1
	PJ10	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	DRV_ENABLE_Ch1
	PJ11	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	DRV_BRAKE_Ch1
	PK0	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	DRV_DIR_Ch1
	PD0	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	Led_1
	PD1	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	Led_2
	PD2	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	Led_3
	PD3	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	Led_4
	PD4	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	SBUS2_Tx_Enable
	PD7	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	SBUS2_Rx_Enable
	PJ14	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	Power_PSU_12v
	PJ15	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	Power_LTM_C
	PG9	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	Power_PSU_5v
	PK4	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	Power_LTM_B
	PK5	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	Power_LTM_A
	PK6	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	Power_DRV_4
	PK7	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	Power_DRV_3
	PG15	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	Power_DRV_2
	PB3 (JTDO/TRACESWO)	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	Power_DRV_1

8.2. DMA configuration

nothing configured in DMA service

8.3. BDMA configuration

nothing configured in DMA service

8.4. MDMA configuration

nothing configured in DMA service

8.5. NVIC configuration

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Pre-fetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	15	0
System tick timer	true	15	0
USART2 global interrupt	true	5	0
TIM8 update interrupt and TIM13 global interrupt	true	0	0
UART7 global interrupt	true	5	0
UART8 global interrupt	true	5	0
TIM17 global interrupt	true	5	0
PVD and AVD interrupts through EXTI line 16	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		
TIM1 break interrupt	unused		
TIM1 update interrupt	unused		
TIM1 trigger and commutation interrupts	unused		
TIM1 capture compare interrupt	unused		
TIM2 global interrupt	unused		
TIM3 global interrupt	unused		
TIM4 global interrupt	unused		
I2C1 event interrupt	unused		
I2C1 error interrupt	unused		
I2C2 event interrupt	unused		
I2C2 error interrupt	unused		
TIM8 break interrupt and TIM12 global interrupt	unused		
TIM8 trigger and commutation interrupts and TIM14 global interrupt	unused		
TIM8 capture compare interrupt	unused		
TIM5 global interrupt	unused		
SPI3 global interrupt	unused		
TIM6 global interrupt, DAC1_CH1 and DAC1_CH2 underrun error interrupts	unused		
FPU global interrupt	unused		
I2C4 event interrupt	unused		

Interrupt Table	Enable	Preenmption Priority	SubPriority
I2C4 error interrupt	unused		
TIM15 global interrupt	unused		
TIM16 global interrupt	unused		
HSEM1 global interrupt	unused		

*** User modified value**

9. Software Pack Report