Characterizing and Comparing a D-Type Flip-Flop (DFF) with a Pre-Discharge Soft-Error Tolerant Flip-Flop (PDFF-SE)

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Abstract

The purpose of the project is to replicate, design and simulate a new DFF called "Pre-Discharge Soft-Error Tolerant Flip-Flop" (PDFF-SE) proposed by David Li in **[1]** and compare it against a conventional D-type Flip-Flop (DFF) to see their performance.

The PDFF-SE is designed in such a way to enhance the performance and improve the metastability of a dynamic logic circuit for high speed operations. Part of the characterization includes finding the propagation delays and the metastable regions of each circuit.

The simulations and analysis were performed using the parameters shown in **Table 1** and **Table 2** with *0-to-1* transitions of the clock at 27°C, TT with minimum channel length of 100nm, and a supply voltage of 1.2 V.

The kit used to perform the analysis was the GPDK 90nm from TSMC. The software was Cadence Virtuoso 6.1.5. A supplementary tool used was Matlab R2014b.

Parameter	Value
DC Voltage	1.2 V
Resistor	1 KOhm
Capacitors	50 fF
Rise/Fall Times for Data and Clock	50 ps
Pulse Width for Data	300 ps
Pulse Width for Clock	180 ps
Data Frequency	1.25 GHz
Clock Frequency	2.5 GHz
For Hold Time	
Transient Analysis Run time	4 us
Delay time for Data	40 ps
Delay time for Clock	30 ps
Period of Data	799.93 ps
Period of Clock	400 ps
For Setup Time	
Transient Analysis Run time	3.2 us
Delay time for Data	20 ps
Delay time for Clock	280 ps
Period of Data	800.7 ps
Period of Clock	400 ps

Table 1. Parameters for Conventional DFF and PDFF-SE analysis

Parameter	Value
DC Voltage	1.2 V
Resistor	1 KOhm
Capacitors	50 fF
Rise/Fall Times for Data and Clock	50 ps
Pulse Width for Data	600 ps
Pulse Width for Clock	600 ps
Data Frequency	833.3 MHz
Clock Frequency	1.667 GHz
For Hold Time	
Transient Analysis Run time	4 us
Delay time for Data	40 ps
Delay time for Clock	30 ps
Period of Data	1.99998 ns
Period of Clock	600 ps
For Setup Time	
Transient Analysis Run time	3.2 us
Delay time for Data	20 ps
Delay time for Clock	280 ps
Period of Data	1.20002 ns
Period of Clock	600 ps

Table 2. Parameters for the Transistor Sizing trials in PDFF-SE

1. General D Type FF Characteristics

Time Measurements

Setup time

Minimum time between a transition in D and the sampling edge of the CLK such that, even under worst case conditions, the Q will be guaranteed to change so as to become equal to the new D value.

Hold time

Minimum time that the D must be held constant after the sampling edge of the CLK, assuming that the most recent transition in D occurred no later than t_{setup} prior to the sampling edge of CLK, so that the Q output will remain stable after the end of the CLK pulse.

Negative Setup/Hold Times

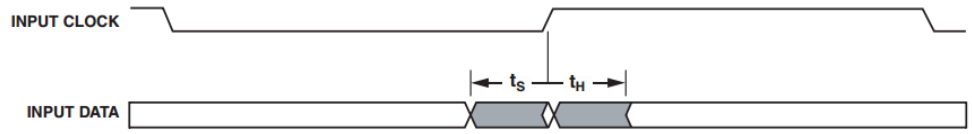

Figure 1. The Setup and Hold times are positive **[2]**.

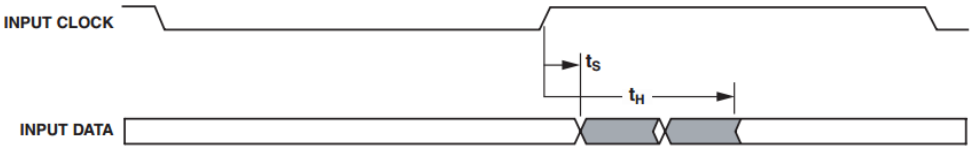

Figure 2. The Setup time is negative and the Hold times is positive **[2]**.

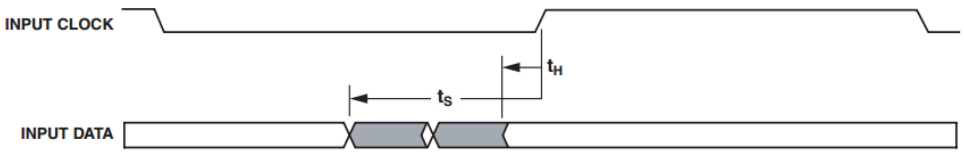

Figure 3. The Setup time is positive and the Hold times is negative **[2]**.

Figure 1 shows the normal operation where the setup and hold times have a comfortable amount of time to generate a valid Q output.

As seen in **Figure 2**, the device is said to have a negative setup time and positive hold time when the rising edge of the data comes after the rising edge of the clock and still give a valid Q output, if the time constraints are satisfied that is.

The device is said to have a positive setup time and negative hold time and positive when the falling edge of the data comes before the rising edge of the clock and still give a valid Q output, as seen in **Figure 3**.

2. Regions of operation for a Flip-Flop

Stable Region

Region where the t_{CQ} is constant, regardless of the data arrival time t_{DC}.

Quasi-stable Region

Region where as the t_{DC} decreases, the t_{CQ} delay starts to rise monotonously. The t_{DQ} reaches a minimum value, referred as the optimum Setup Time $t_{setup\_optimum}$.

Metastable Region

Region where the t_{CQ} delay is much larger than the normal delay (stable region), and increases exponentially.

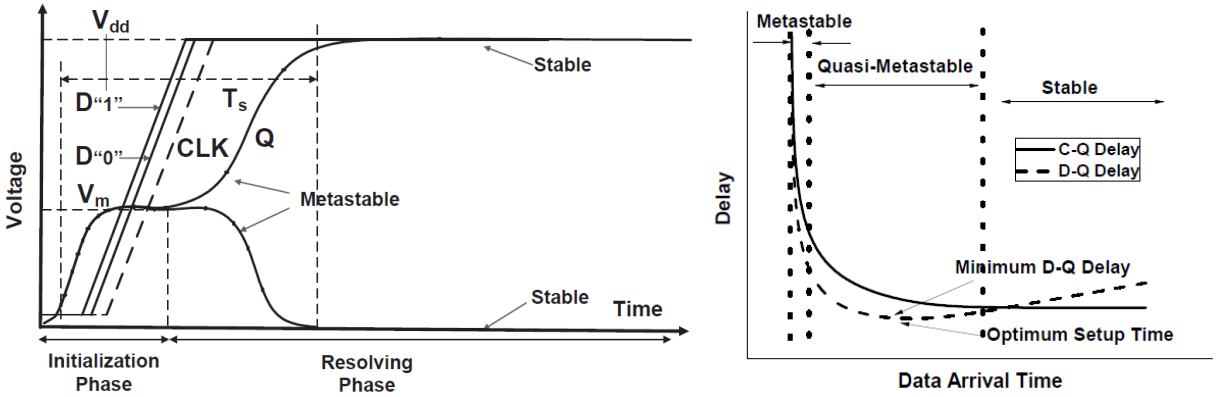

Figure 4. Transient waveforms of Data, Clock and Output describing the several parameters **[1]**.

3. Metastability

It is a phenomenon where a bistable element enters and undesirable third state in which the output is at an intermediate level between logic “0” and “1”.

Metastability occurs when the setup/hold window for the circuit is violated.

In a flip-flop, it happens when the input data D makes a transition inside $t_{aperture}$.

Two parameters are normally extracted from simulation to model and analyze the delay behavior in the metastable region: T_0 and τ.

4. Metastable window

$$\delta(t_s) = \frac{T_0}{e^{\frac{t_s}{\tau}}} = T_0 \cdot e^{-\frac{t_s}{\tau}} \qquad (\mathbf{1})$$

δ or T_w: It is the metastability window.

It is the time period where data transitions cannot be resolved within a given settling (resolution) time t_s, and it should be kept as small as possible. If a data transition arrives inside this window, it will not be resolved. **[3]**

T_0: Asymptotic width of the metastability window with no settling time.

It cannot be measured directly. It is a conceptual time window, extrapolated from the exponential behavior of the flip-flop during prolonged metastability, related to the setup time and minimum voltage required for a valid output.

This can also be defined as the smallest data input arrival to clock edge time such that, for all arrival times larger than this, the t_{CQ} delay does not increase above its nominal value.

It defines a window in which a data transition may cause a metastable event **[3]**.

τ : Regeneration (Resolution) time constant.

It represents the inverse of the gain-bandwidth product of the feedback element in the flip-flop.

It is a constant determined by the circuit topology, transistor sizes, and the chip fabrication. It determines how long the metastable state will last if the device enters such state.

t_s: Settling, Observation, or Resolution time of metastability.

It is the amount of slack time available (allowed) for the output to settle to a stable stage, in excess of the normal propagation delay time.

It is the amount of time from the sampling edge of the clock to when the output has reached a logic high or low value.

It is the maximum time the output can remain metastable, without causing synchronizer failure (gets out of metastability after that time).

$$t_s = t_{CLK} - t_{CQnom} - t_{setup} \qquad (2)$$

Under normal operation, when the flip-flop exhibits no metastability, the settling time is the nominal t_{CQ} delay value, $t_{s(nom)}$.

The equation says that the settling time t_s starts to count from t_{CQnom}, where there is no change in t_{CQ} delay for a diminish in t_{DC} delay, and it has to end before limit of t_{setup} of the next clock cycle.

In other words, it must be done within one period of the clock minus the amount of the required setup time, and no more.

The τ and T_0 constants are related to electrical characteristics of the device and may vary according to the process technology **[9]**.

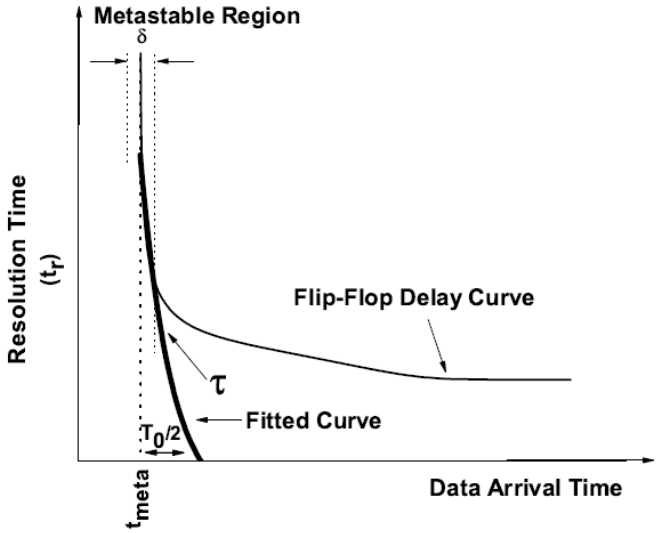

Figure 5. Plot of resolution (settling) time vs Data arrival time [1].

5. Method for finding Setup Time, Hold Time, and Metastability using Transient Analysis

Setup Time

First, the metastability region for setup time is found by plotting the input data *rising* edges arriving at different time delays, each time delay getting shorter than the previous one, with respect to the rising clock edge (t_{DC}).

At the same time, the clock-to-output delay is plotted, to see how long it takes for the data to be reflected at the output, depending on the time of arrival (t_{CQ}).

Under stable region, the t_{CQ} delay will maintain stable for decreasing t_{DQ} delay (t_{CQnom}).

Assuming that the hold time is satisfied, the setup time, as a safe margin, can be determined as the value of t_{DC} delay where intercepts the point located 10% above the t_{CQnom},.

The optimum setup time is taken as the lowest point of the t_{DQ} delay vs t_{DC} curve.

Hold Time

The metastability region for hold time is found in a similar way for the setup time.

It is found by plotting the input data *falling* edges occuring at different time delays, each time shorter than before, with respect to the rising clock edge.

The data signal has to be stable long enough *before* the clock edge arrives, for the setup time not to be violated.

Metastability

The quasi-metastable region (t_s region) and metastable region (t_{meta} region) are also found through these procedures.

Once the t_{CQ}starts to rise (exponentially), then it is said that the device has entered into quasi-metastable region.

The quasi-metastable region ends when t_{CQ} delay is equal to t_s. Any more rise of the t_{CQ} indicates that the device has entered into metastable region.

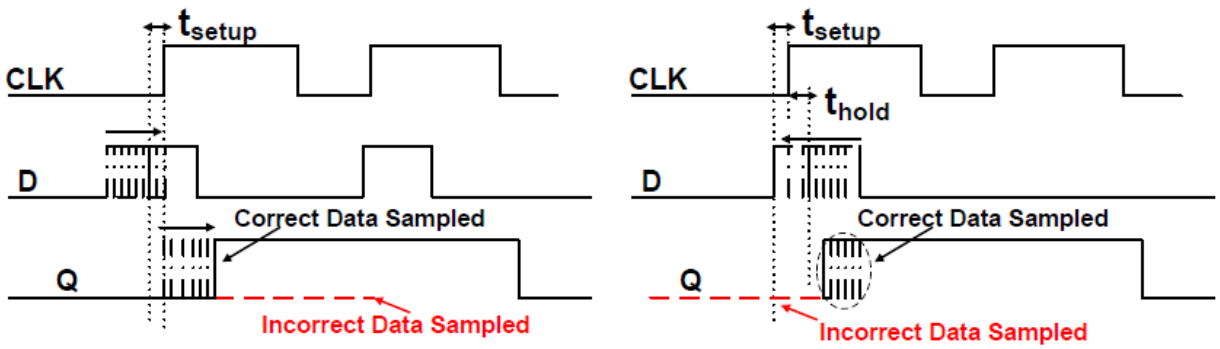

Figure 6. Flip-Flop timing waveforms [1].

Delay Measurements

Clock-to-Output delay t_{CQ}

Propagation delay from the CLK to output Q, assuming that the input data D has been set early enough, relative to the leading edge of the CLK.

Data-to-Output Delay t_{DQ}

Propagation delay from the input data D to the output Q, assuming the CLK has been turned ON early enough, relative to the transition of D signal.

Data-to-Clock Delay T_{DC}

The flip-flop delay is measured as the time between the latest point of data arrival and the corresponding output transition.

6. Method for extracting τ and T_0 constants from simulation

To extract the τ and T_0 from the simulation, the t_{CQ} delay vs the displacement between the input data D and the clock signal, t_{DC}, is plotted for a given flip-flop architecture.

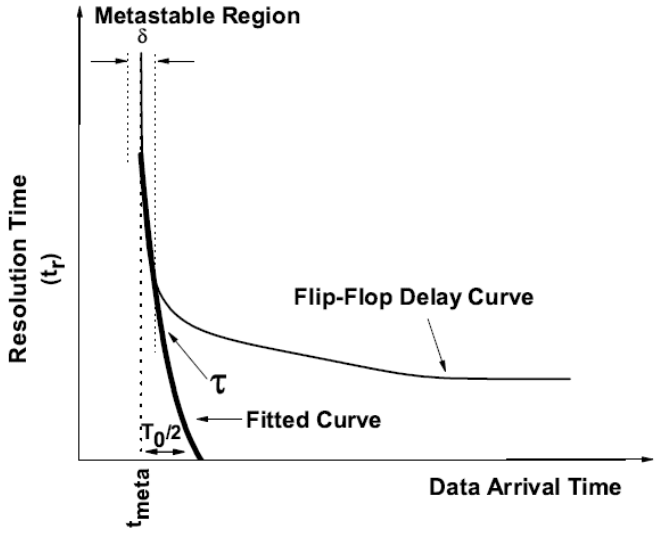

Figure 7. Plot of resolution (settling) time vs Data arrival time, revisited for convenience.

t_{meta}: The metastable point at which the flip-flop fails to capture the correct data.

The last data arrival time where new data is captured is defined as t_s, and the first where it is not bound is defined as t_{meta}.

If an input transition occurs at exactly t_{meta}, the device (theoretically) has an infinite resolution time t_s.

When the input data signal approaches at this time t_{meta}, t_s will grow exponentially, requiring the maximum time to resolve which could be infinite, and the input logic value is no longer latched by the flip-flop at that point.

Once t_{meta} is determined, the data arrival time t_{DC} is displaced logarithmically to one side of t_{meta} **[11]**.

The value of t_{meta} is subtracted from the setup's t_{DC}, giving the x-axis $t_{D-tmeta}$, or:

$$t_{D-tmeta} = t_{DC} - t_{meta} \qquad (3)$$

The settling (resolution) time t_s is plotted vs $t_{D-tmeta}$ in a semilog scale.

The t_s is referred to have a value of zero where t_{CQ} delay is nominal (i.e. non-metastable operation of the latch). This means that the input transition satisfies the setup and hold times of the device.

A fitted/extrapolated linear curve is obtained from resolution time t_s (starting from t_{CQnom} delay) vs the time displacement between the input data (t_{DC}) and t_{meta}, plotted on an x-axis semi-log scale. This leads to:

$$\tau = -\frac{1}{slope}$$

$$\log_{10}(T_0/2) = \log_{10}(x\ intercept)$$

$$\frac{T_0}{2} = x\ intercept$$

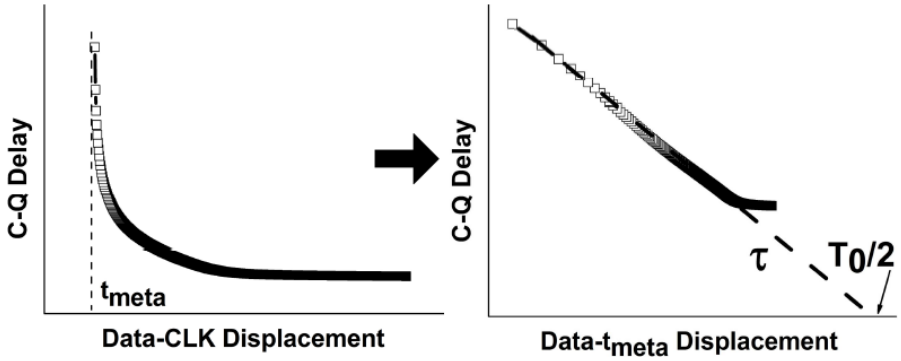

Figure 8. Plot describing how to extract τ and T_0 [1].

As described in a previous section, when the transition of the input data signal to clock is close to t_{meta}, t_s grows exponentially **[8]**.

To recreate the fitted curve, the linear extrapolation equation is used for 3 points or coordinates:

$$y_3 = y_1 + \frac{(y_2 - y_1)}{(x_2 - x_1)} \cdot (x_3 - x_1) \qquad (\mathbf{4})$$

Since the x-axis points are in log base 10:

$$y_3 = y_1 + \frac{(y_2 - y_1)}{\log_{10}(x_2/x_1)} \cdot \log_{10}(x_3/x_1) \qquad (\mathbf{5})$$

$$\tau = -\frac{(y_2 - y_1)}{\log_{10}(x_2/x_1)} \qquad (6)$$

$$T_0 = 2 \times x_3 \qquad (7)$$

7. Design Metrics for the Flip-Flop

Mean-Time-Between-Failures

It indicates the average time interval between two successive failures in a system.

A higher value increases the overall reliability of the system.

$$MTBF = \frac{e^{t_s/\tau}}{f_D \cdot f_{CLK} \cdot T_0} = \frac{1}{f_D \cdot f_{CLK} \cdot \delta(t_s)} \qquad (8)$$

f_D: Data transition frequency

f_{CLK}: Clock frequency

The probability that the data will transition within the metastability window δ, is simply $f_D \cdot \delta(t_s)$.

The MTBF increases exponentially as the metastability settling time t_s inscreases.

A good approach is to design metastable-hardened flip-flops with smaller T_0 and τ.

A small value of τ results in fast flip-flop resolution time from the metastability region, and thus increases the MTBF.

As the clock frequency and the data transition frequency increases, the MTBF decreases as a result of a smaller settling time t_s.

The larger the metastability window $\delta(t_s)$, the shorter the MTBF.

A way to calculate the resolution time constant, from the critical path, is the following

$$\tau = \frac{C_Q + 4C_M}{g_m - {}^1/_R} \qquad (9)$$

C_Q: Critical path capacitances. It includes the gate and diffusion capacitances of the transistors.

C_M: Is the Miller capacitance, which is simply the coupling capacitance between the gate and the Source/Drain terminal of a MOSFET.

g_m: Transconductance of an inverter, which is the contribution of the NMOS and the PMOS transconductances, at the critical path.

R: Equivalent resistance of an inverter.

PDP

The Power-Delay-Product is a common metric used for analyzing the tradeoff between the propagation delay and power consumption.

The PDP represents the average energy consumed per switching event.

$$\alpha = \frac{\#\ of\ Signal\ Transitions}{\#\ of\ Signals\ \times \#\ of\ Clock\ Cycles}\ \% \qquad (\mathbf{10})$$

α: The switching activity

PDP is calculated as the worst t_{DQ} delay and the power dissipation for a given α.

$$PDP = P_{ave}(\alpha) \cdot t_{DQ} \qquad (\mathbf{11})$$

MDP

It is the product between τ and the flip-flop delay for a given transistor sizing scheme.

$$MDP = \tau \cdot t_{DQ} \qquad (\mathbf{12})$$

Small transistor sizes of the inverters means lower power and delay, but higher τ values.

As the inverter pair size increases, the reduction of τ comes at the expense of performance degradation.

This design metric is used to find the best design (balanced) trade-off between the delay (metastability) and τ, focused on reliability and high-performance.

$$t_{DQ} = t_{CQnom} + t_{setup} \qquad (\mathbf{13})$$

MPDP

It is called the Metastability-Power-Delay-Product, and it focuses in power consumption:

$$MPDP = P_{ave}(\alpha) \cdot t_{DQ} \cdot \tau = PDP \cdot \tau \qquad (\mathbf{14})$$

8. Brief Description of the Pre-Discharged Flip-Flop Soft-Error Tolerant

The objective of this circuit is to reduce the $\boldsymbol{\tau}$ and the T_0 to improve the metastability of a combinational logic circuit. This is achieved by modifying the *transistor sizes* of the master and slave stages in the pre-discharge soft-error flip-flop.

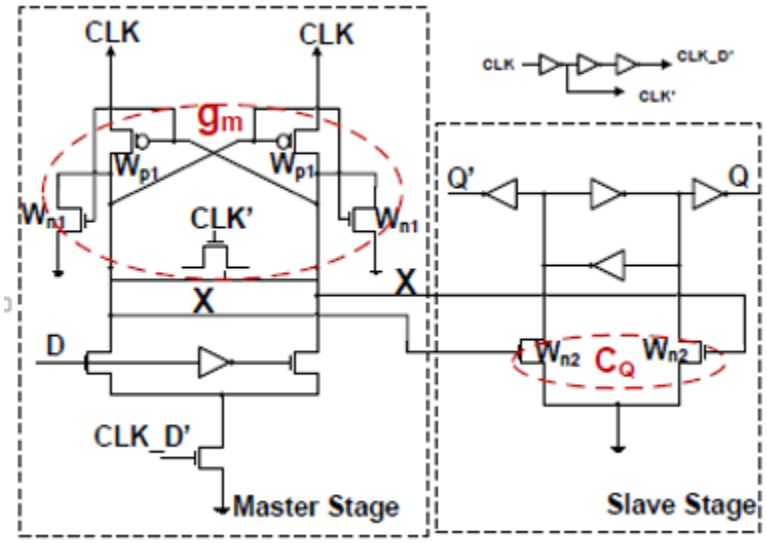

Figure 9. Schematic of a PDFF **[1]**.

One of the methods of reducing the T is to increase the trans-conductance (Gm) of the cross-coupling inverter loop at the master stage or by reducing the parasitic and Miller capacitance (**equation 9**). So, to increase Gm, we can increase the cross-coupled inverter transistor sizes in the master stage.

Master-Stage

The master-stage consists of a differential cross-coupled inverter with a positive feedback in the critical path. The clock is connected to the drain PMOS transistors.

A pre-discharge circuit is connected by the use of an equalizer transistor $\overline{CLK}$ to pre-discharge the SET and RESET nodes to prevent a false evaluation when the CLK is low.

When CLK is high, the critical path in the Master-Stage is reduced to just one of the PMOS pass-transistors (active inverter) to charge one of the internal nodes to logic "1".

The transparency window is created by a pulse generator to allow a negative setup time as you will see later in the report. Allowing a negative setup time is an improvement in the performance as well as in the soft-edge robustness against clock skew.

Slave Stage

When the master stage is at a discharging phase, $\overline{CLK}$ is low, and depending on the data transitions, either the SET or the RESET will remain at logic "0" and the other will be pulled up to logic "1" by the either of the PMOSs' in cross-coupled inverters in the master stage. There will be further elimination of the footer NMOS transistor in the slave stage which will enhance the speed and performance of the circuit. And the outputs Q and $\overline{Q}$ are retained by the SRAM-based cross-coupled inverters in the slave stage.

Single-Event Transients

A Single Event Upsets (SEU) is an event that modifies the charge in a node or capacitor, and can cause an SRAM-based devices (i.e. FPGAs) to lose their configuration due to a change in a bit, driving the device to malfunction or making it to behave unpredictably.

SEU is caused by charged particles (i.e. alpha particles) striking at a sensitive node inside a microelectronic device, changing the flip-flop or memory's state.

Therefore, the Quatro cell has been introduced to restore the value at any node when it is modified due to single-event transient (SET). This restoration occurs when other unaffected nodes help to restore the correct value of the affected node, because one transistor of each inverter driving one of the affected nodes is driven by one unaffected node.

Slave-Stage and the Modified Quatro-SE cell

The Quatro cell is used to help restore the value at any node when it is modified due to single-event transient (SET). This restoration occurs when other unaffected nodes help to restore the correct value of the affected node, because one transistor of each inverter driving one of the affected nodes is driven by one unaffected node.

The PDFF-SE has a different slave-stage, in which is benefits from a Modified Quatro soft-error cell circuit, as seen in **Figure 10** and **Figure 11**.

When the master stage is at a discharging phase, $\overline{CLK}$ is low. Depending on the data transitions, either the SET or $RESET$ node will remain at logic "0" and the other will be pulled up to logic "1" by the either of the PMOSs' in cross-coupled inverters in the master stage.

The outputs Q and $\overline{Q}$ are retained by the Quatro cell in the slave stage.

The advantage for the Quatro cell is that it can facilitate many differential FF architectures due to its requirement to be connected to differential signals to be written into the cell location of either of the 4 important nodes (X1 and X2, or X3 and X4).

The addition of tolerant cells impact the FF performance by adding more resistivity, in terms of changing the values stored at the critical nodes during the normal operation of the flip-flops.

Hence, two additional CLK-controlled transistors are added to the Quatro (M7 and M8) cell respectively in order to maintain high-performance (see **Figure 10**). These transistors are controlled either by CLK in the Master-stage, or $CLKB$ in the Slave-stage.

Once a SET upsets a node, the affected node is restored by the corresponding NMOS or PMOS connected to that affected node is switched on and isn't driven by an affected node.

Therefore, the critical nodes in the PDFF-SE are connected to and protected by the Quatro cell.

To even further improve the Quatro cell, two additional clock-controlled transistors are added to maintain high performance **[1].** Hence, the modified Quatro cell.

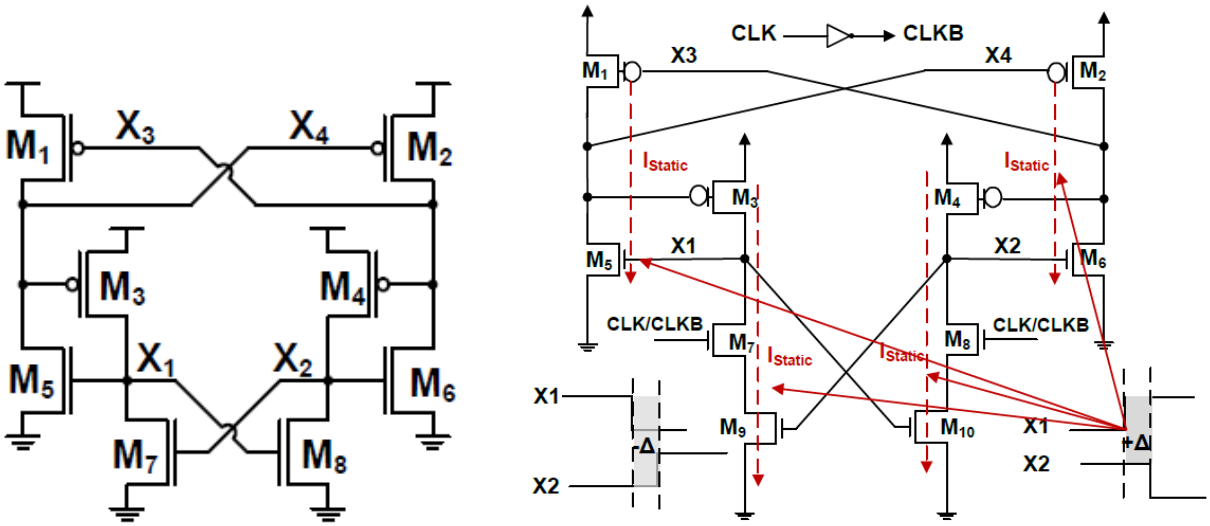

Figure 10. Quatro SE cell (left) and Modified Quatro SE cell (right) **[1]**.

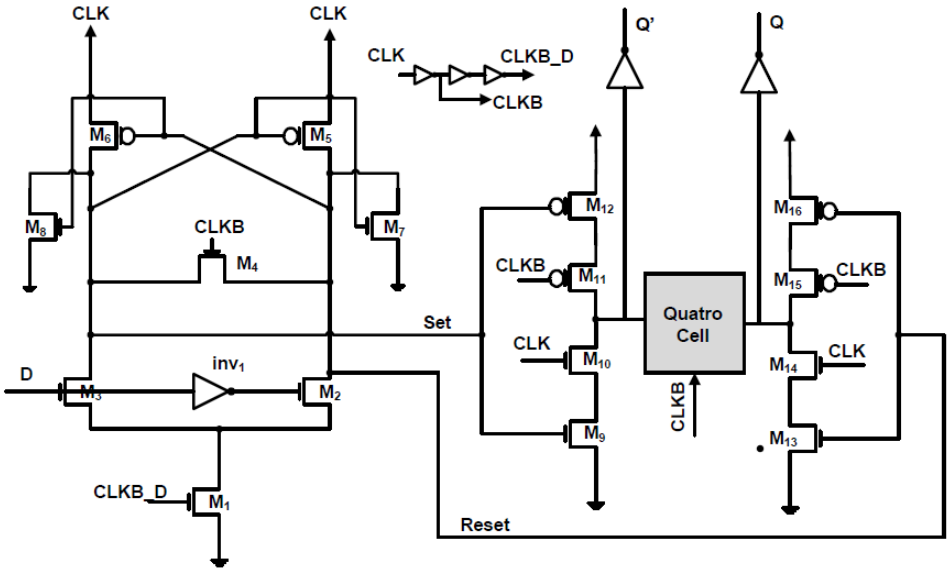

Figure 11. Schematic of the PDFF-SE **[1]**.

9. Transparency Window and Negative Setup Time of the PDFF (PDFF-SE)

A transparency window is created using a pulse generator to allow negative setup time.

A negative setup time is the time that the input D can change after the clock edge, and nevertheless the new level will be correctly sampled, provided that it remains stable after that time.

Allowing a negative setup time is an improvement in the performance as well as in the soft-edge robustness against clock skew.

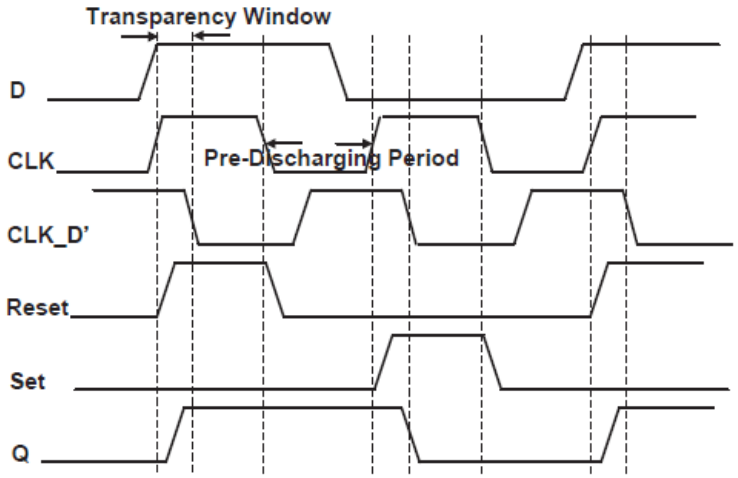

Figure 12. Timing waveform of the PDFF-SE **[1]**.

The output data is retained in the Slave-Stage by the SRAM-based cross-coupled inverter pair.

During the period in which the transparency window is closed, both pull-down paths in the Master-Stage are off.

While CLK = 0, CLKB activates M4, and pre-discharges the nodes SET and RESET to logic 0.

When both nodes are zero, the Slave-Stage holds the data to its current state.

When the transparency window is open, M4 is off, and depending on the input D, one of the pull-down paths is ON while the other is OFF, such that either SET or RESET will remain at 0 and the other at logic 1 from the cross-coupled PMOS transistors.

Due to the pre-discharging, the pull-down path in the Master-Stage is no longer on the critical path, because it simply prevents any wrong evaluation outside the transparency window.

As soon as M4 is OFF, the *evaluation period* begins, and the critical path in the Master-Stage becomes just a single PMOS transistor, raising the signal SET or RESET to logic 1 while CLK is high.

10. Procedure and Results

Analysis of the DFF

The purpose is to design and simulate a D-type Flip-Flop to find the setup and hold times, and the asymptotic width T_0 of the metastability window.

Using an already designed schematic of the DFF named DFFQX1, from the gsclib090 library in Cadence Virtuoso's 90nm Technology, a symbol was created to be used for the test bench.

The clock and data signals are delivered by ideal pulse voltage sources, connected to an RC network and are buffered by BUFX2 elements. The output of the DFF is buffered by BUFX4. Both buffer elements come from the gsclib090 library, and symbols were created for them to be used on the test bench.

For more realistic data and clock signals that have been fed from the ideal voltage sources, capacitors were added as loads at the outputs and the inputs and inverting buffers were added. Half the size of a buffer is placed at the input of the DFF compared to the buffer size placed at the output (the same test bench is used for the PDFF.)

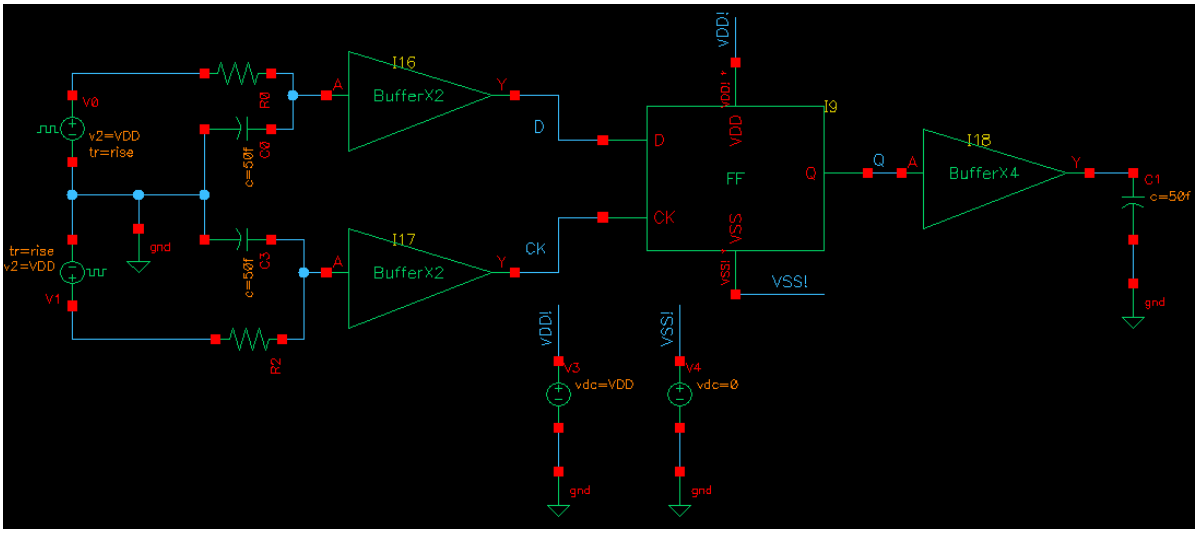

Figure 13. D-type Flip-Flop test-bench.

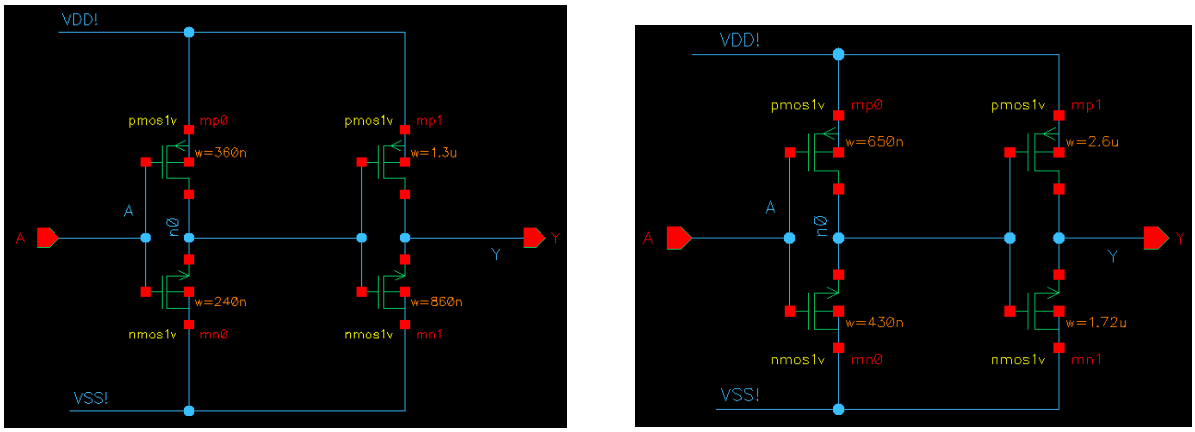

Figure 14. BUFX2 schematic (left) and BUFX4 schematic (right).

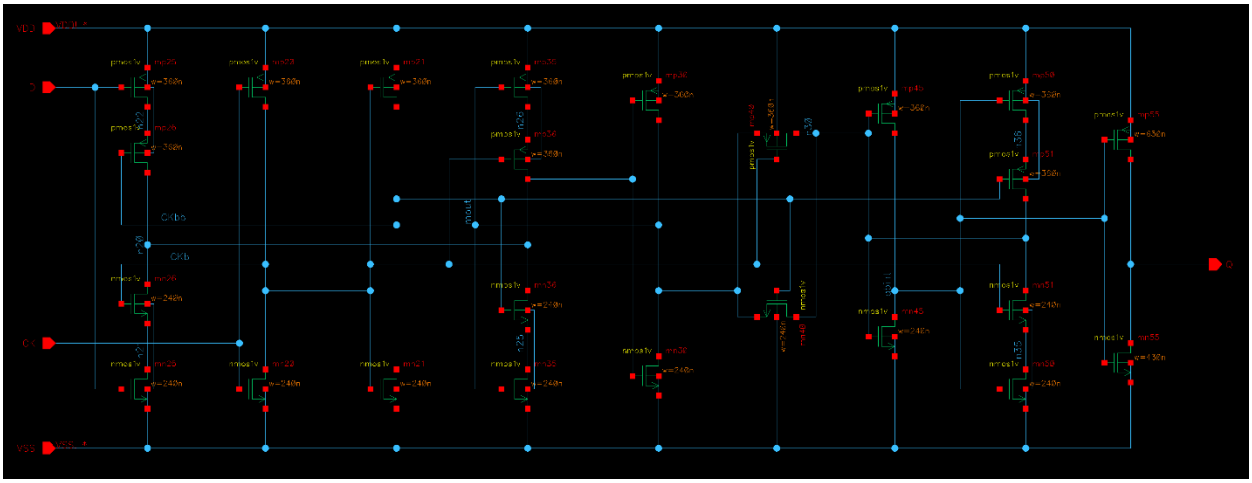

Figure 15. Schematic of the D-type Flip Flop

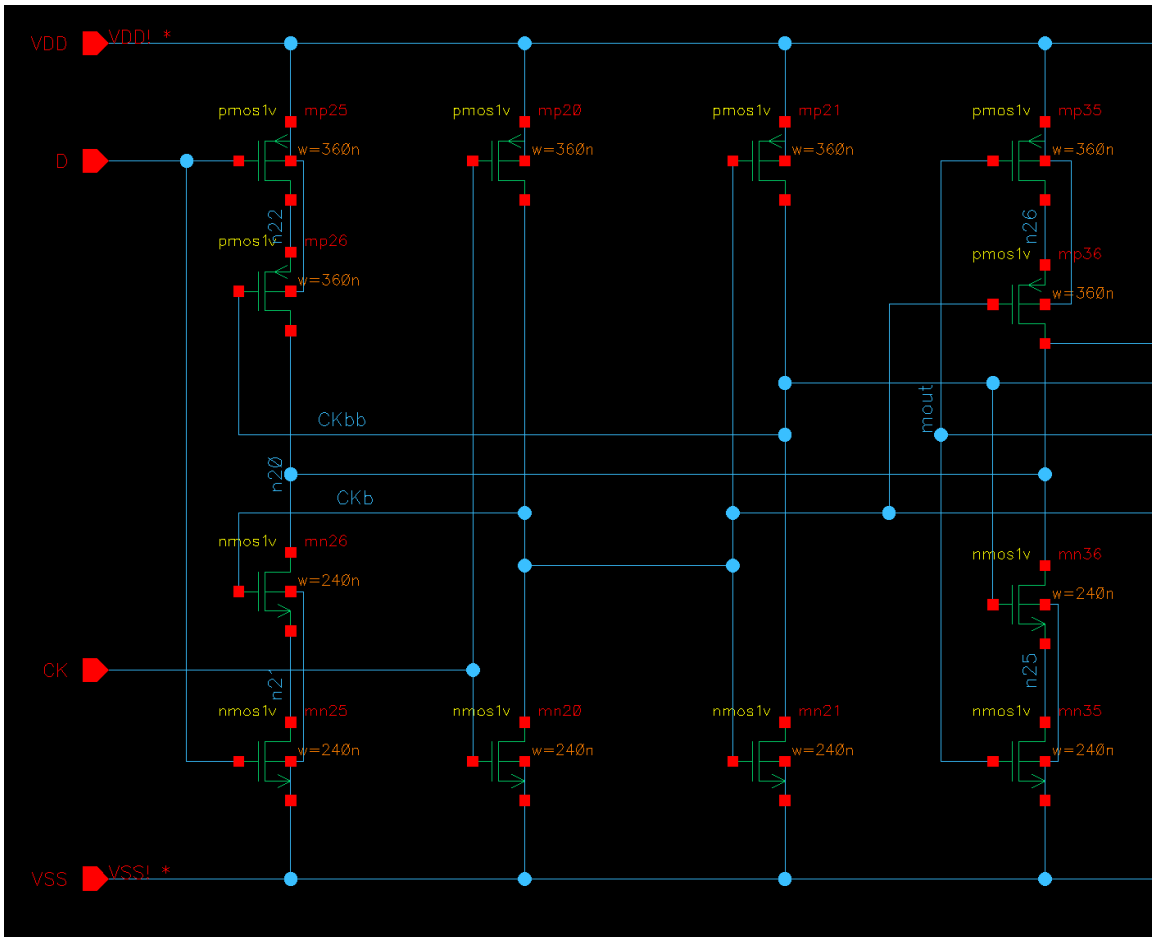

Figure 16. Left-half of the D-type FF schematic.

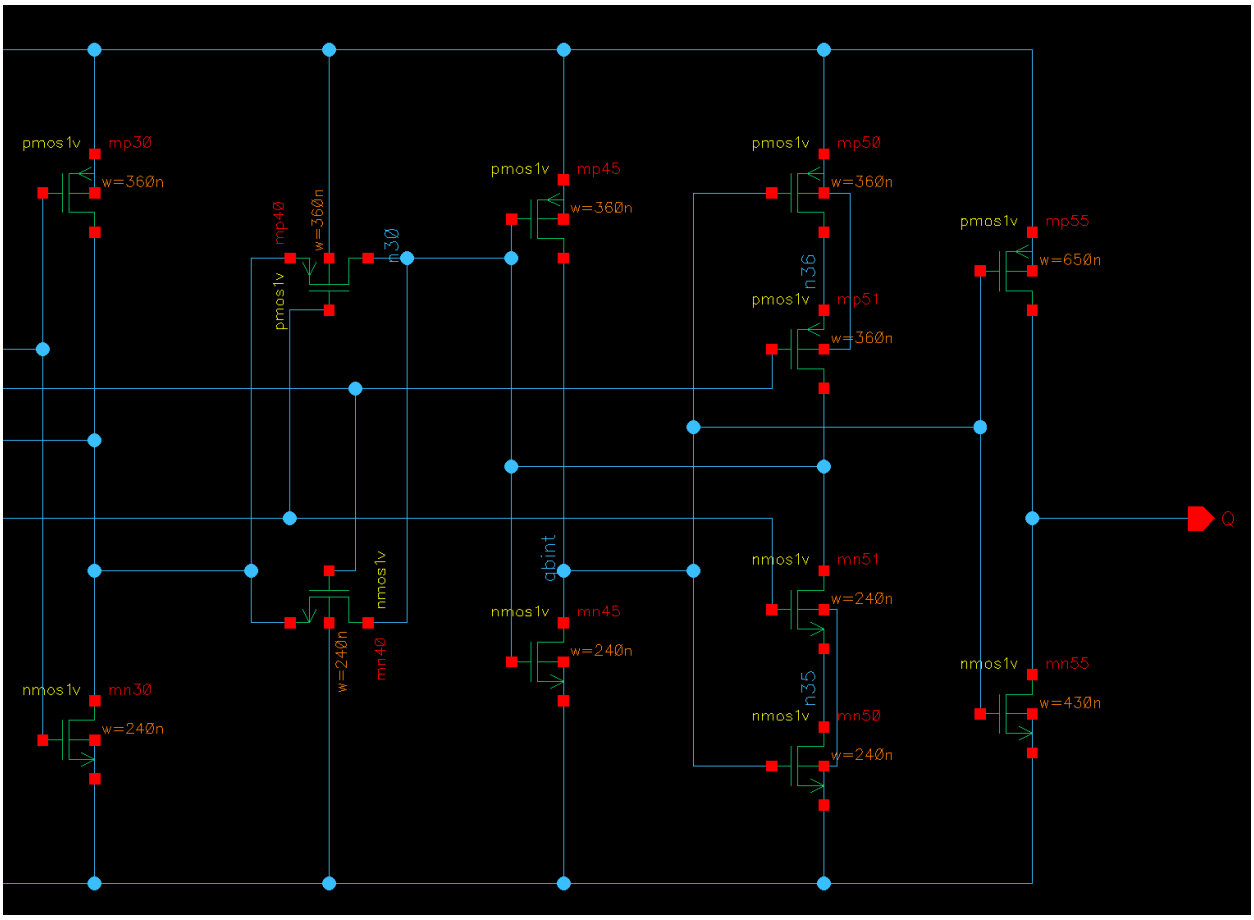

Figure 17. Right-half of the D-type FF schematic.

The steps described in **Section 5** are implemented for the simulations. **Figure 18** shows the ADE settings for the transient analysis for setup and hold time. The output waveforms of D, CLK and Q are shown in **Figure 19** for setup time.

As part of the method, both clock and data signals will start with different initial delays, and the clock signal is set to run twice the frequency of the data.

Then the data is made to run at a frequency slightly faster than half of the clock frequency for setup time. The data signal rising edge will “catch up” the rising edge of the clock signal, decreasing t_{DC} delay.

The data frequency is made to run slightly slower than half of the clock frequency for hold time. This will make the falling edge of the data signal to appear closer and closer to the rising edge of the clock from behind.

Figures 20-22 show the delay function settings for setup time.

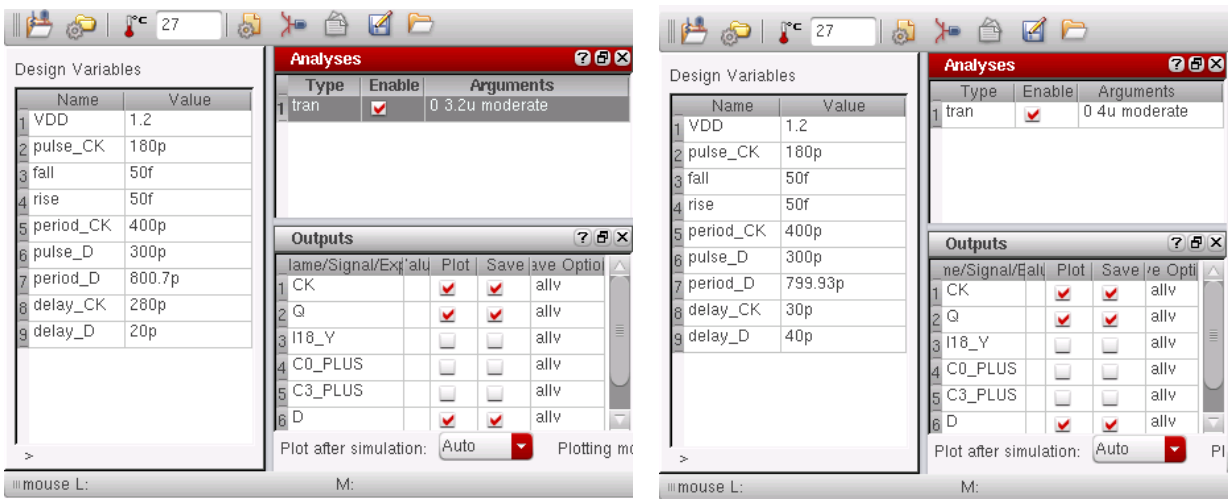

Figure 18. ADE settings for Setup Time (left) and Hold Time (right) transient simulation of the D-type FF.

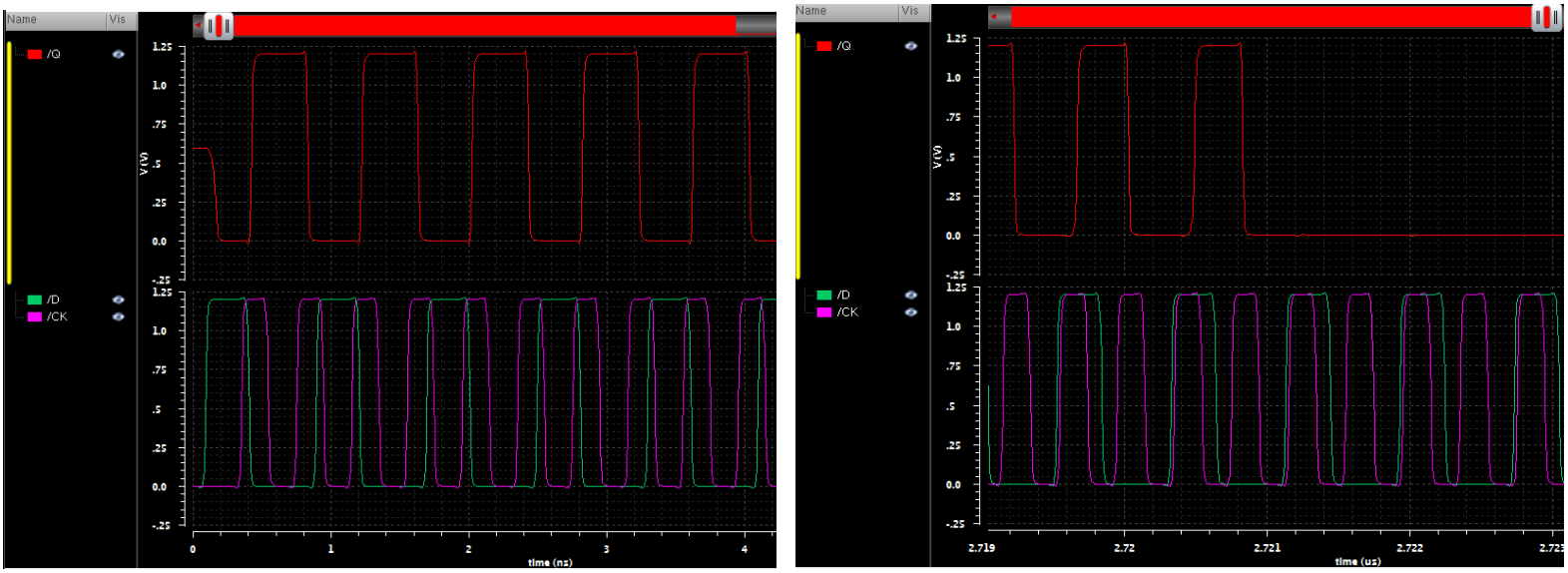

Figure 19. Example of the transient waveforms of Data, Clock and Output for Setup Time Simulation.

The left image in **figure 19** shows the signals at the beginning of the runtime for the setup simulations.

Due to the period of the D that we have assigned in table 1, the data signal's frequency decreases gradually. Therefore the clock's rising edge will eventually catch up with the Data's rising edge, as in the right image in **figure 19** near the end of the runtime.

However, the Q will stop giving a valid output transition before the clock (CK) went ahead of the data's rising edge. These output results showed that the DFF circuit maintained the positive setup time.

Furthermore, when simulating for the hold time, we will see both the positive setup time and the negative hold time in one simulation.

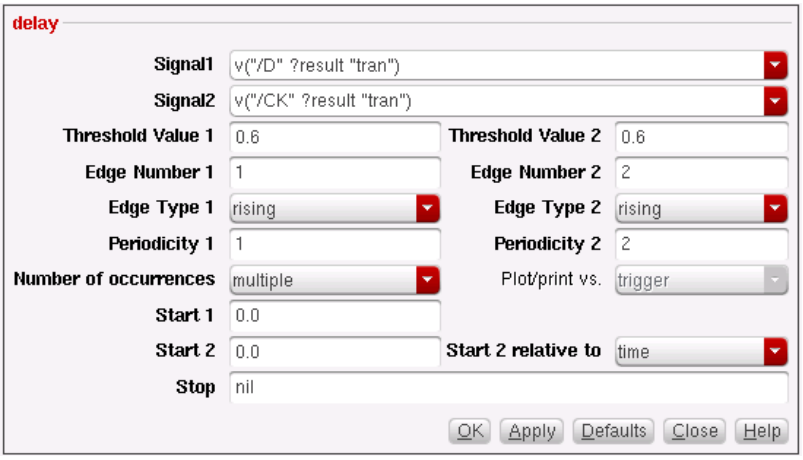

Figure 20. Delay function configuration for t_{DC}

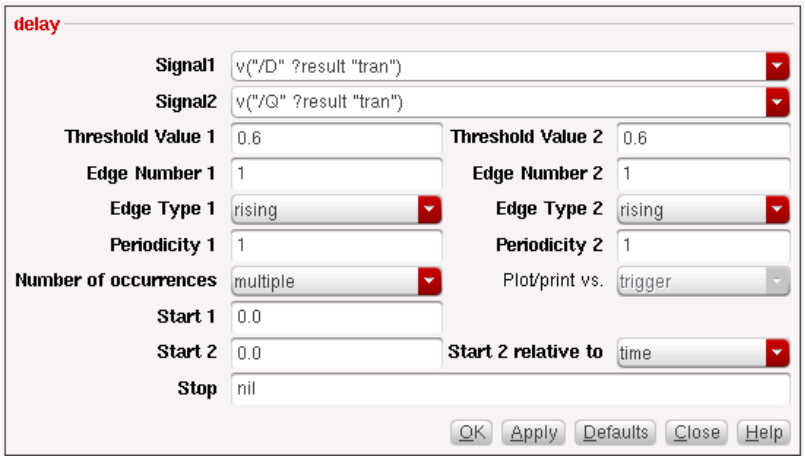

Figure 21. Delay function configuration for t_{DQ}

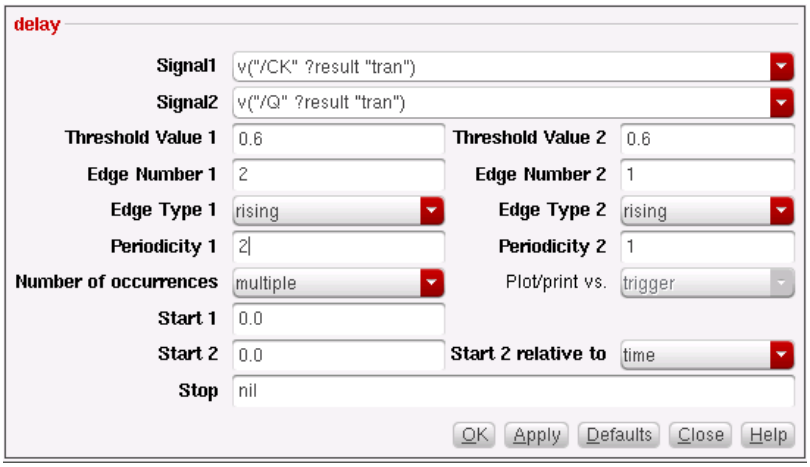

Figure 22. Delay function configuration for t_{CQ}

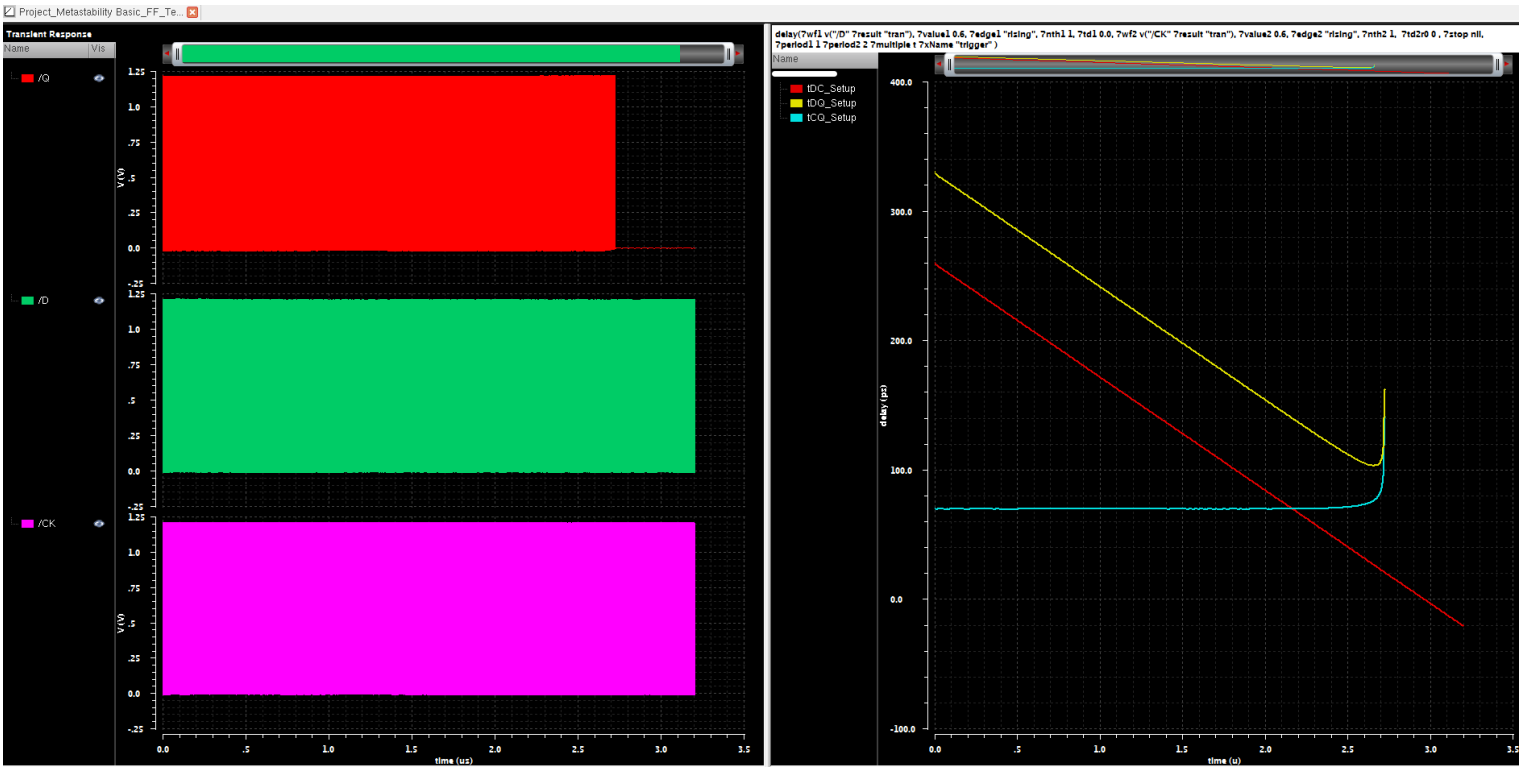

Figure 23. Example of the t_{DC}, t_{DQ}, and t_{CQ} plots after applying the delay function.

After applying the delay function to find the different curves, **Figure 23** shows the outcome.

The next step is to plot t_{DQ} and t_{CQ} against t_{DC} by performing a "Y vs Y" function directly in the plot.

Figure 24 shows the complete picture, that includes the setup and hold time.

Note :

For the hold time analysis, it follows the same configuration as in **Figures 20-22**, except that the edge for D has to be set as "falling".

With the settings shown in **Table 1** and in **Figure 18**, the plot of the curves for setup and hold time is shown in **Figure 24**.

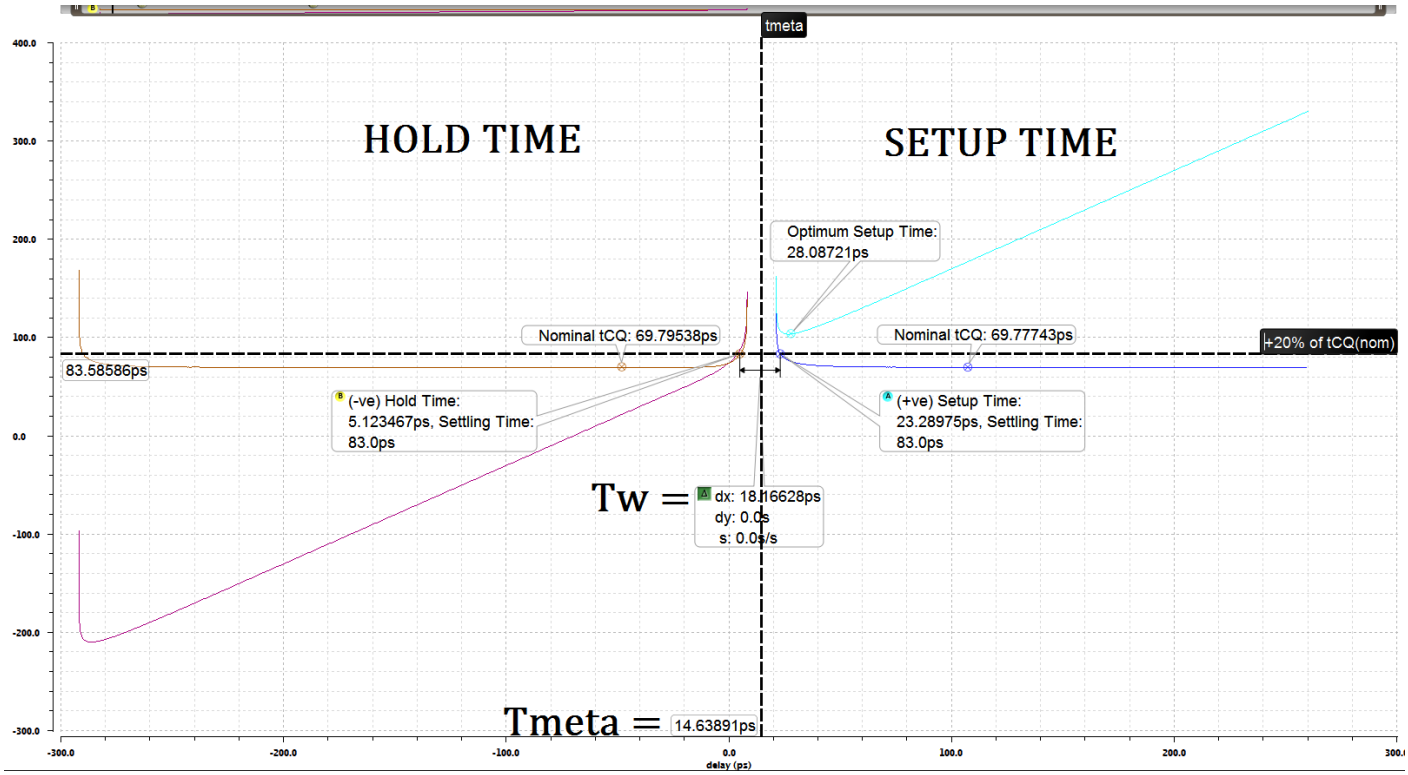

Figure 24. Plot of t_{CQ}, t_{DQ}, and t_{DC} for setup and hold time of the D-type FF, following settings from Table 1.

It is seen that the left-hand side of **Figure 24** has the Hold time delay outputs, and the right-side has the Setup time outputs.

This DFF has a positive setup time, t_{setup}, and a negative hold time, t_{hold}. The edge of the clock on the figure above is represented as the 0 point at the x-axis.

The stable region is where the t_{CQ} delay curve is constant with time on t_{DC} axis, the quasi-stable region is when the delay starts to increase on both the $t_{CQ}$and t_{DC} axis, and the metastable region is when the curve increases on the y-axis only and rises exponentially.

The metastable window δ for this device could be measured from 10-20% above the nominal value of the t_{CQ}. From that same point, the setup and hold times can be measured with respect to the zero point (clock edge).

For our case, the setup and hold times are flipped on the x-axis, meaning the setup time should have been on the left side while the hold is on the right. Looking at the graph, both T_{setup} and T_{hold} occurred before the 0 (the rising edge of the clock) on the x-axis. This tells us that the falling edge of the data occurred before the rising edge of the clock. Taking that into consideration (and as mentioned earlier), we get our setup time to be positive and the hold time to be negative.

t_{meta} is the point where the circuit no longer gives a valid Q output, therefore, t_{meta} could vary from the point where the $t_{CQ-setup}$ enters a metastable state until the point where $t_{CQ-hold}$ had entered the metastable state.

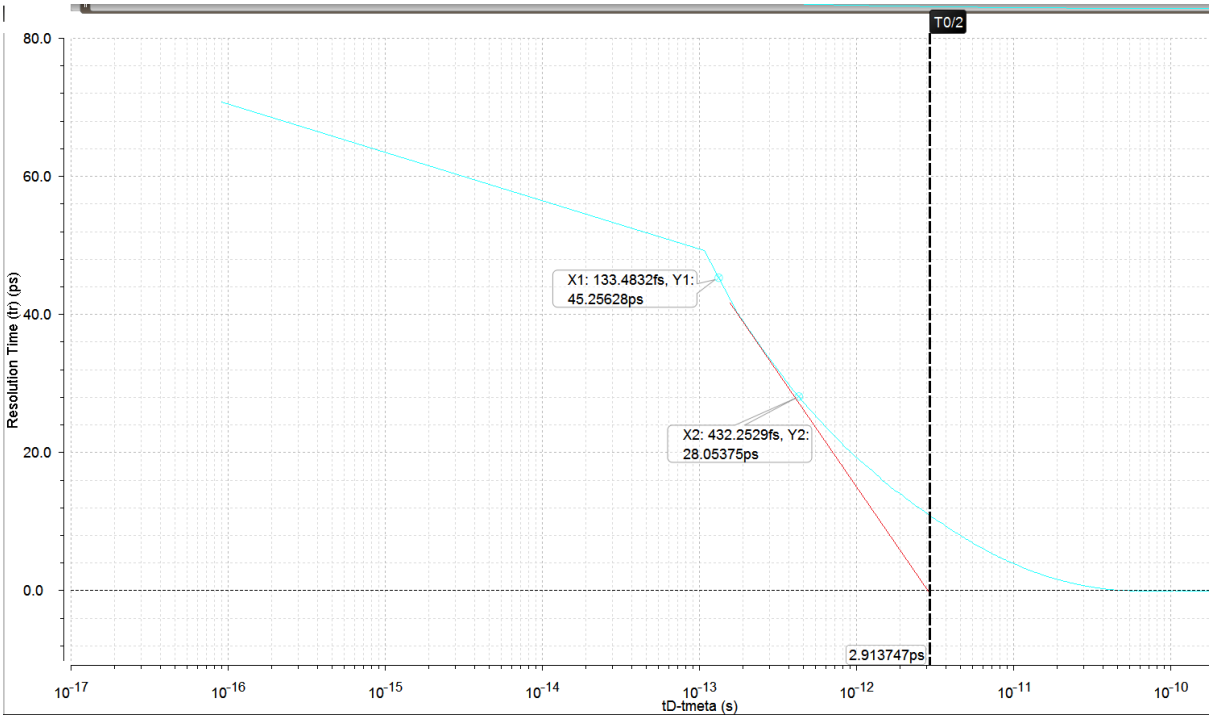

Figure 25. Plot describing the extrapolated curve for the D-type FF

As described in previous sections, it is possible to get the fitted curve. By taking two points, T_0 and τ can be calculated using equations **(5)** to **(7)**.

Having that $x_1 = 133.48fs,\ y_1 = 45.25ps, x_2 = 432.25fs,\ y_2 = 28ps$ and $y_3 = 0$, solving for x_3:

$$\tau = -\frac{(28ps - 45.25ps)}{\log_{10}(432.25fs/133.48fs)} = 33.8\ ps$$

$$y_3 = 45.25ps + \frac{(28ps - 45.25ps)}{\log_{10}(432.25fs/133.48fs)} \cdot \log_{10}(x_3/133.48fs) = 2.9\ ps$$

$$T_0 = 2 \times x_3$$

$$T_0 = 2 \times 2.9\ ps = 5.8\ ps$$

$$delay = t_{CQ} + t_{setup} = 69.79\,ps + 23.29\,ps = 93.08\,ps$$

$$t_s = t_{CLK} - delay = 400ps - 93.08ps = 306.9\,ps$$

$$f_D = number\ of\ transitions\ of\ the\ data = 1.25G\ x\ 2 = 2.5GHz$$

$$MTBF = \frac{e^{306.9p/33.8p}}{2.5G \cdot 2.5G \cdot 5.8p} = 302\ x\ 10^3\ s = 84\ hours$$

$$MDP = \tau \cdot t_{DQ} = 33.8\,ps \cdot 93.08\,ps = 31\ x\ 10^{-22}\ s^2$$

Parameter	Conventional DFF
τ	33.8 ps
$\boldsymbol{T_0}$	58.72 ps
$\boldsymbol{T_s}$	306.9 ps
Nominal $\boldsymbol{T_{CQ}}$	69.79 ps
$\boldsymbol{T_{DQ}}$	93 ps
$\boldsymbol{T_{setup}}$	23.29 ps
$\boldsymbol{T_{hold}}$	- 5.12 ps
$\boldsymbol{T_w}$	18.16 ps
$\boldsymbol{t_{meta}}$	14.63 ps
MDP	31 x 10^{-22} s^2
MTBF	84 hours

Table 5.Result for the conventional DFF.

Analysis of the PDFF-SE

The following figures show the testbench, and schematic with transistor values of the PDFF-SE.

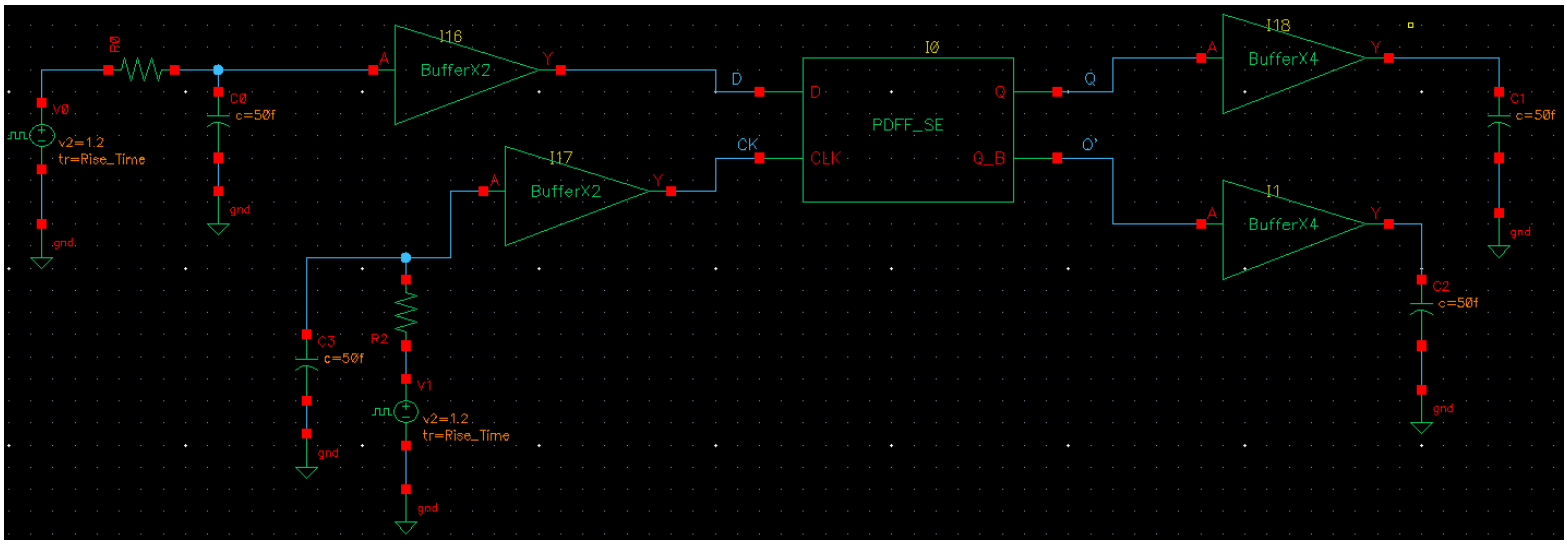

Figure 26. Test Bench for the PDFF-SE

PDFF-SE Schematic

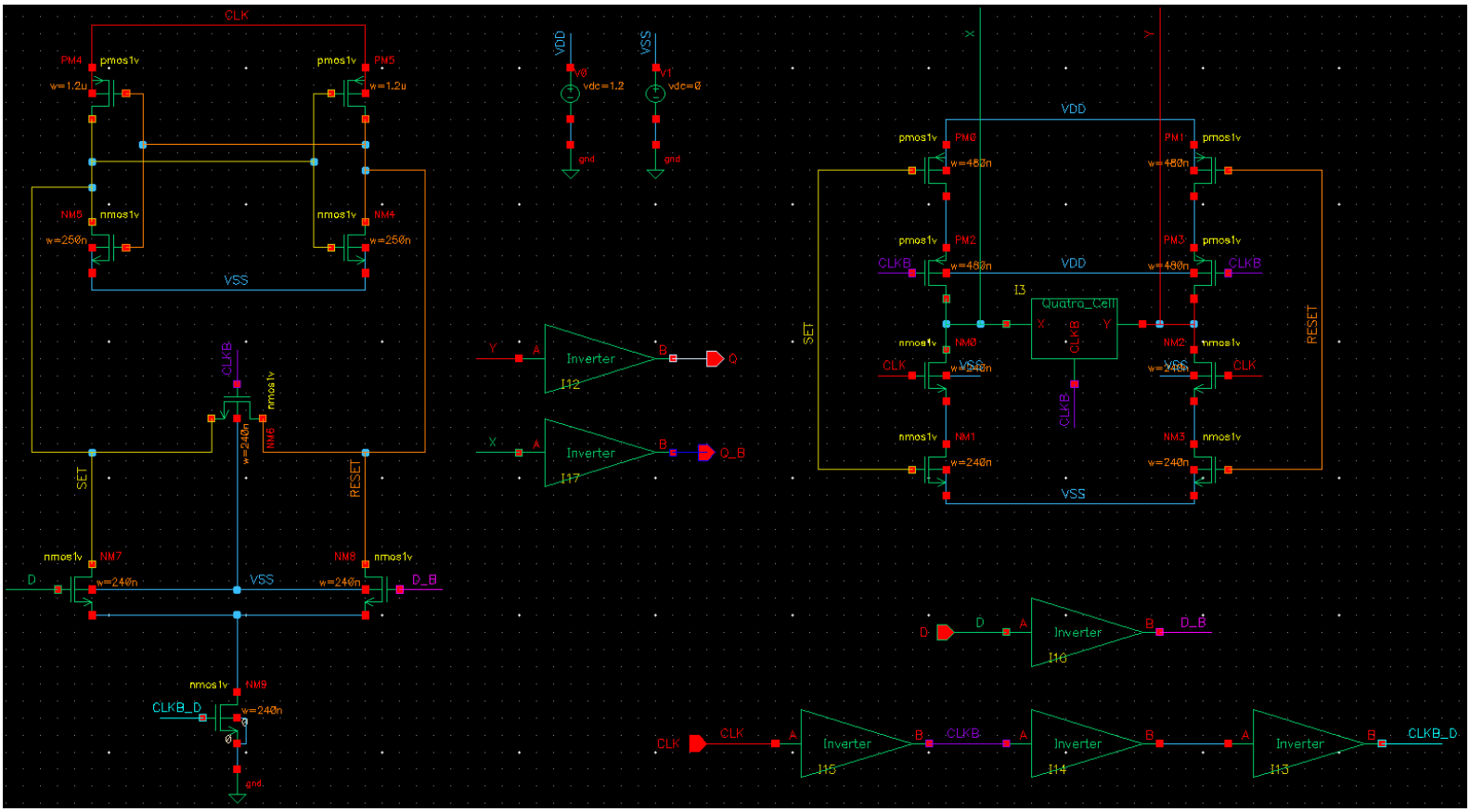

Figure 27. Schematic of the PDFF-SE.

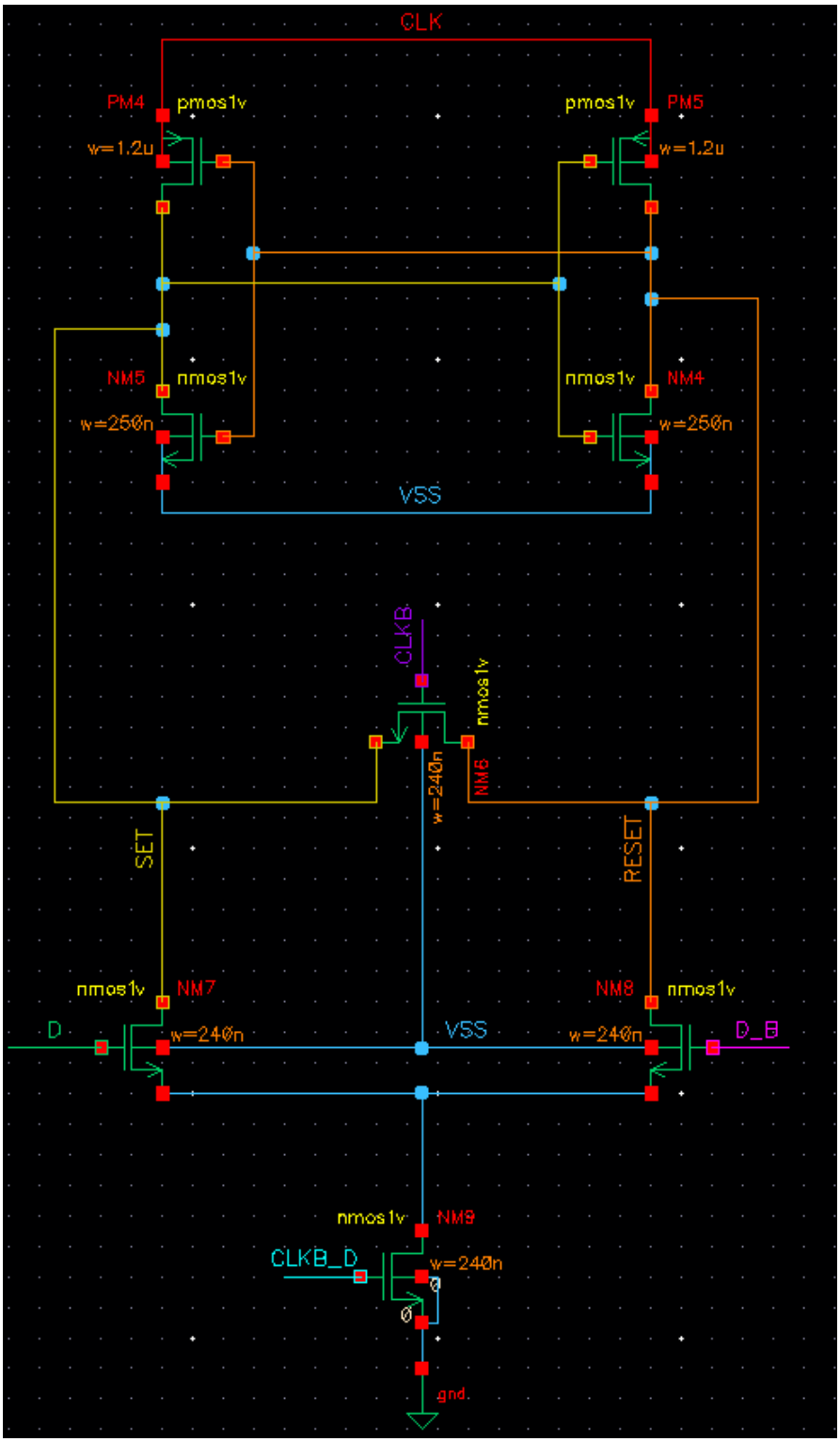

Figure 28. Schematic of the Master-Stage of the PDFF-SE.

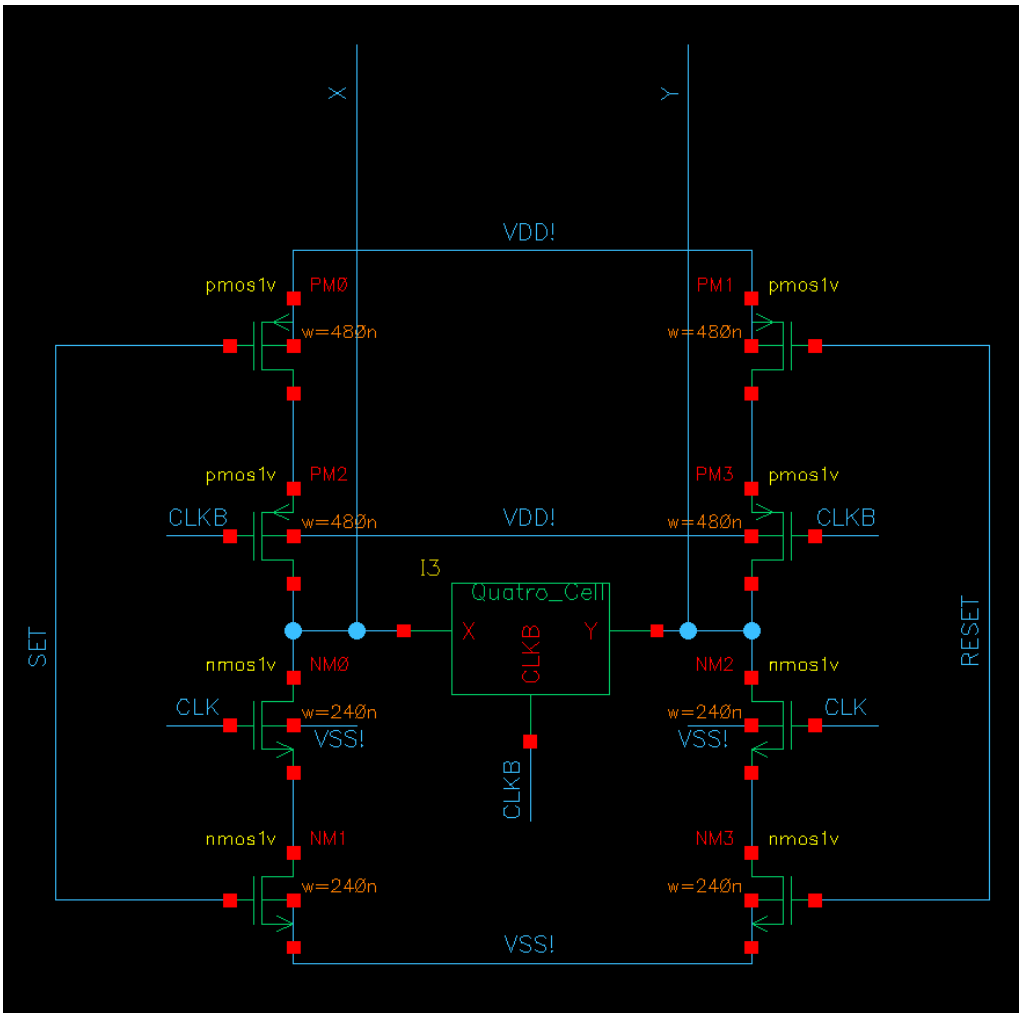

Figure 29. Schematic of the Slave-Stage of the PDFF-SE.

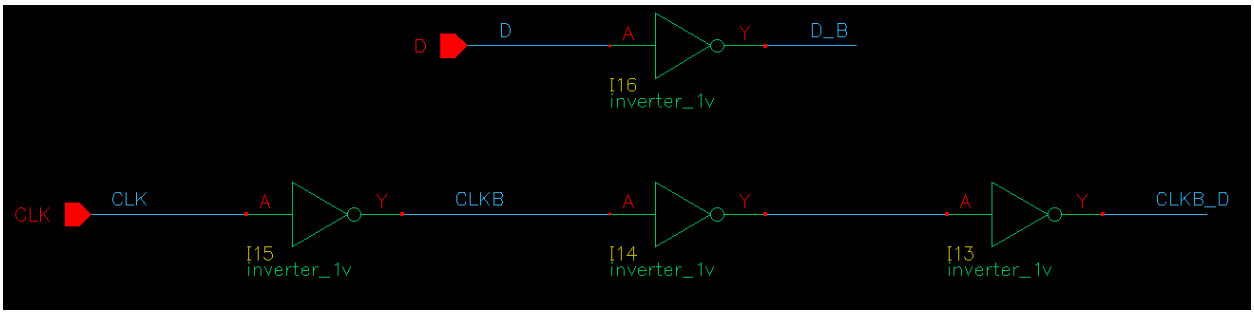

Figure 30. Clock pulse generator.

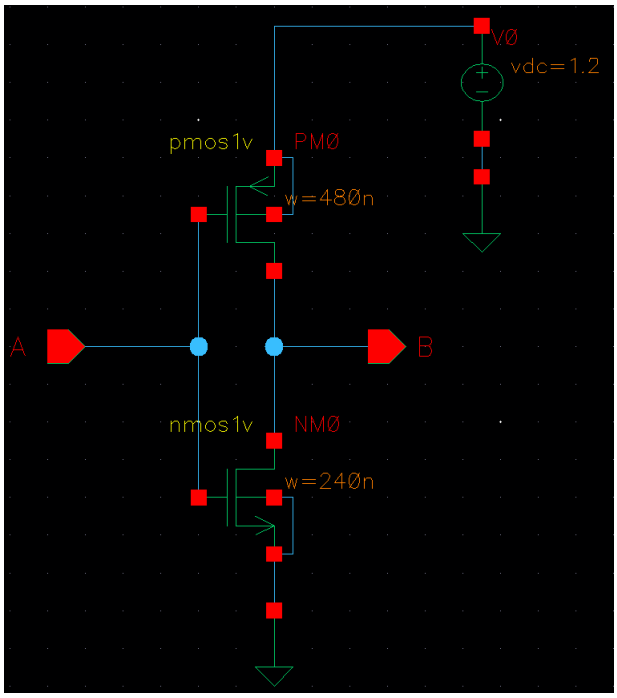

Figure 31. Inverter schematic used inside the PDFF-SE

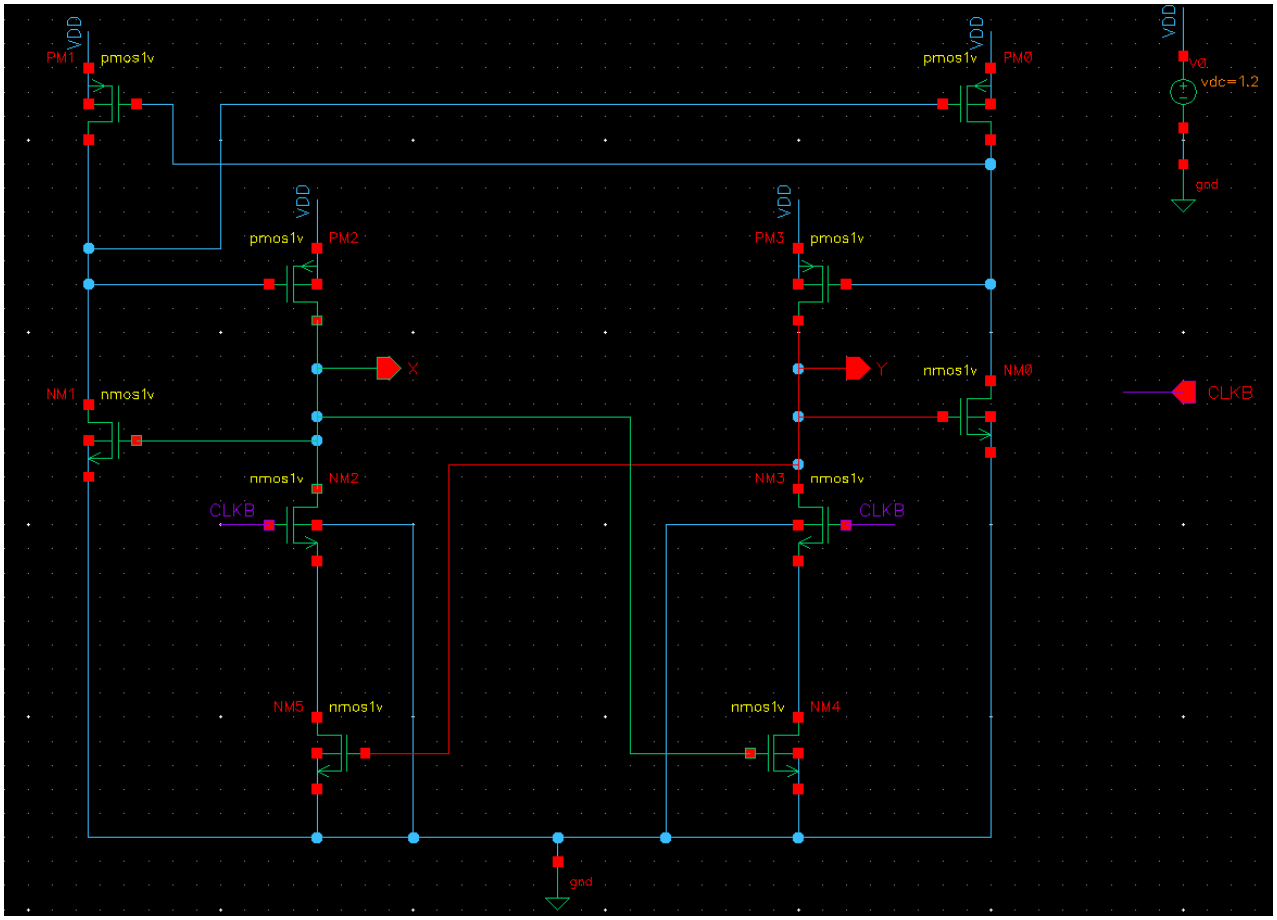

Figure 32. Quatro Cell Schematic

Transistor Sizing of PDFF-SE

Master and Slave Stages

Parameter	Master Stage	Slave Stage
NMOS Width	240nm	240nm
NMOS for Cross-Coupled Inverters Width	250nm	-
PMOS Width	4.8xNMOS = 1.2um	2xNMOS = 480nm
Length	100nm	100nm

Table 6. Master-Slave Transistor Sizing

Quatro Cell

Parameter	Value
Vdd	1.2V
NMOS Width	120nm
PMOS Width	120nm
Length	100nm

Table 7. Transistor Sizing of a Quatro Cell

Inverters

Parameter	Value
Vdd	1.2V
NMOS	240nm
PMOS	480nm
Length	100nm

Table 8. Transistor sizing of an Inverter

The PMOS size in the cross-coupling inverter in the master stage is made quite large to achieve better output results and metastability. The NMOS transistors are set to 250nm because they set the most accurate balance to the sizing of the transistors and the loads to achieve the most accurate output results (by far).

Note that increasing the transistor sizes will increase the Gm as well as the parasitic capacitances. The reason for choosing the cross-coupling inverter to vary in the master stage, is because the initial synchronization occurs there, and by keeping the slave stage to its minimum size (or close to minimum) we can minimize the capacitances at the critical nodes to satisfy the equation above to reduce the T.

However, to support the transistor sizes reasoning, in paper [1], it is mentioned that the master stage cross-coupling should be sized up while in the slave stage, it is only mentioned that the Quatro Cell must be set to its minimum sized transistors.

Output Simulations for PDFF-SE

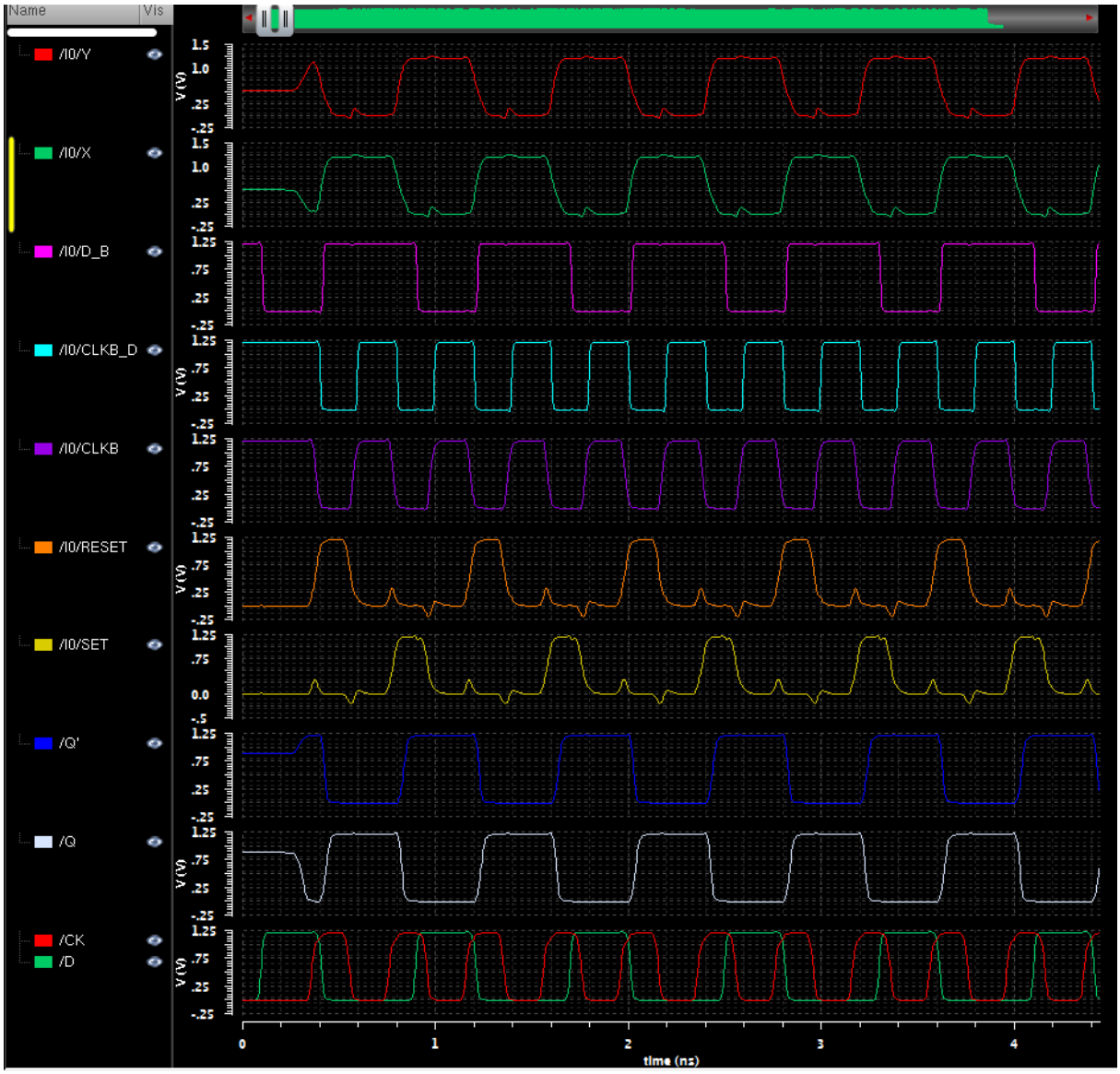

Figure 33. Transient waveform outputs of the PDFF-SE for setup time.

This is a setup simulation showing the data's (D) rising edge transitioning earlier than the clock (CK) in the beginning of the run time. Due to the period of the D that we have assigned in **Table 1**, the data signal will technically decrease in speed (frequency) because the period is 800.7 ps (increased in time.)

That caused the clock's rising edge to eventually catch up with the clock and furthermore become ahead of the data's rising edge and causing negative setup time (**figure 34**.) We can also see that the signals became smoother after the inverters have been used for the circuit's inputs and outputs.

Figure 34. Transient waveform outputs of the PDFF-SE for setup time, at the metastability region.

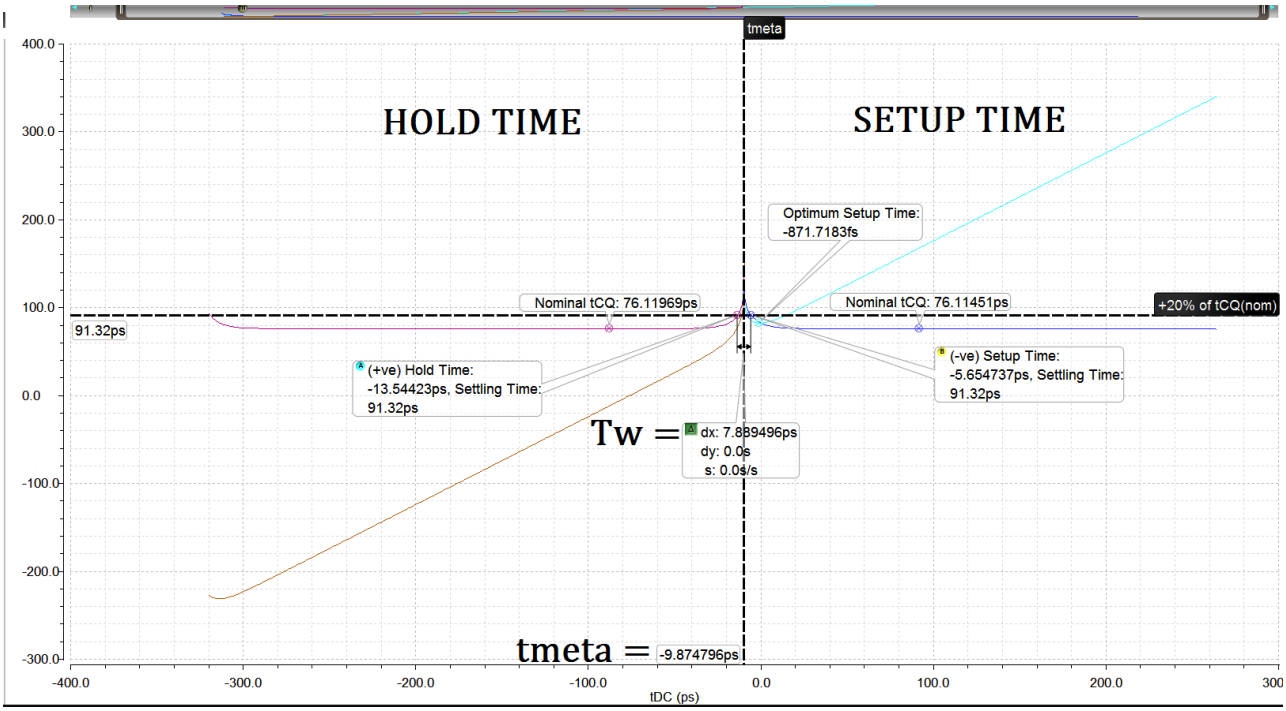

Figure 35. Plot of t_{CQ}, t_{DQ}, and t_{DC} for setup and hold time of the PDFF-SE.

Pre-Discharge Flip-Flop with Soft-Error Tolerance (PDFF-SE) Output of the Delays

Figure 34 shows the metastability window (t_w) between the setup and hold times. It shows that t_{meta} is -9.87 ps, and the T_w is 7.89ps for the PDFF-SE.

There has been some great improvement shown in the plot for the T_w in the PDFF-SE circuit compared to the conventional DFF's metastable window T_w.

The change in the T_w caused the T_0 to decrease greatly. Decreasing the T_0 value will cause the increase in the MTBF as shown in **Equation (8)**. As the window decreases, there is less of a chance that the circuit might enter the metastable state. Note that the curves in **Figure 35** have shifted to the left-hand side on the x-axis with respect to 0s (i.e. rising edge of the clock), showing a negative setup time behavior.

The metastable window T_w is measured from 20% above the nominal value of the t_{CQ}, and from that same point, we can measure the setup and hold times with respect to the clock edge.

Looking at the graph, assuming that the incoming data rising edge moves from right-to-left, both t_{setup} and t_{hold} occurred after the rising edge of the clock on the x-axis. Normally, the graph is read from left-to-right, but the delay function in Cadence caused the curves to be the way is being presented.

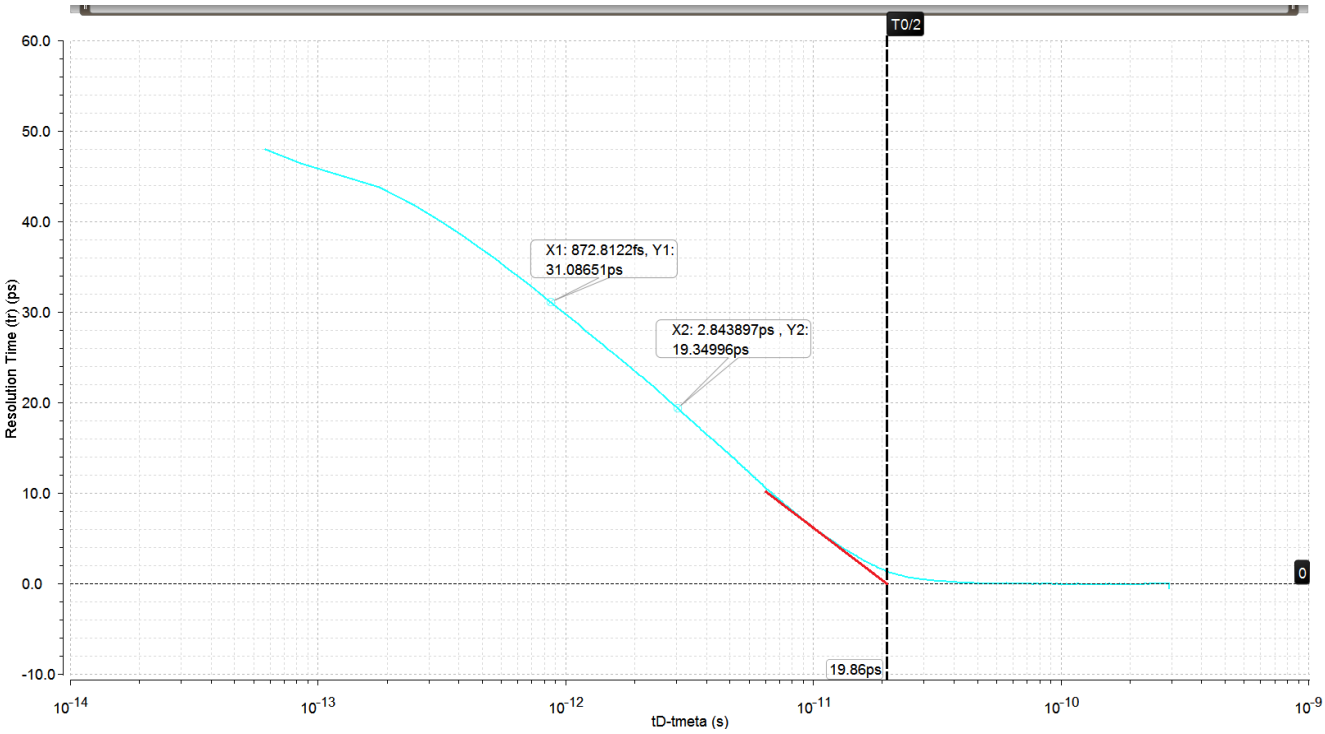

Figure 36. Plot describing the extrapolated curve for the PDFF-SE.

$$\tau = -\frac{(19.35p - 31.08p)}{\log_{10}(2.84f/872.81f)} = 3.6\ ps$$

$$y_3 = 31.08p + \frac{(19.35 - 31.08p)}{\log_{10}(2.84f/872.81f)} \cdot \log_{10}(x_3/872.81f) = 19.86\ ps$$

$$T_0 = 2 \times 19.86\ ps = 39.72\ ps$$

$$t_{CQ} + t_{setup\ 20\%} = 76.11\ p + (-5.65\ p) = 70.46\ ps$$

$$t_s = t_{CLK} - (t_{CQ} + t_{setup\ 20\%}) = 400p - 70.46p = 329.54\ ps$$

$$f_D = number\ of\ transitions\ of\ the\ data = 1.25GHz\ x\ 2 = 2.5GHz$$

$$MDP = \tau \cdot t_{DQ} = 3.6\ ps \cdot 70.46\ ps = 2.5\ x\ 10^{-22}\ s^2$$

$$MTBF = \frac{e^{329.54p/3.6p}}{2.5G \cdot 2.5G \cdot 39.72p} = 2.86\ x\ 10^{40}\ s = 7.94\ x\ 10^{36}\ hours$$

Parameter	PDFF
$\boldsymbol{\tau}$	3.6 ps
$\boldsymbol{T_0}$	39.72 ps
$\boldsymbol{T_s}$	329.54 ps
Nominal $\boldsymbol{T_{CQ}}$	76.11 ps
$\boldsymbol{T_{DQ}}$	70.46 ps
$\boldsymbol{T_{setup}}$	- 5.65 ps
$\boldsymbol{T_{hold}}$	13.54 ps
$\boldsymbol{T_w}$	7.88 ps
$\boldsymbol{t_{meta}}$	- 9.87 ps
MDP	2.5 x 10^{-22} s^2
MTBF	7.94 x 10^{36} hours

Table 9. Result from the PDFF-SE analysis.

Transistor Sizing Test

For the cross-coupled inverters, setting an initial size of wp = 1.44um and wn=240nm, the following steps describes how the resolution time constant and the asymptotic metastability window's width are extracted from the simulation results.

Following **Table 2**, the transient simulation settings for setup and hold time are shown in **Figure 37** and **Figure 38**, respectively.

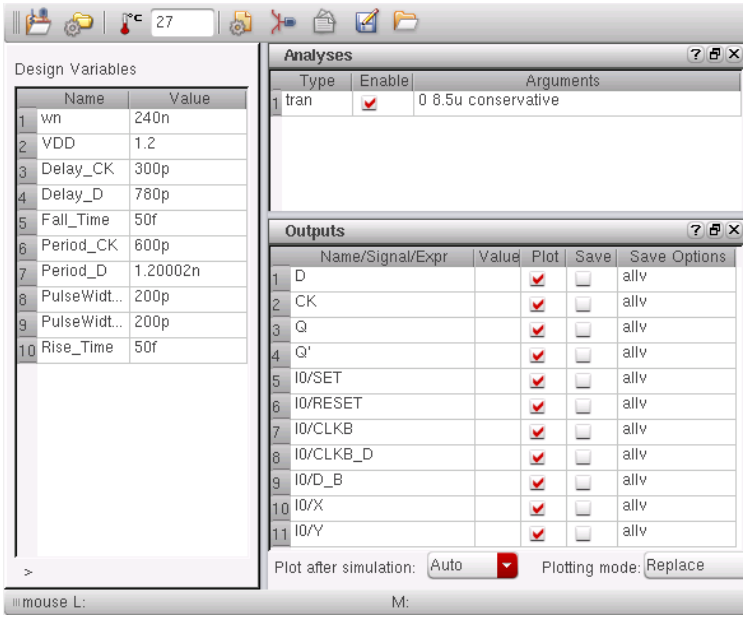

Figure 37. ADE settings for Setup Time of the PDFF-SE.

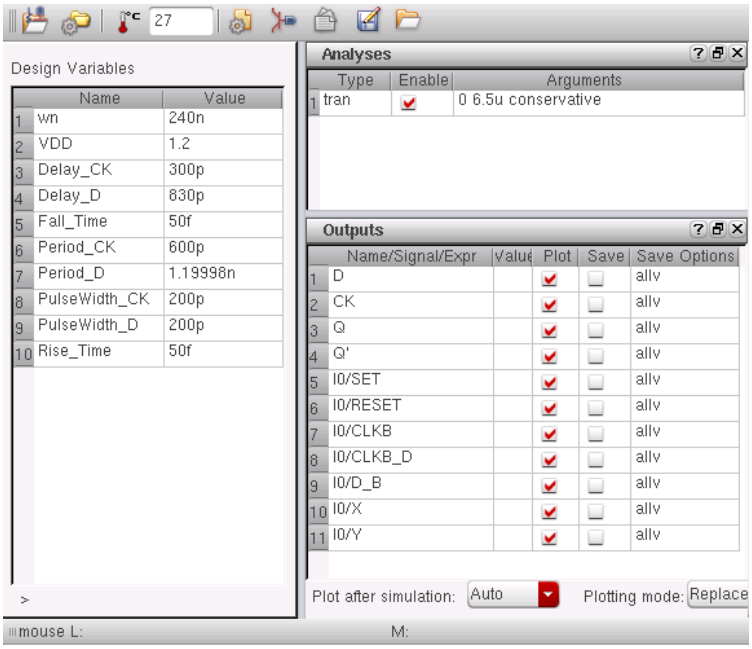

Figure 38. ADE settings for Hold Time of the PDFF-SE.

Figure 39 shows the simulation result for the inverter size described above, having found a value for t_{meta} of -9.246168ps for both setup and hold time.

Note that the device has a negative setup-time, and a positive hold-time, based on the location of t_{meta} with respect of the clock edge (located at 0 s on the x-axis).

Having a negative setup time, the data can still change its state after the clock edge has arrived, for a limited time.

Whereas for the positive hold time, the data must be stable after the setup time has being satisfied (after the clock edge has arrived), and cannot change after some time.

The values in the plot are shown negative for the hold time evaluation due to the nature of the *delay function* from Cadence.

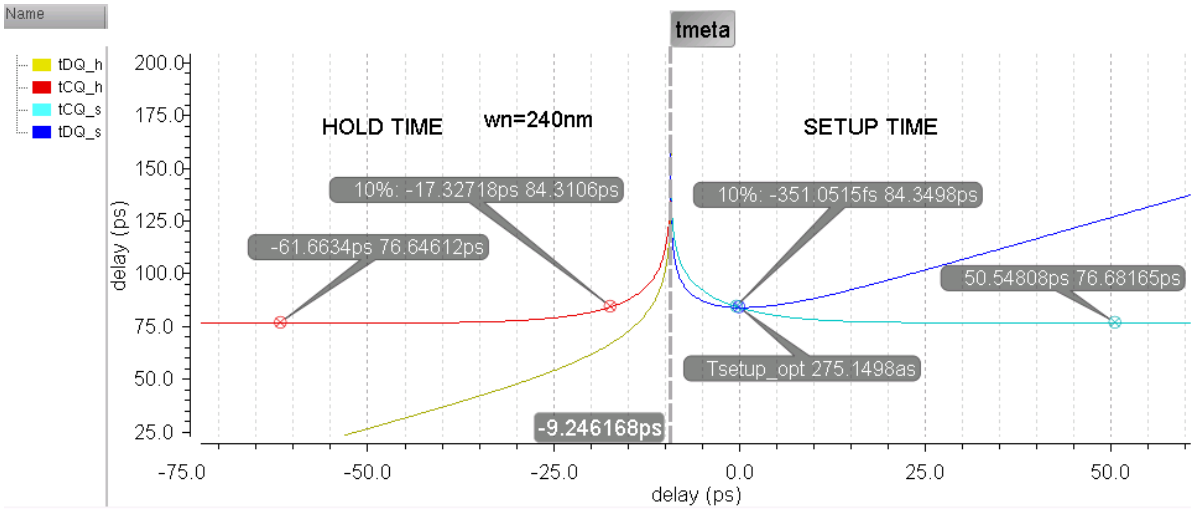

Figure 39. Simulation output for an inverter size of $wn = 240nm$ and $wp = 1.44\mu m$.

Figure 40 and **Figure 41** show the curve obtained following the method for extracting τ and T_0 constants from simulation, described previously.

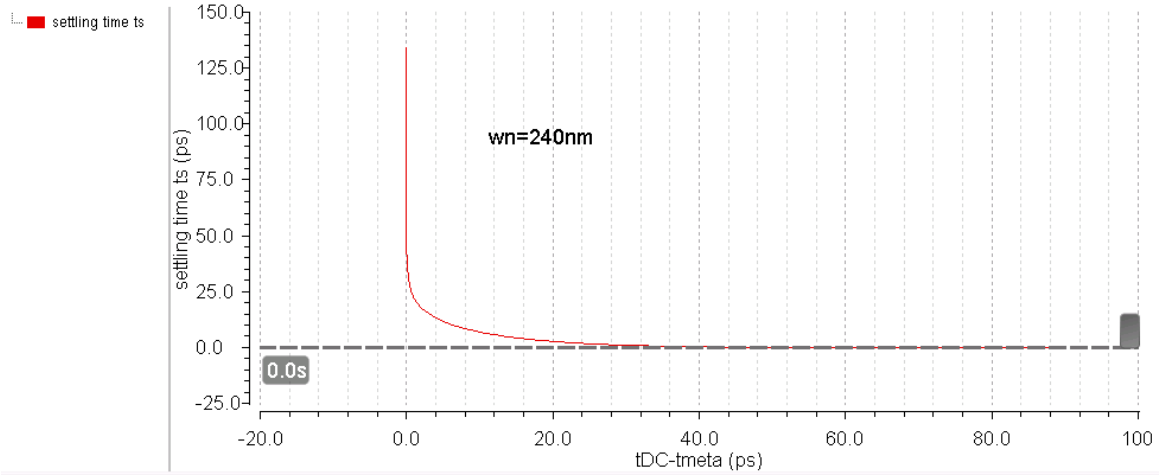

Figure 40. Plot of settling time t_s vs tD-tmeta taken from the t_{CQ} for Setup time.

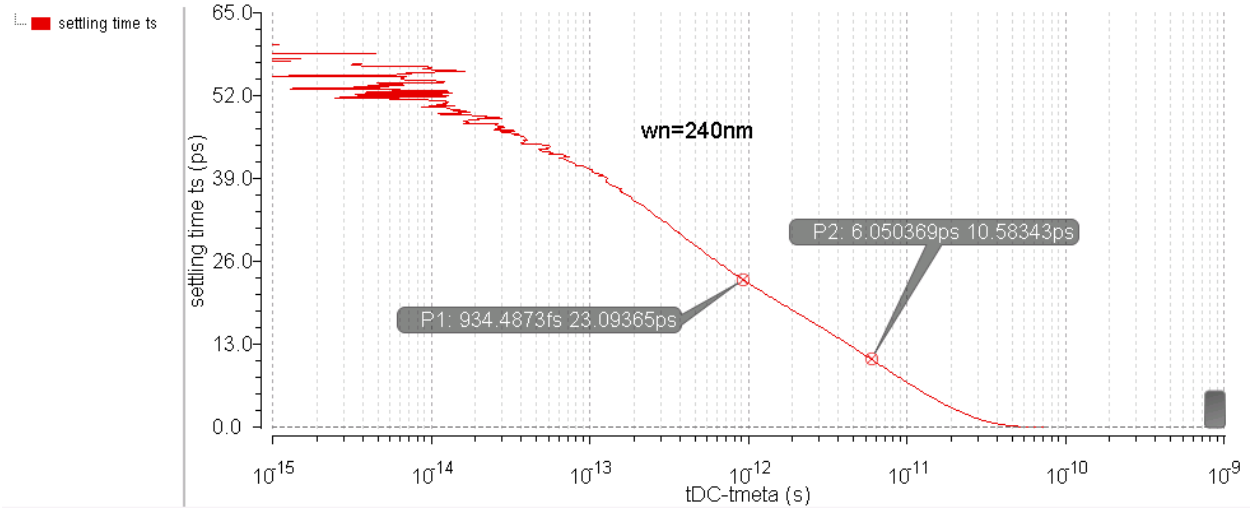

Figure 41. Plot of settling time t_s vs tD-tmeta in semilog, for wn=240nm.

Having the following points P1(934.4873 fs, 23.09365 ps), P2(6.050369 ps, 10.58343 ps), and P3(x3, 0 s), the next step is to solve for the x-axis intercept point x3:

$$y_3 = y_1 + \frac{(y_2 - y_1)}{\log_{10}(x_2/x_1)} \cdot \log_{10}(x_3/x_1)$$

$$\tau = -\frac{(y_2 - y_1)}{\log_{10}(x_2/x_1)} = -\frac{(10.58343 \times 10^{-12} - 23.09365 \times 10^{-12})s}{\log_{10}(6.050369 \times 10^{-12}/934.4873 \times 10^{-15})}$$

$$\tau = 1.54217 \times 10^{-11}s$$

$$x_3 = 2.93799 \times 10^{-11}s$$

$$T_0 = 2 \times x_3 = 2 \cdot 2.93799 \times 10^{-11} = 5.87598 \times 10^{-11} s$$

Exporting the data of the plot into a .csv file from Cadence, the extrapolated line can be plotted using a software like Matlab. The csv file contains the points (coordinates) that form the curve, and the pair of columns are renamed in Matlab as "tsX" and "tsY":

```
semilogx(tsX,tsY);
hold on
plot([1E-16,1E-10],[0,0])

plot( [934.4873E-15, 6.050369E-12, 2.93799E-11],...
      [23.09365E-12 , 10.58343E-12, 0   ]);
hold off
```

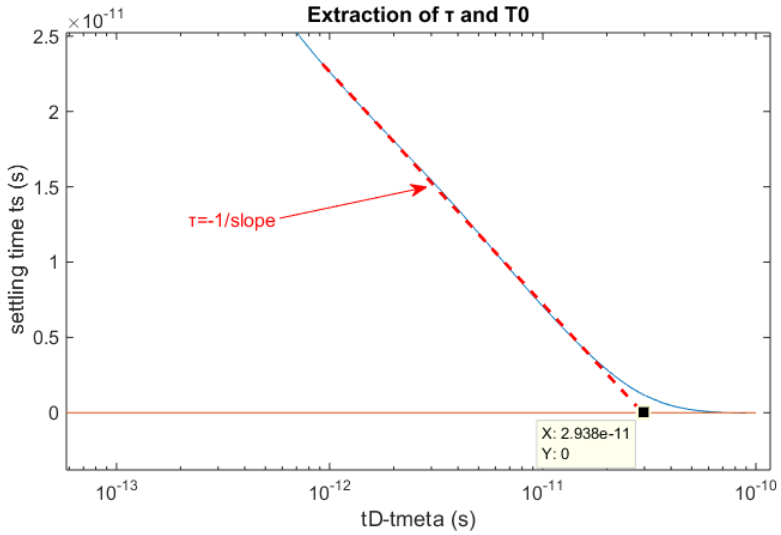

Figure 42. The red line shows the extrapolated curve up to $t_s = 0$, in semilog scale.

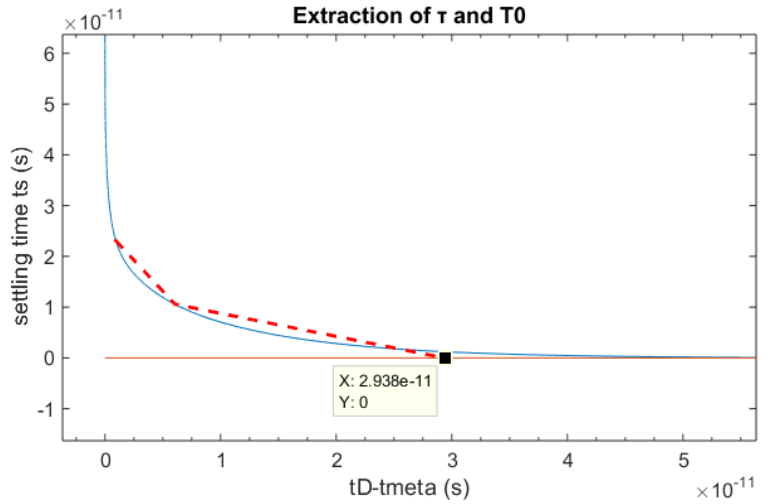

Figure 43. Same plot as the previous one, without semilog scale.

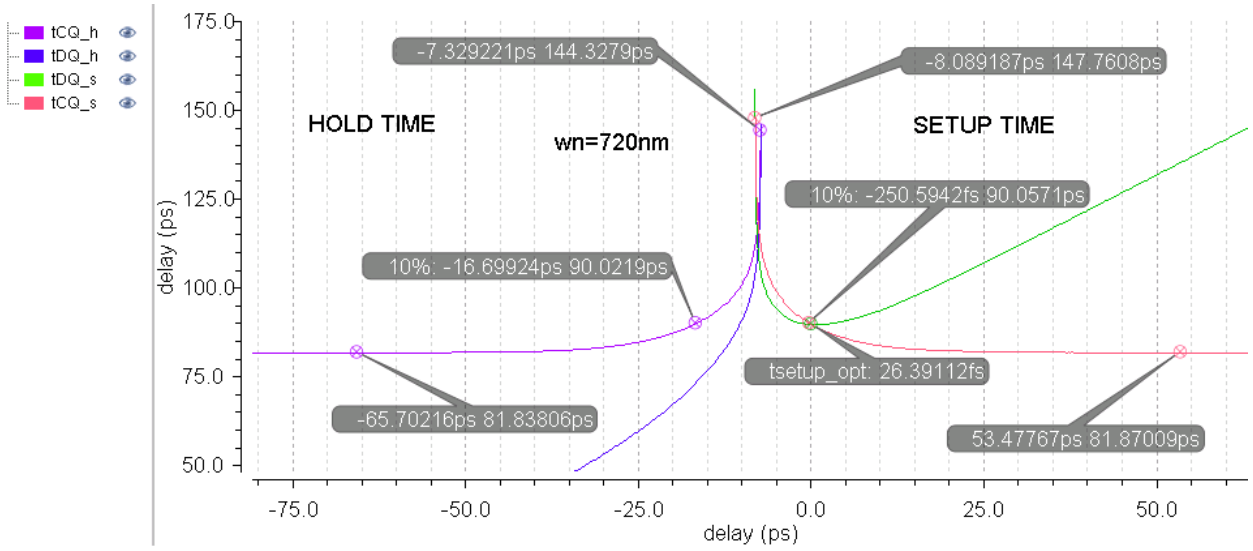

Figure 44. Simulation output for an inverter size of wn=720nm and wp=1.44µm.

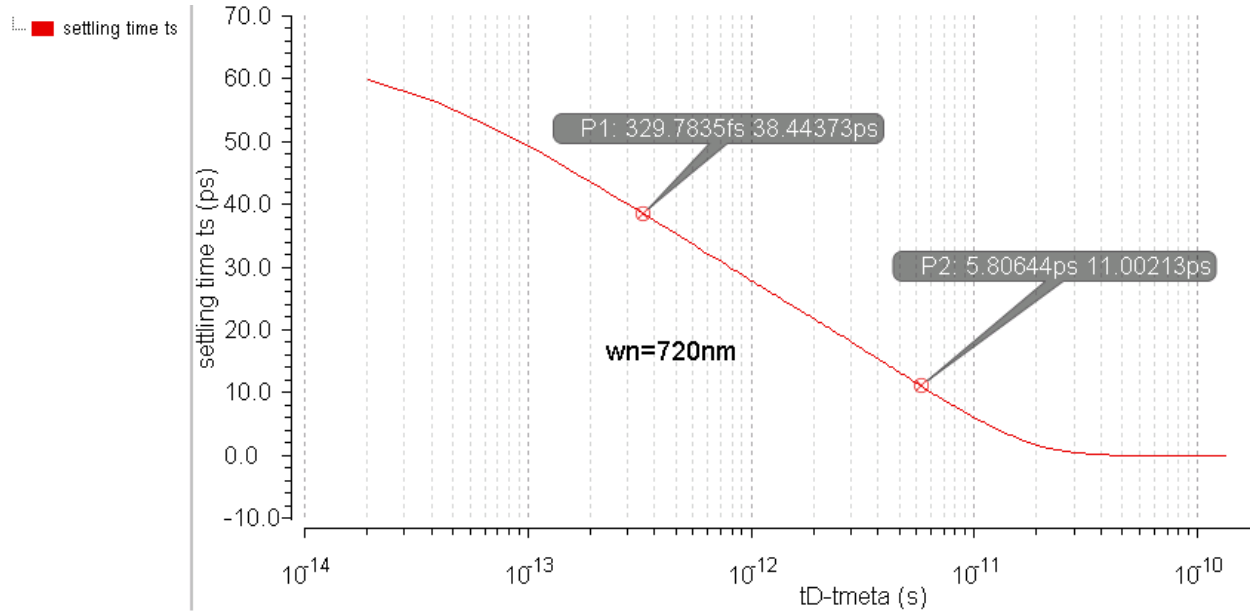

Figure 45. Plot of settling time t_s vs tD-tmeta in semilog, for wn=720nm.

For points P1(329.7835 fs, 38.44373 ps), P2(5.80644 ps, 11.00213 ps), and P3(x3, 0 s):

$$\tau = 2.20294 \times 10^{-11} s$$

$$x_3 = 1.83375 \times 10^{-11} s$$

$$T_0 = 2 \times x_3 = 2 \cdot 1.83375 \times 10^{-11} = 3.6675 \times 10^{-11} s$$

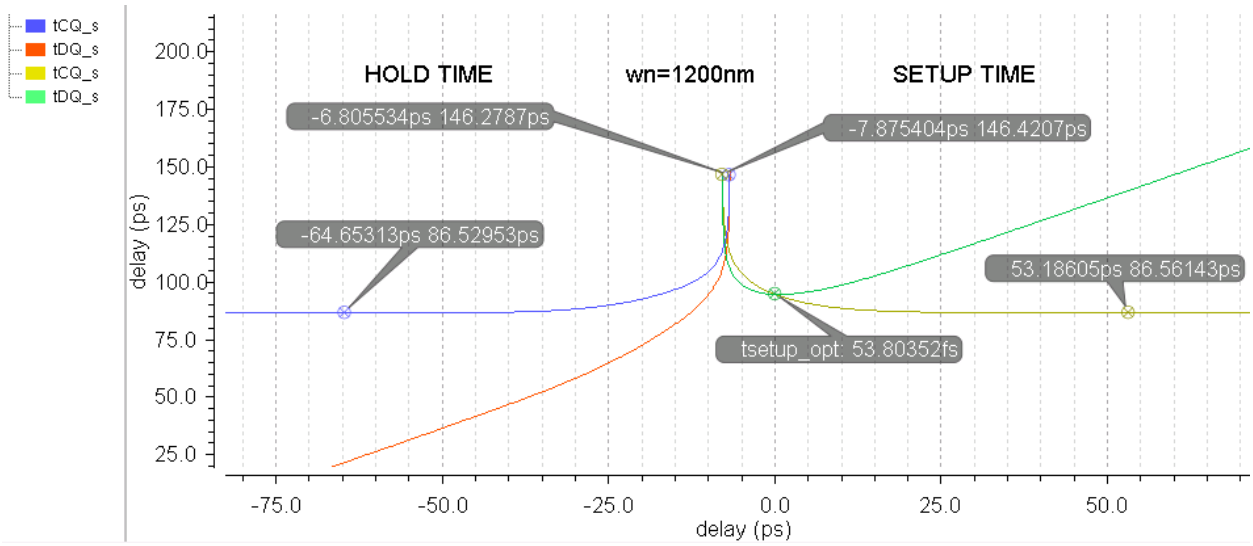

Figure 46. Simulation output for an inverter size of wn=1.2µm and wp=1.44µm.

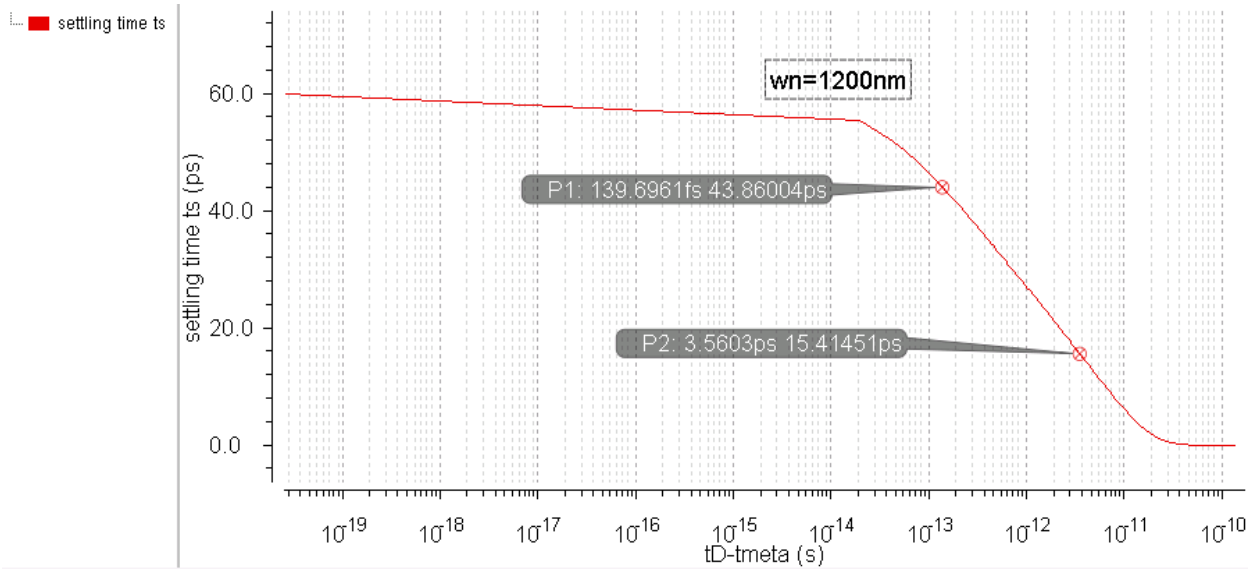

Figure 47. Plot of settling time t_s vs tD-tmeta in semilog, for wn=1200nm.

For points P1(139.6961 fs, 43.86004 ps), P2(3.5603 ps, 15.41451 ps), and P3(x3, 0 s):

$$\tau = 2.02272 \times 10^{-11} s$$

$$x_3 = 2.05852 \times 10^{-11} s$$

$$T_0 = 2 \times x_3 = 2 \cdot 2.05852 \times 10^{-11} = 4.11704 \times 10^{-11}$$

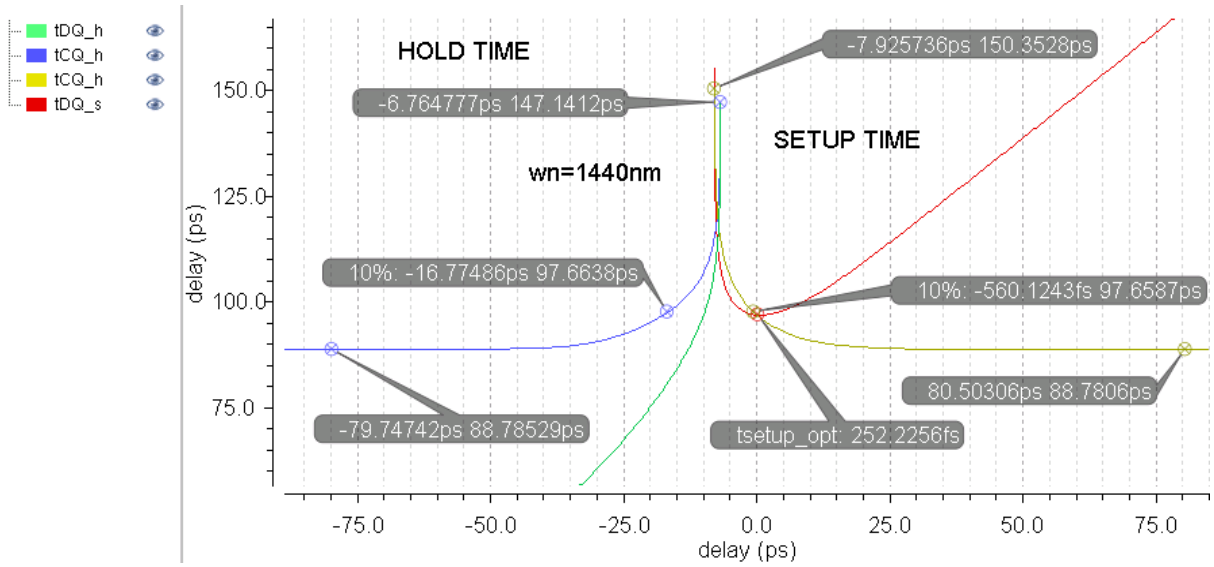

Figure 48. Simulation output for an inverter size of wn=1.44µm and wp=1.44µm.

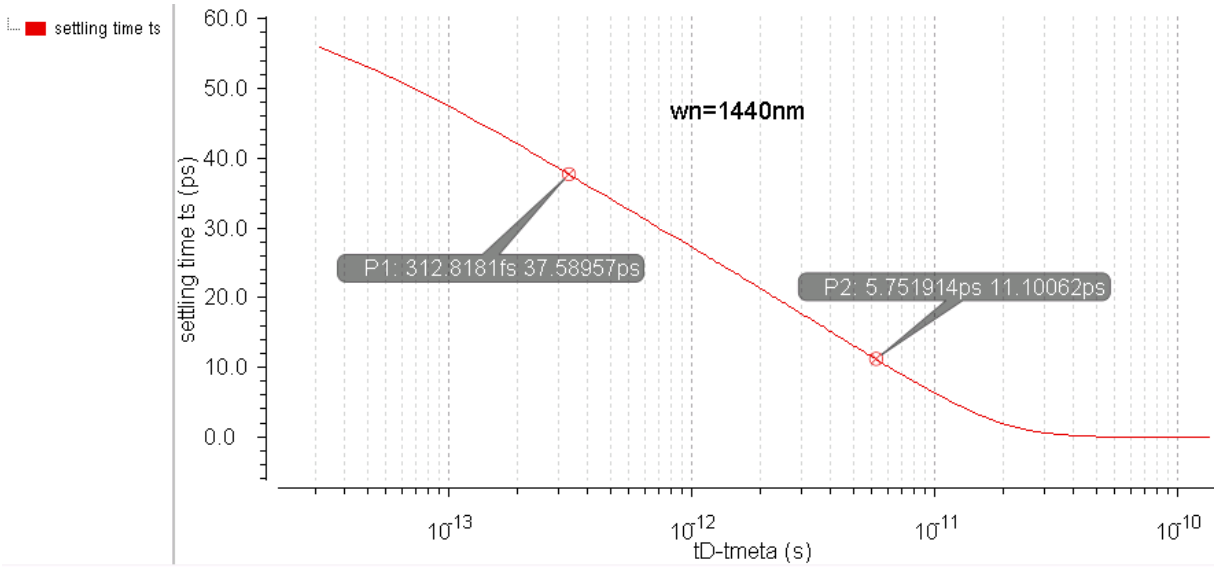

Figure 49. Plot of settling time t_s vs tD-tmeta in semilog, for wn=1440nm.

For points P1(312.8181 fs, 37.58957 ps), P2(5.751914 ps, 11.10062 ps), and P3(x3, 0 s):

$$\tau = 2.09478 \times 10^{-11} s$$

$$x_3 = 1.94863 \times 10^{-11} s$$

$$T_0 = 2 \times x_3 = 2 \cdot 1.94863 \times 10^{-11} = 3.89726 \times 10^{-11} s$$

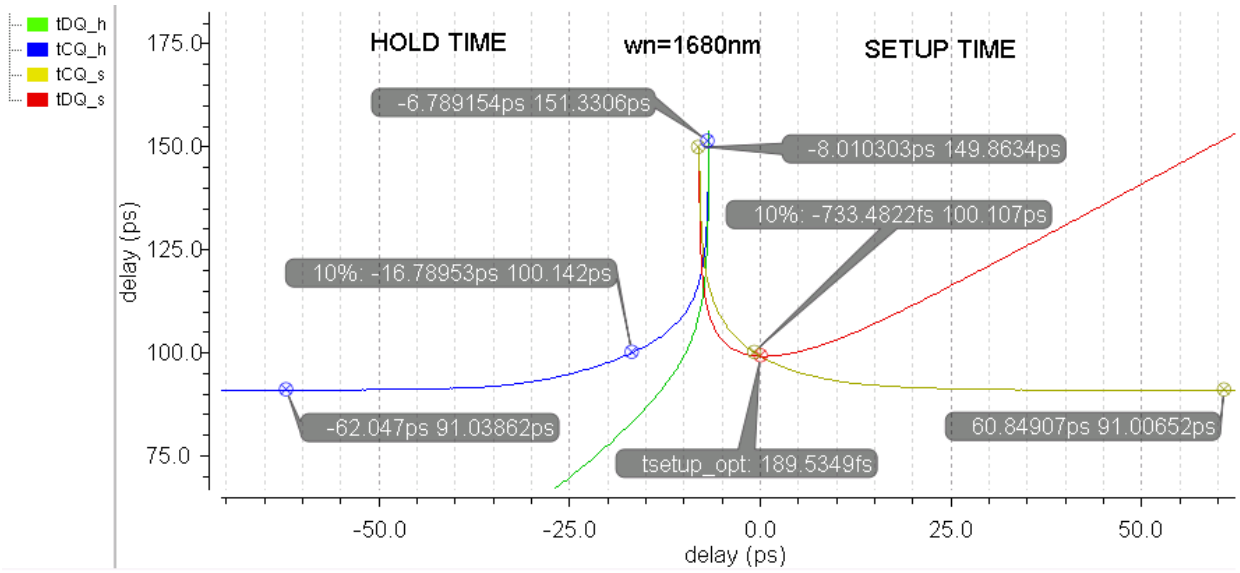

Figure 50. Simulation output for an inverter size of wn=1.68µm and wp=1.44µm.

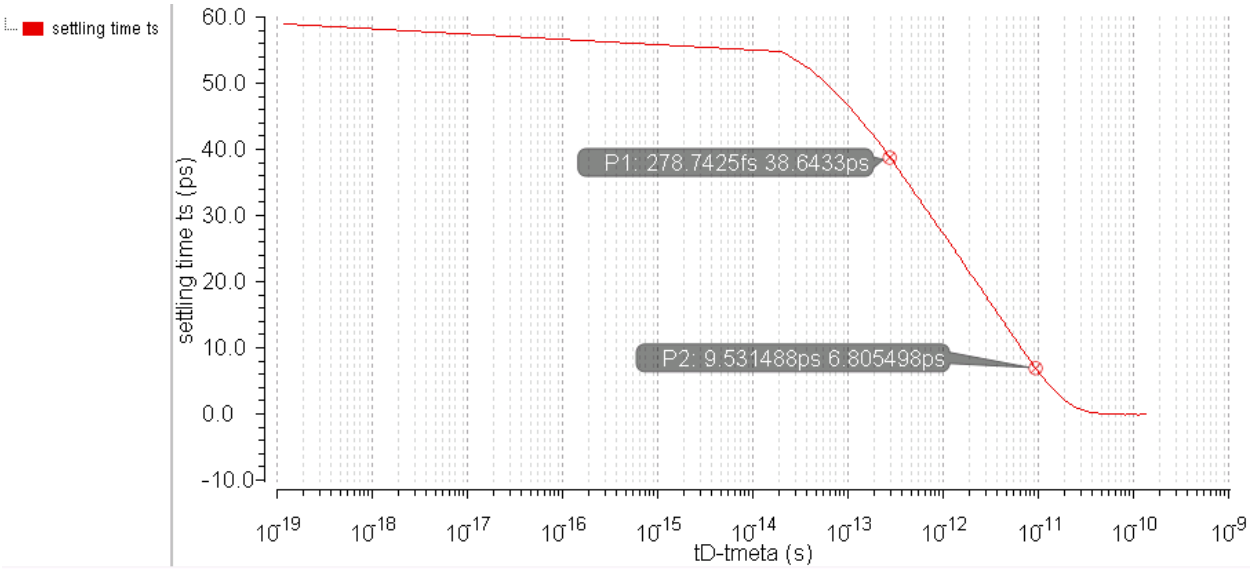

Figure 51. Plot of settling time t_s vs tD-tmeta in semilog, for wn=1680nm.

For points P1(278.7425 fs, 38.6433 ps), P2(9.531488 ps, 6.805498 ps), and P3(x3, 0 s):

$$\tau = 2.075553 \times 10^{-11} s$$

$$x_3 = 2.02793 \times 10^{-11} s$$

$$T_0 = 2 \times x_3 = 2 \cdot 2.02793 \times 10^{-11} = 4.05586 \times 10^{-11} s$$

wp	wn	τ	T_0	t_{meta} for t_{setup}	t_{meta} for t_{hold}
1440 nm	240 nm	15.4217 ps	58.7598 ps	-9.246168 ps	-9.246168 ps
1440 nm	720 nm	22.0294 ps	36.675 ps	-8.089187 ps	-7.329221 ps
1440 nm	1200 nm	20.2272 ps	41.1704 ps	-7.875404 ps	-6.805534 ps
1440 nm	1440 nm	20.9478 ps	38.9726 ps	-7.925736 ps	-6.764777 ps
1440 nm	1680 nm	20.75553 ps	40.5586 ps	-8.010303 ps	-6.789154 ps

Table 10. Comparison of different parameters for different values of wn of the inverters.

As seen in the plots, the t_{meta} for the negative setup time decreases when the wn increases, indicating that the data cannot arrive or change farther in time than before, after the clock edge has arrived.

On the other hand, the t_{meta} for the hold time increases, indicating that the hold time required is less when wn is increased.

$$t_s = t_{CLK} - t_{CQnom} - t_{setup\ 10\%}$$

$$t_{setup\ 10\%} \approx t_{setup\ optimum}$$

$$\delta(t_s) = \frac{T_0}{e^{t_s/\tau}} = T_0 \cdot e^{-t_s/\tau}$$

$$f_D = 2 \times \left(\frac{1}{1.2 \times 10^{-9} s}\right) = 1.667 \times 10^9\ Hz$$

$$f_{CLK} = \frac{1}{0.6 \times 10^{-9} s} = 1.667 \times 10^9\ Hz$$

$$MTBF = \frac{e^{t_s/\tau}}{f_D \cdot f_{CLK} \cdot T_0} = \frac{1}{f_D \cdot f_{CLK} \cdot \delta(t_s)}$$

$$t_{DQ} = t_{CQnom} + t_{setup}$$

$$MDP = \tau \cdot t_{DQ}$$

wn	t_{CQnom} for t_{setup}	$t_{setup\ 10\%}$	t_s	$\delta(t_s)$	$MTBF$
240 nm	76.68165 ps	0.275 fs	5.23318 E-10 s	1.07594 E-25	3344.58 s
720 nm	81.87009 ps	26.3911 fs	5.18104 E-10 s	2.2403E-21	0.160629 s
1200 nm	86.56143 ps	53.80352 fs	5.13385 E-10 s	3.90652 E-22	0.921168 s
1440 nm	88.7806 ps	252.2256 fs	5.10967 E-10 s	9.9375 E-22	0.362119 s
1680 nm	91.00652 ps	189.5349 fs	5.08804 E-10 s	9.15644 E-22	0.393009 s

Table 11. Calculation of MTBF for different NMOS transistor sizes in the cross-coupled inverter.

As seen in **Table 11**, the MTBF decreases for small values of t_s.

The settling time it depends on the speed of the clock and the value of the estimated setup time.

wn	τ	$t_{setup\ 10\%}$	t_{DQ}	MDP
240 nm	15.4217 ps	0.275 fs	7.66819 E-11 s	1.18257 E-21 s^2
720 nm	22.0294 ps	26.3911 fs	8.18965 E-11 s	1.80413 E-21 s^2
1200 nm	20.2272 ps	53.80352 fs	8.66152 E-11 s	1.75198 E-21 s^2
1440 nm	20.9478 ps	252.2256 fs	8.90328 E-11 s	1.86504 E-21 s^2
1680 nm	20.75553 ps	189.5349 fs	9.11961 E-11 s	1.89282 E-21 s^2

Table 12. Calculation of the MDP.

Conclusions

We've chosen the conventional D Flip-Flop (DFF) to find the characteristics of a flip-flop without any protection against single error upsets (SEU) nor any other reduction of the chances that a circuit may enter in a metastable state due to the delay of the data signal.

The parametric analysis settings shown in **Table 1** were used to perform the simulations, and the mathematical equations tell us the characteristics of the DFF at the "worst" case designs of a flip-flop.

The PDFF-SE circuit showed us that it improved the metastability of a FF by introducing transistors to pre-discharge the SET and RESET nodes in the critical path of the circuit. It can protect the critical nodes from false evaluation when the CLK is low.

Cross-coupled inverters are also introduced in the master stage to improve the MTBF of the dynamic logic circuit. The slave stage was modified to act as an XOR gate by introducing CLKB for PMOS and CLK for NMOS.

The output nodes X and Y are connected to the Quatro cell to increase the immunity of the circuit from alpha particles that can cause a Single Error Upset (SEU) events, and retain the signal at the output Q while maintaining high performance.

One of the main methods to increase the MTBF is by reducing the $\boldsymbol{\tau}$ and the T_0 in the PDFF-SE. As we can see in the **Table 13**, an improvement in these two parameters have significantly improved the MTBF compared to the conventional DFF. We can also see the influence of the negative setup time that has shown improvement in the performance.

As seen on **Table 11**, the MTBF is affected by several factors. One of them being the settling (resolution) time, in which for small calculated values, the MTBF decreases. By having flexible constraints, like the clock speed or the position of the setup time, we can improve the MTBF.

Parameter	Conventional DFF	PDFF
τ	33.8 ps	3.6 ps
T_0	58.72 ps	39.72 ps
T_s	306.9 ps	329.54 ps
Nominal T_{CQ}	69.79 ps	76.11 ps
T_{DQ}	93 ps	70.46 ps
T_{setup}	23.29 ps	- 5.65 ps
T_{hold}	- 5.12 ps	13.54 ps
T_w	18.16 ps	7.88 ps
t_{meta}	14.63 ps	- 9.87 ps
MDP	31 x 10^{-22} s^2	2.5 x 10^{-22} s^2
MTBF	84 hours	7.94 x 10^{36} hours

Table 13. Comparison Table between Conventional DFF and PDFF-SE

Future Work

Furthermore understanding of the trade-offs between the power, delay reduction, temperature and the voltage can be studied to better understand how it affects the metastability of the circuits.

Future researches may also be focused on modifying and improving the PDFF-SE circuit design in order to improve the metastability of a dynamic logic circuit and to improve the performance,

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