Assignment 4 ELEC5809 Winter 2015 Carleton University April 7, 2015

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Briefing

Using Cadence PLL circuit, apply a frequency step of amplitude as large as possible but still keeping the circuit locked.

Capture the shape of the step response and

1. Compare the observed time constant (10-90%) from that found in Assignment 4
2. Add a single reference period delay within the loop
3. Repeat the step response measurement
4. Compare results with no delay case

Compare you results with theoretical predictions you find in the literature.

Description

By adding one Input-Reference-frequency period in the Feedback path, the PLL will take more time to acquire lock condition.

Initially, this added delay will cause the period of the Feedback frequency to double its length with respect to the period of the Input Reference frequency.

The Phase Detector will detect the “large” phase difference, and will drive the Charge Pump for longer time, injecting more current into the Loop Filter.

This will generate a higher voltage value than what would normally be required without the delay, making the VCO to run faster (almost double the output frequency) in order to compensate for the large phase difference and to close the gap.

In theory, the Control Voltage waveform will display several cycle slips, until the phase difference is less than the phase margin of the Phase Detector, which has to be less than 2π.

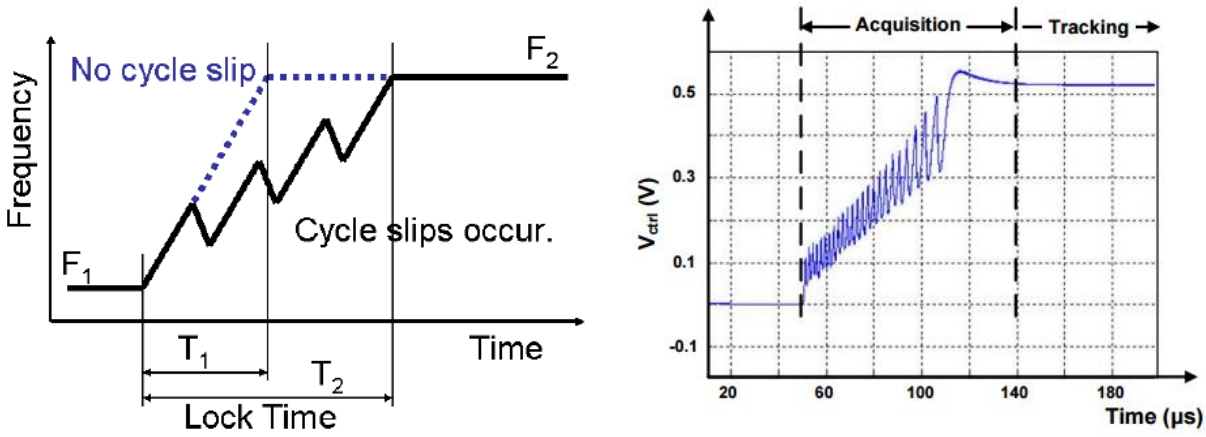

Figure 1. Example of how cycle slips degrade PLL locking time

Eventually, the control voltage will stabilize and the PLL will acquire lock.

But, since the VCO is running two times faster, then the Hold-in frequency range at which the PLL can acquire lock is reduced by half, starting from its minimum permissible Input Reference frequency.

About cycle slips

When an instantaneous phase error is presented to the phase detector, a cycle slipping can occur.

When the N divider value "changes", then the phase of the VCO signal divided by N will initially be incorrect in relation to the input reference signal (after the P divider).

If the Loop Bandwidth is very small (around 1%) relative to the frequency difference due to a step in frequency, then this phase error will accumulate faster than the PLL can correct for it.

By dividing the frequency difference by the instantaneous phase error presented to the phase detector, is possible to calculate how many cycles it would take the phase detector to cycle slip.

If this time is less than about half the rise time of the PLL, then cycle slipping is likely to occur.

The lock time is inversely proportional to the Loop Bandwidth, and the overshoot (undershoot) will remain exactly the same.

If the loop bandwidth is lowered, the VCO frequency responds more slowly to the error signal from the phase detector. The more slowly the VCO frequency responds, the larger the phase error is built up at the phase detector.

When a step frequency is large enough, the phase error at the phase detector will build up to 2π.

Characteristics of the 3rd order Type 2 PLL

Open loop:

$$G(s) = \frac{K_{VCO} \cdot K_{PD} \cdot F(s)}{sN}$$

Closed loop:

$$H(s) = \frac{G(s)}{1 + G(s)} = \frac{K_{VCO} \cdot K_{PD} \cdot F(s)}{sN + K_{VCO} \cdot K_{PD} \cdot F(s)}$$

Phase Error transfer function:

$$\phi_e(s) = (1 - H(s)) \cdot \phi_i(s)$$

$$\phi_e(s) = \frac{sN \cdot \phi_i(s)}{sN + K_{VCO} \cdot K_{PD} \cdot F(s)}$$

For an input frequency step:

$$\phi_i(s) = \frac{\Delta\omega}{s^2}$$

Then:

$$\phi_e(s) = \frac{sN \cdot \frac{\Delta\omega}{s^2}}{sN + K_{VCO} \cdot K_{PD} \cdot F(s)}$$

Applying the Laplace Transform Final Value theorem:

$$\lim_{t\to\infty} y(t) = \lim_{s\to 0} s \cdot Y(s)$$

$$\lim_{s\to 0} s \cdot \phi_e(s) = \frac{s^2 N \cdot \frac{\Delta\omega}{s^2}}{sN + K_{VCO} \cdot K_{PD} \cdot F(s)} = \frac{N \cdot \Delta\omega}{(0)N + K_{VCO} \cdot K_{PD} \cdot F(0)}$$

Filter transfer function

$$F(s) = \frac{sRC_1 + 1}{s^2 RC_2 C_1 + s(C_1 + C_2)}$$

$$F(0) = \frac{RC_1}{C_1 + C_2}$$

Phase error for a Frequency step response:

$$\phi_e = \frac{2\pi \cdot \Delta\omega \cdot N}{I_{cp} \cdot F(0) \cdot K_{VCO}} \quad where\ F(0) = \frac{RC_1}{C_1 + C_2}$$

$$C_1 = 44.0256\,pF \quad C_2 = 1.40019\,pF \quad R = 29.9959\,K\Omega$$

$$I_{cp} = 25\mu A$$

$$K_{PD} = \frac{I_{cp}}{2\pi} \quad A/rad$$

$$K_{PD} = 3.97887 \times 10^{-6} \quad \text{A/rad}$$

$$K_{VCO} = 453.30697 \times 10^6\ \frac{Hz}{Vs} \quad \rightarrow \quad K_{VCO} = 2.84821\ \times 10^9\ \frac{rad}{Vs}$$

$$N = 64$$

To calculate the 3dB loop bandwidth:

$$F(s) = \frac{sRC_1 + 1}{s^2RC_2C_1 + s(C_1 + C_2)} = \frac{sRC_1 + 1}{s(C_1 + C_2)(sRC_a + 1)}$$

$$C_a = \frac{C_1C_2}{C_1 + C_2} \qquad \omega_1 = \frac{1}{RC_1} \qquad \omega_{p3} = \frac{1}{RC_a}$$

Neglecting the capacitor C2, then:

$$C_1 = 44.0256\,pF \qquad R = 29.9959\,K\Omega \qquad K_{VCO} = 2.84821\ \times 10^9\ \frac{rad}{Vs}$$

$$\xi = \frac{R}{2}\sqrt{\frac{I_{cp} \cdot K_{VCO} \cdot C_1}{2\pi \cdot N}}$$

$$\xi = \frac{29.9959\,K\Omega}{2}\sqrt{\frac{25\mu A \cdot 2.84821\ \times 10^9\ \frac{rad}{Vs} \cdot 44.0256\,pF}{2\pi \cdot 64}} = 1.32442$$

Natural Frequency:

$$\omega_n = \sqrt{\frac{I_{cp} \cdot K_{VCO}}{2\pi \cdot N \cdot C_1}}$$

$$\omega_n = \sqrt{\frac{25\mu A \cdot 2.84821 \times 10^9 \frac{rad}{Vs}}{2\pi \cdot 64 \cdot 44.0256\, pF}} = \quad 2.0055 \times 10^6 \ rad/s$$

$$f_n = \frac{\omega_n}{2\pi} = 319.186\, KHz$$

Loop Filter Bandwidth frequency:

$$\omega_{3dB} = \omega_n \sqrt{1 + 2\xi^2 + \sqrt{4\xi^4 + 4\xi^2 + 2}}$$

$$\omega_{3dB} = 2.0055 \times 10^6 \ rad/s \sqrt{1 + 2(1.32442)^2 + \sqrt{4(1.32442)^4 + 4(1.32442)^2 + 2}}$$

$$\omega_{3dB} = 6.05846 \times 10^6\, rad/s$$

$$f_{3dB} = \frac{\omega_{3dB}}{2\pi} = 964.233\, KHz$$

Frequency at zero in s-domain:

$$\omega_z = \frac{1}{RC_1} = \frac{1}{(29.9959\, K\Omega)(44.0256\, pF)} = \quad 757.2387\, Krad/s$$

$$f_z = \frac{\omega_z}{2\pi} = 120.518\, KHz$$

If the second capacitor is considered:

$$C_a = \frac{C_1 C_2}{C_1 + C_2} = \frac{(44.0256\, pF)(1.40019\, pF)}{44.0256\, pF + 1.40019\, pF} = 1.357\, pF$$

$$\omega_p = \frac{1}{RC_a} = \frac{1}{(29.9959\, K\Omega)(1.357\, pF)} = 2.45716 \times 10^7 rad/s$$

$$f_p = \frac{\omega_p}{2\pi} = 3.91069\, MHz$$

Crossover frequency (0 Gain):

$$\omega_c = \omega_z \sqrt{\frac{C_1}{C_2} + 1}$$

$$\omega_c = (757.2387\ Krad/s) \sqrt{\frac{44.0256\ pF}{1.40019\ pF} + 1}$$

$$\omega_c = 757.239\ Krad/s$$

The phase margin degradation due to the third pole:

$$\phi_m(\omega_c) = \tan^{-1}\left(\frac{\omega_c}{\omega_z}\right) + \tan^{-1}\left(\frac{\omega_c}{\omega_p}\right)$$

Solving for the loop filter after applying the final value theorem:

$$F(0) = \frac{RC_1}{C_1 + C_2} = \frac{(29.9959\ K\Omega)(44.0256\ pF)}{44.0256\ pF + 1.40019\ pF} = 29071.3\ \Omega$$

This indicates that, in time domain, the PLL can track the step change of the input frequency.

The DC Loop Gain is then:

$$K = K_{VCO} \cdot K_{PD} \cdot F(0)$$

$$K = \left(2.84821\ \times 10^9\ \frac{rad}{Vs}\right) \cdot \left(\frac{25\mu A}{2\pi}\right) \cdot (29071.3\ \Omega)$$

$$K = 3.2516 \times 10^9\ rad/s$$

$$K = 517.5\ MHz$$

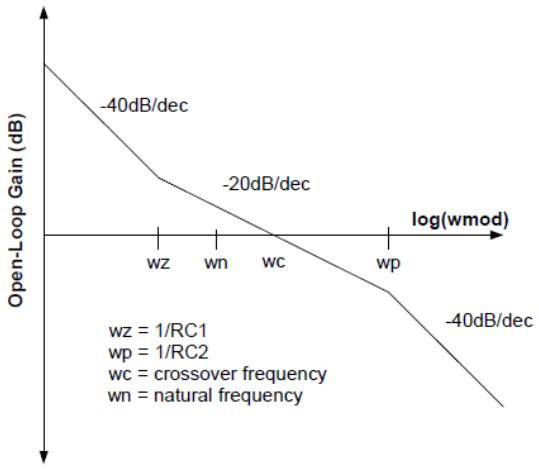

Figure 2. Open Loop Gain characteristic plot

$$\omega_o - K \leq \omega_{VCO} \leq \omega_o + K$$

$$\omega_{out} = \omega_o + K_{VCO} \cdot V_{control}$$

$$V_{control} = \frac{\phi_e \cdot I_{cp}}{2\pi} \cdot F(s)$$

$$V_{control} = \frac{\Delta\omega \cdot N}{K_{VCO}}$$

$$\phi_e = \frac{2\pi \cdot \Delta\omega \cdot N}{I_{cp} \cdot F(0) \cdot K_{VCO}} = \frac{2\pi \cdot \Delta\omega \cdot 64}{(25\mu A) \cdot (29071.3\ \Omega) \cdot \left(2.84821 \times 10^9 \frac{rad}{Vs}\right)}$$

$$\phi_e = \Delta\omega \cdot 1.9426 \times 10^{-7} rad \cdot s$$

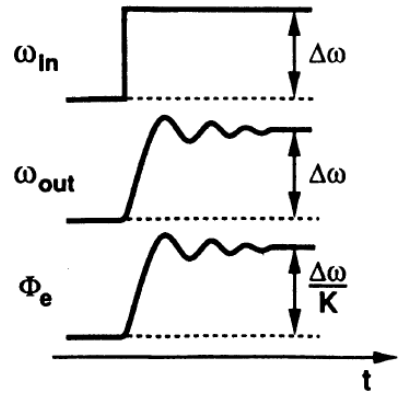

Figure 3. Example of Input Frequency Step response

The Hold-in frequency range:

$$\Delta\omega_{hold-in} = \frac{K}{N} \cdot \phi_{e,max} \quad where\ \phi_{e,max} \leq 2\pi$$

The Lock-in frequency range:

$$\Delta\omega_{lock-in} \approx 2\xi\omega_n$$

When applying the delay of one input reference period in the feedback path, the frequency division turns to be N = 128.

PLL Parameters	$\boldsymbol{N = 64}$	$\boldsymbol{N = 128}$
ξ	1.32422	0.936366
ω_n	2.0055 M rad/s	1.41811 M rad/s
f_n	319.186 KHz	225.698 KHz
ω_{3dB}	6.05846 M rad/s	3.38066 M rad/s
f_{3dB}	964.233 KHz	538.049 KHz
K	3.2516 G rad/s = 517.5 MHz	
K/N	50.8063 M rad/s	25.4031M rad/s
K/N	8.086 MHz	4.04303 MHz
$\Delta\omega_{hold-in}$	319.225 M rad/s	159.613 M rad/s
$\Delta f_{hold-in}$	50.8063 MHz	25.4031 MHz
$\Delta\omega_{lock-in}$	5.31145 M rad/s	2.65574 M rad/s
$\Delta f_{lock-in}$	845.343 KHz	422.674 KHz

Table 1. PLL characteristic parameters, seen after the input frequency divider P=5.

Procedure

The following is a Parametric Analysis for an input reference frequency from 20 MHz to 50 MHz, with step frequencies of 2.5 MHz to see where it starts losing lock.

This is done without the added delay in the feedback path.

Based on the Lock-in frequency range and the input prescaler P=5, the maximum input frequency has to be:

$$f_{step\ input} = \Delta f_{lock-in} \cdot P = 845.343\ \text{KHz} \cdot 5 = 4.22672\ \text{MHz}$$

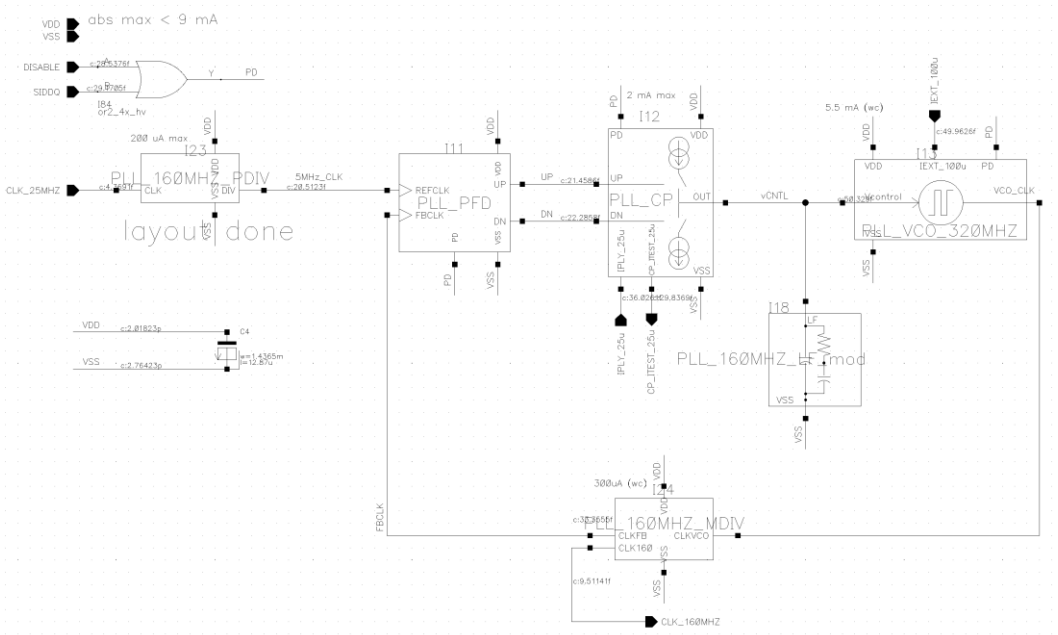

Figure 4. PLL circuit schematic with no delay added in the feedback path.

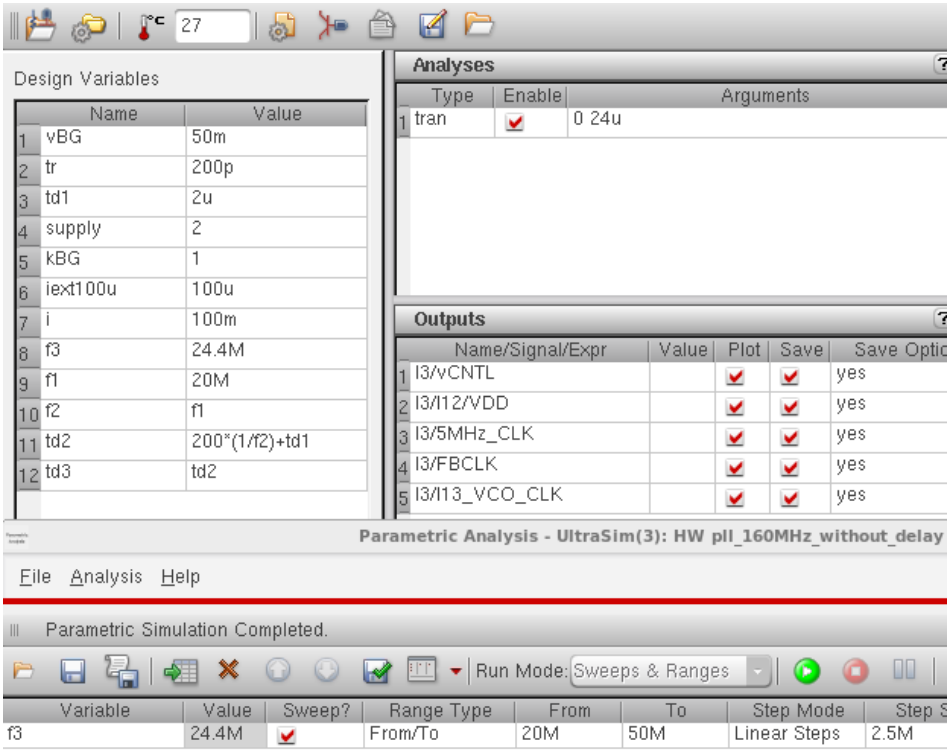

Figure 5. ADE settings for the PLL with no delay added in the feedback path.

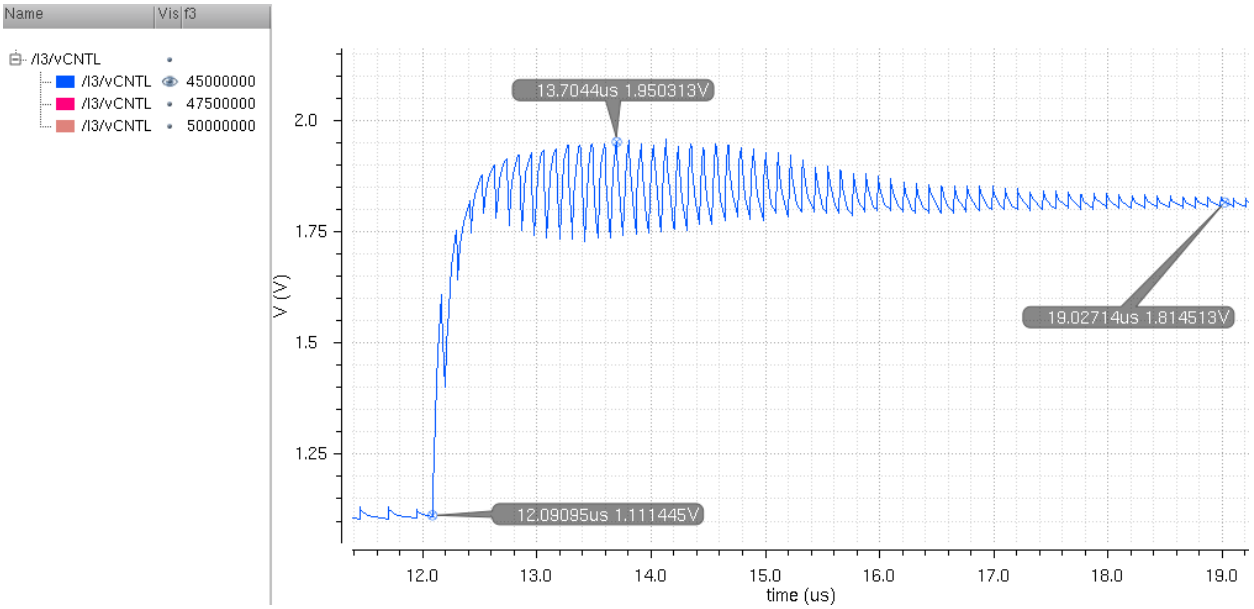

Figure 6. Control Voltage waveform during the frequency step from 20MHz to 45MHz.

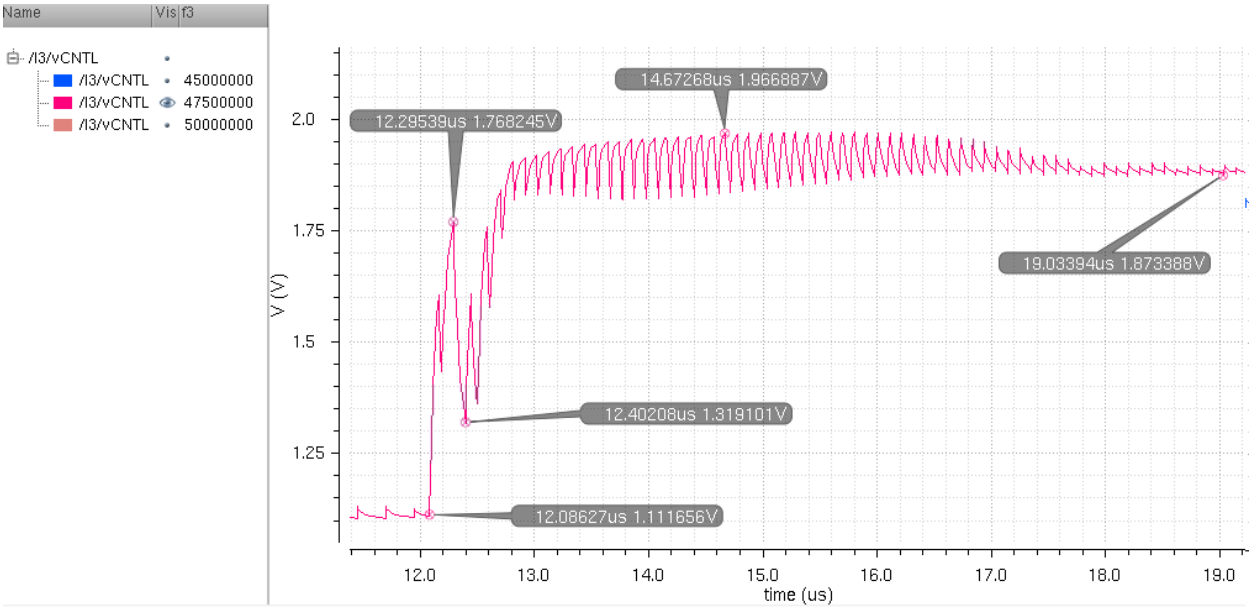

Figure 7. Control Voltage waveform during the frequency step from 20MHz to 47.5MHz.

Notice the cycle slip in **Figure 7** between 12.29µs and 12.4µs. To prove this fact:

$$\Delta f \cdot P = (47.5\ \text{MHz} - 20\text{MHz}) \cdot 5 = 5.5\ \text{MHz}$$

This step in frequency is larger than $\Delta f_{lock-in}$ of 4.2267 MHz. So it cycle-slips.

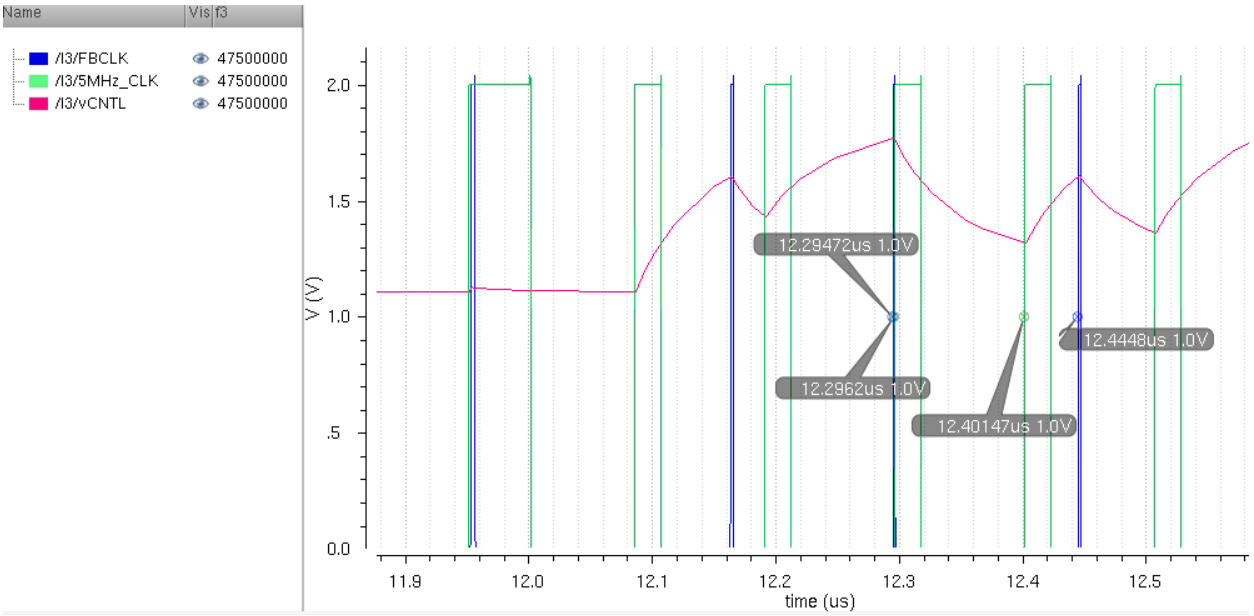

Figure 8. Plot of the Feedback waveform, the input frequency after the prescaler (5MHz_CLK) and the VCNTL with the cycle slip.

For the assignment purposes, the step frequency chosen is from 20MHz to 40MHz as seen in **Figure 9**.

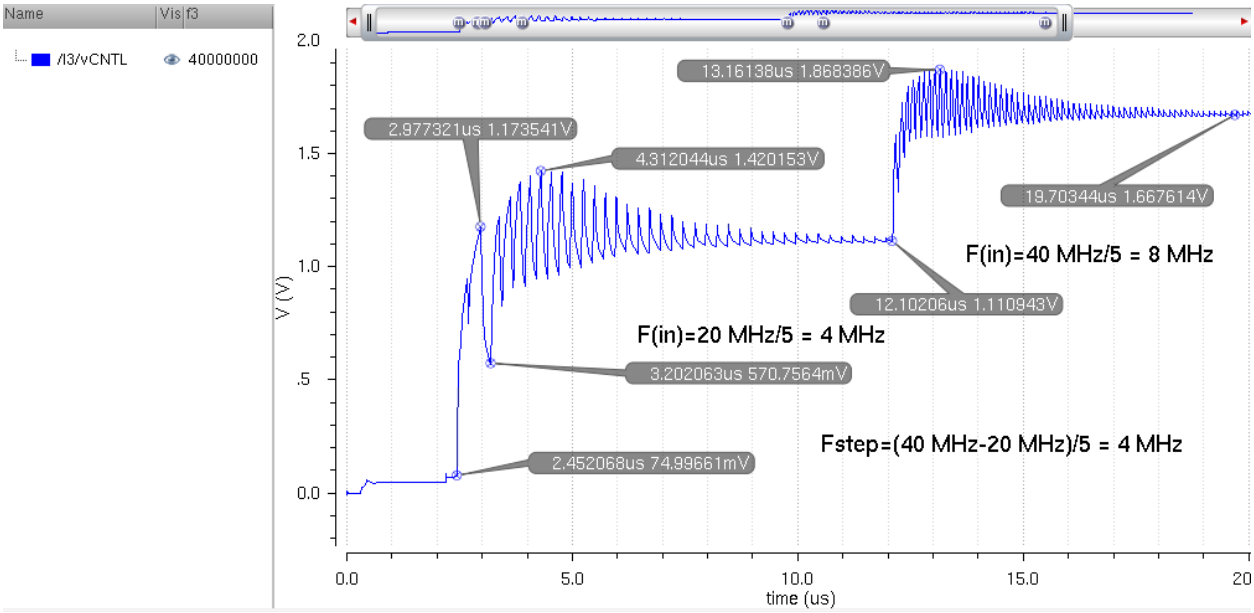

Figure 9. Control Voltage for a step frequency of 4MHz (after the input prescaler).

The delay is applied via a Flip-Flop configured as a toggle switch. Together with the N-frequency divider, the frequency division increases from 64 to 128, effectively adding one whole input reference frequency period into the feedback path. The FF is a copy from one of the same located inside the N-divider circuit.

The toggle is attached to an inverting multiplexer and a NAND gate, for a non-inverting transition, and the multiplexer is activated at time 11.45µs using a pulse voltage source.

Based on the Lock-in frequency range and the input prescaler P, the maximum input frequency has to be:

$$f_{step\ input} = \Delta f_{lock-in} \cdot P = 422.674\ \text{KHz} \cdot 5 = 2.11337\ \text{MHz}$$

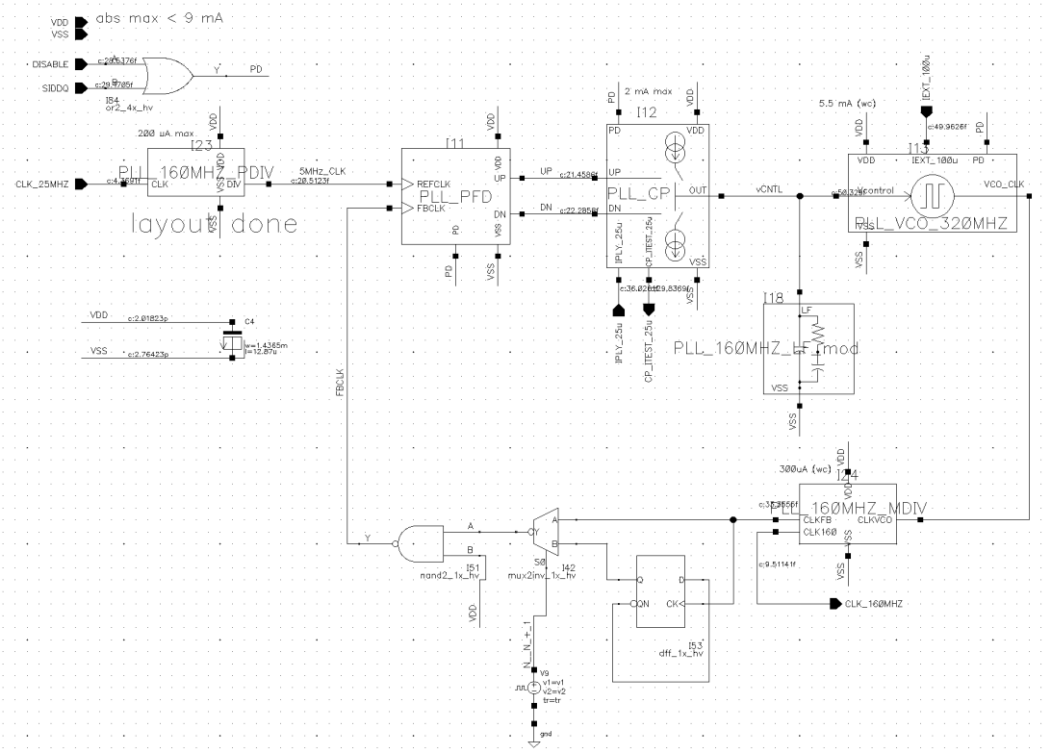

Figure 10. PLL circuit schematic with the delay added in the feedback path.

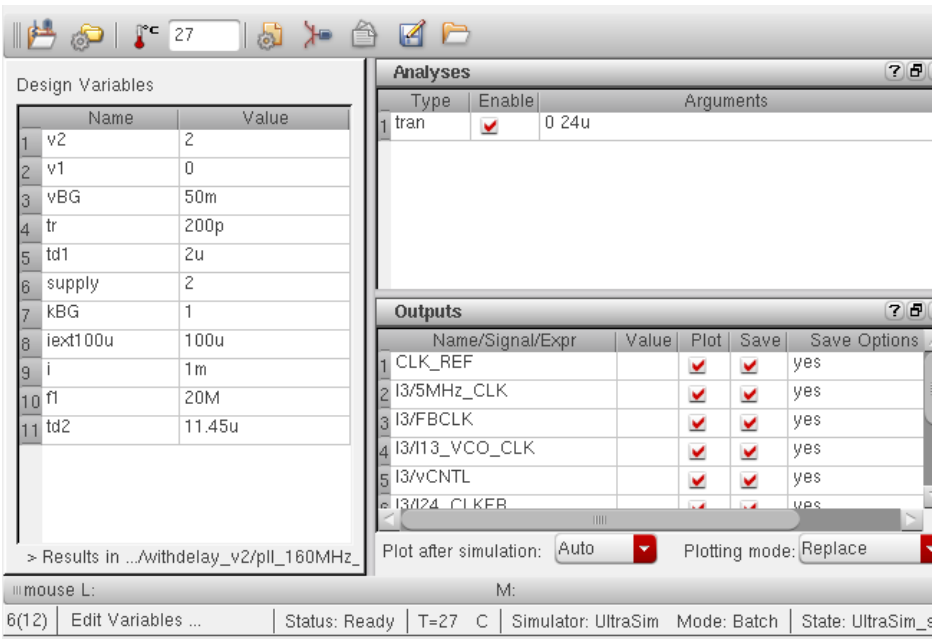

Figure 11. ADE settings for the PLL with the delay added in the feedback path.

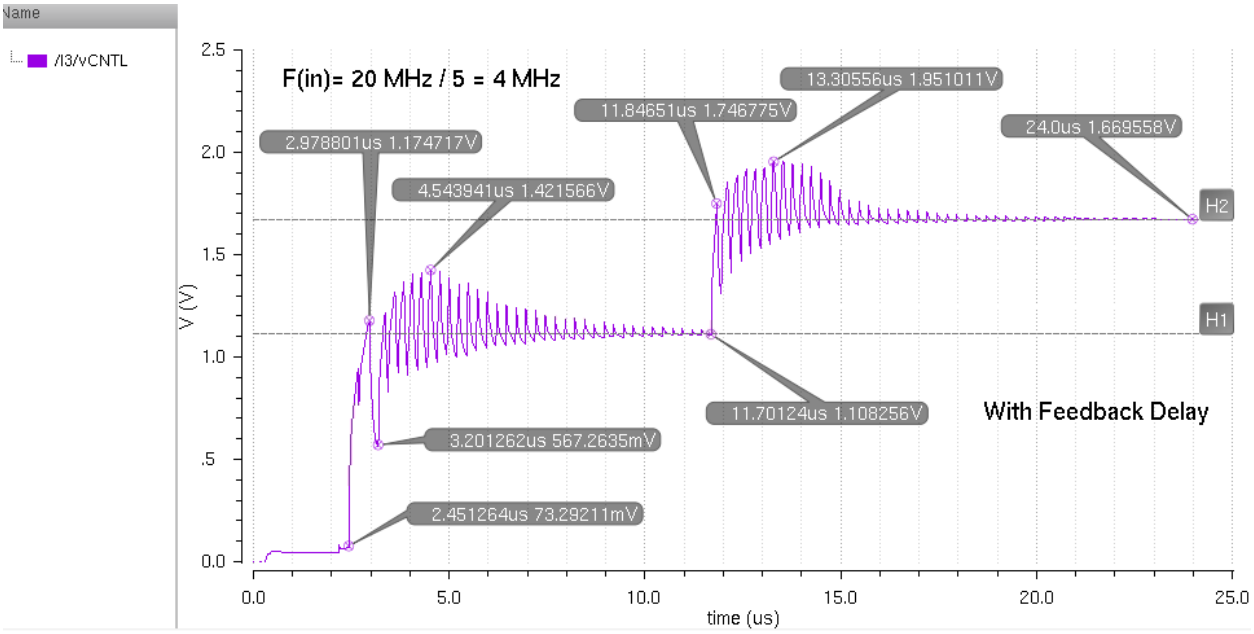

Figure 12. Control Voltage for an input of 20MHz (4 MHz after the prescaler) and with the delay applied in the Feedback path.

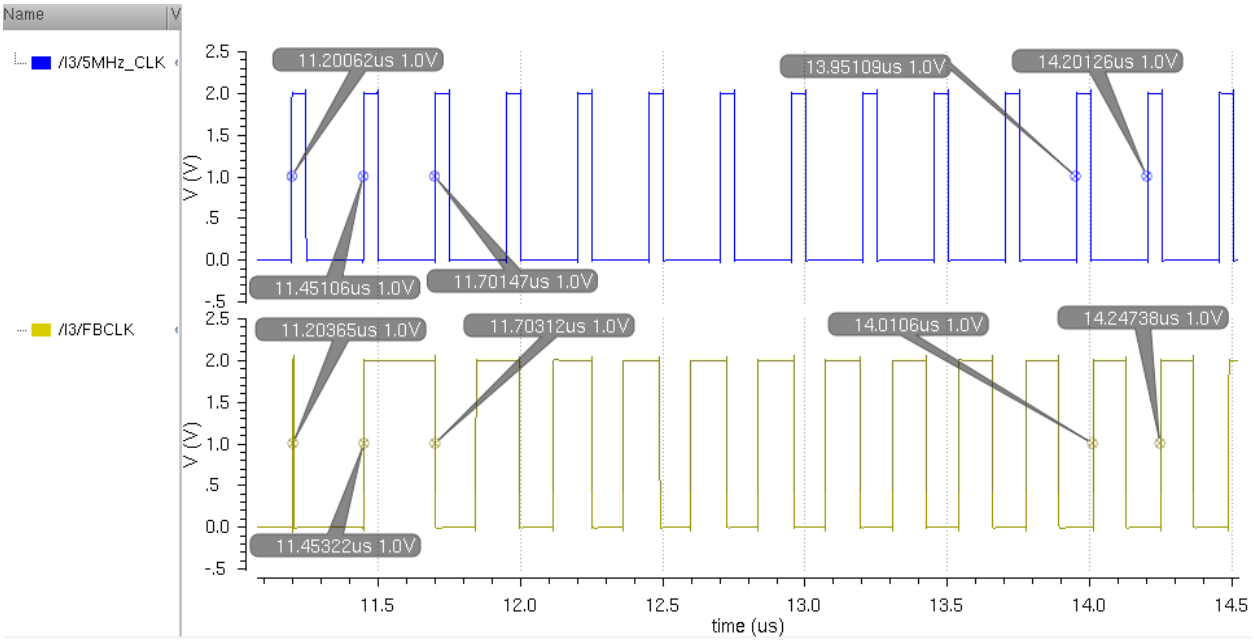

Figure 13. Plot of the Feedback waveform and the input frequency after the prescaler (5MHz_CLK) just after introducing the delay.

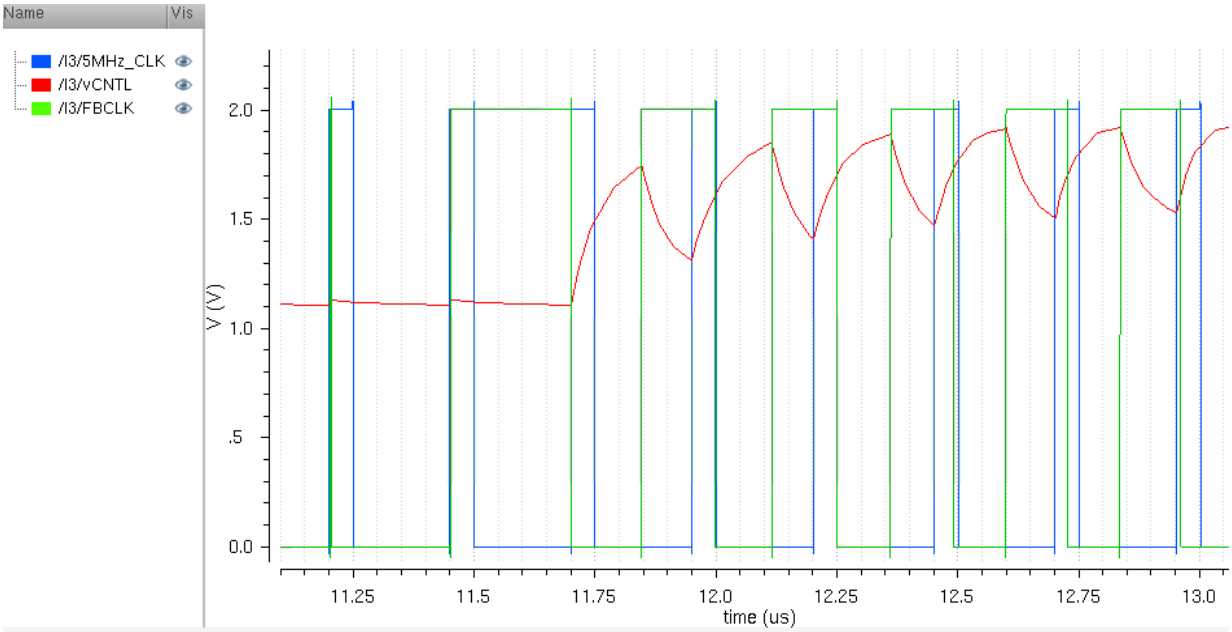

Figure 14. Plot of the Feedback waveform and the input frequency after the prescaler (5MHz_CLK) just after introducing the delay, including the Control Voltage waveform.

To compare both designs, **Figure 15** shows a plot of the Control Voltage for an input frequency of 4MHz (blue) and for a full period delay introduced in the Feedback path (green).

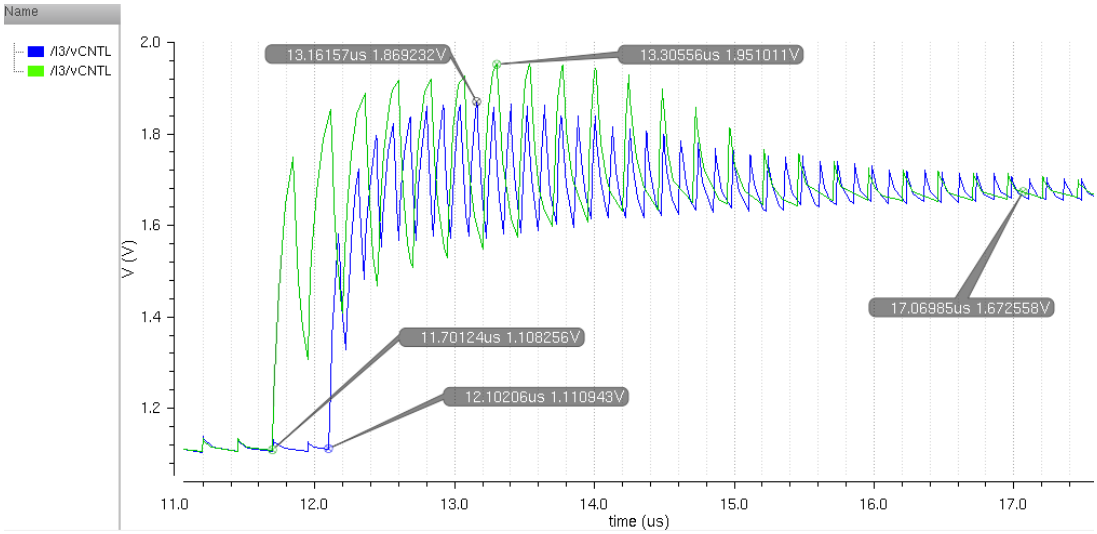

Figure 15.Plot of the Control Voltage for an input frequency of 20MHz, 4MHz after the prescaler.

Conclusion

It is shown that the PLL can keep track of the input frequency after a frequency step change without cycle slipping as long as it is below the Lock-in range, either by forcing a change at the input of the PFD or by introducing one input reference period delay in the Feedback path.

References

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