Assignment 4 ELEC5809 Winter 2015 Carleton University March 19, 2015

Sergio Espinal 100926721

1. Find the Lock-in and Tracking ranges, for definitions and analytical expressions refer to Niedzwiedzki and/or Grebennikov. Compare the measured results with analytical predictions (analyze the circuit to obtain PD gain, values of filter C, R and VCO gain).

The PLL is a feedback control circuit that follows the instantaneous phase input signal by adjusting the phase and frequency output of the VCO.

A PLL circuit is a nonlinear circuit which responds to both the frequency and the phase of the input signal, automatically raising or lowering the frequency of a voltage-controlled oscillator until it is synchronized with the reference in both frequency and phase.

The PLL structure consist mainly of a Phase Detector, a Charge Pump, a Loop Filter, and a Voltage-Controlled Oscillator.

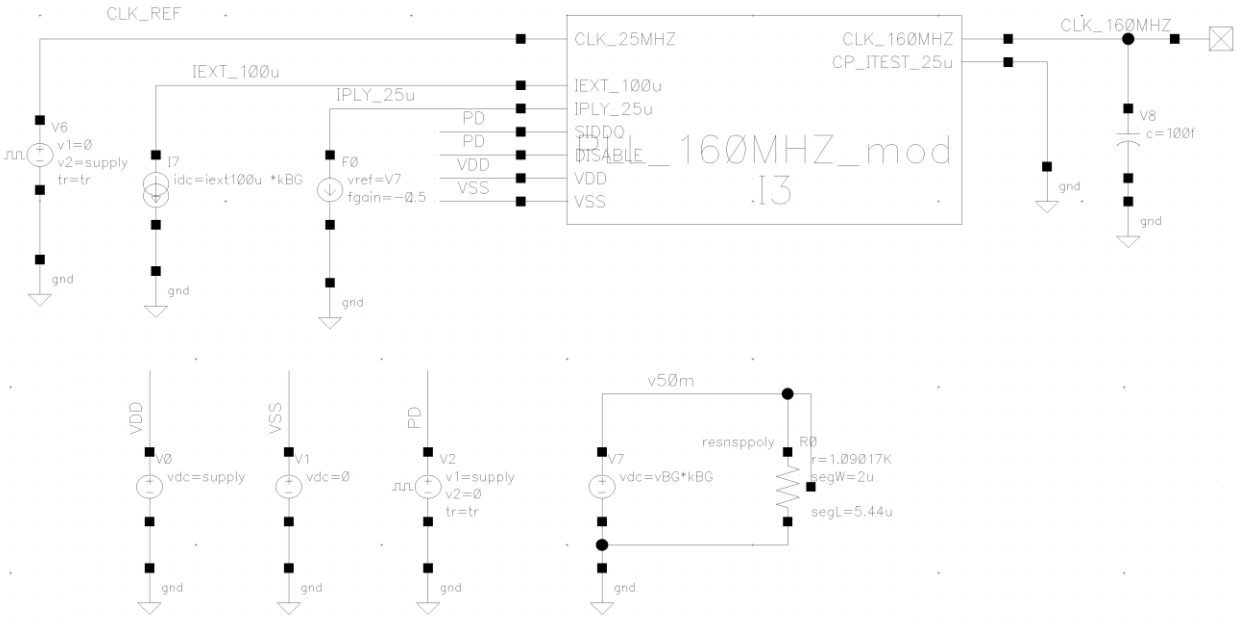

Figure 1. PLL Testbench

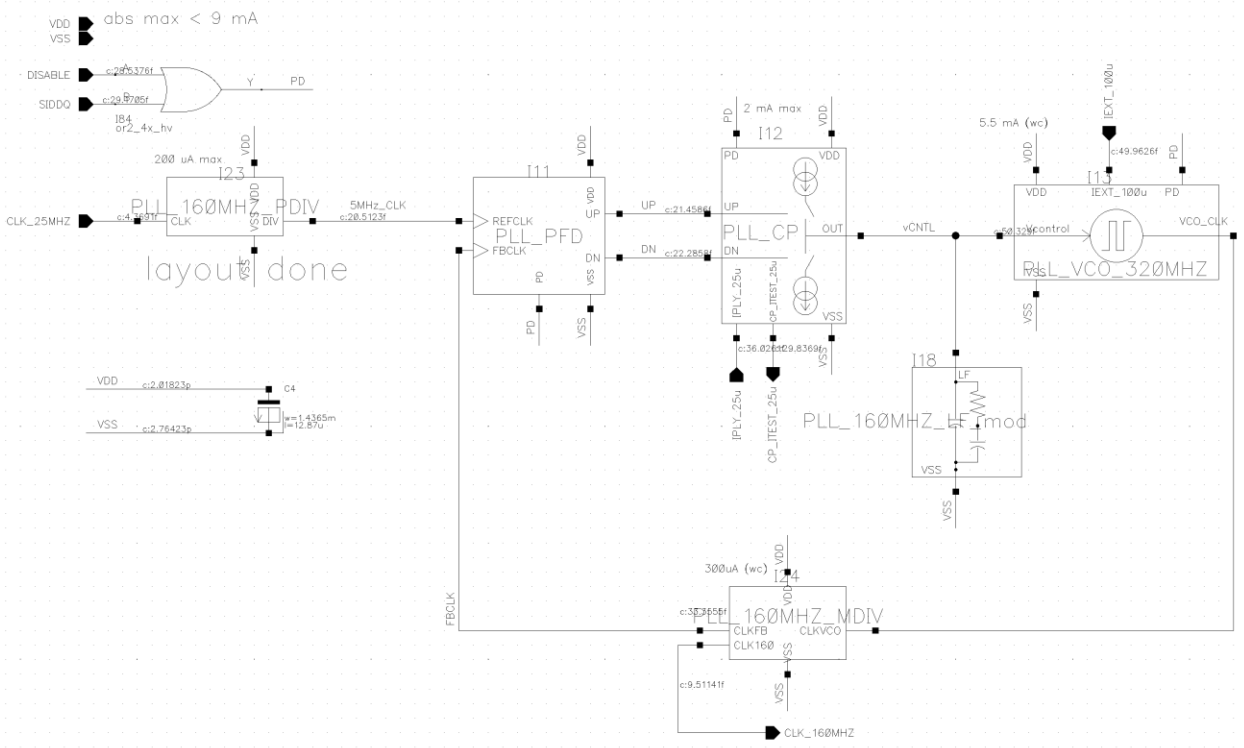

Figure 2. PLL block diagram

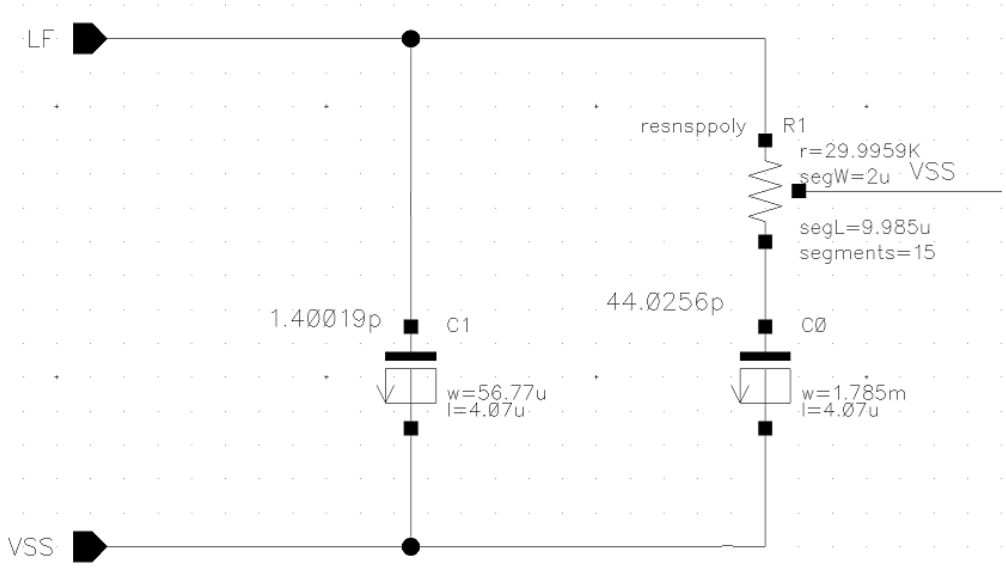

Figure 3. Low-pass Filter circuit

From **Figure 3** the value of the components can be determined:

Component	Value
C1 (C0 in schematic)	44.0256 pF
C2 (C1 in schematic)	1.40019 pF
R1	29.99 KΩ

Table 1. LPF components

To calculate the Phase Detector gain, the value of the current is determined from the PLL testbench schematic in **Figure 1**.

The component F0 is a current-controlled current source, with a gain of -0.5. Its voltage source is V7, with a value VDC = vBG*kBG. By setting the bandgap parameters vBG= 50mV and kBG=1 during simulation, the value of the current will be 25 µA.

$$K_d = \frac{I_p}{2\pi} = \frac{25\mu A}{2\pi}$$

$$K_d = 3.97887 \times 10^{-6} \quad \mathrm{V/rad}$$

By looking at the schematic, the author stated that for an input of 25 MHz, the VCO will generate an output of 320 MHz. Then, it can be assumed that for different Input Reference frequencies, the VCO output frequency will be:

$$\frac{5\ MHz}{25\ MHz} = \frac{f_{VCO}}{320\ MHz} \rightarrow f_{VCO} = 64\ MHz$$

$$\frac{50\ MHz}{25\ MHz} = \frac{f_{VCO}}{320\ MHz} \rightarrow f_{VCO} = 640\ MHz$$

The VCO output frequency depends on the Control Voltage and the VCO gain:

$$\omega_{out} = \omega_0 + K_{VCO} \cdot v_c \qquad (rad/s)$$

To compute the free-running frequency, where $v_c = 0$:

$$\omega_{out} = \omega_0$$

VCO control voltage:

$$v_c = K_d \sin[\phi_e] \approx K_d \cdot \phi_e \quad \text{for small} \quad \phi_e$$

Loop Gain of the PLL is determined as:

$$K = K_d \cdot \frac{K_{VCO}}{N} \cdot P = \frac{I_p \cdot K_{VCO} \cdot P}{2\pi \cdot N}$$

Here, N and P represent the frequency dividers in the circuit.

The **Tracking (Hold-in) range** is the range of frequencies which the VCO can compensate up to a maximum phase error. For a PD with a "saw tooth" characteristic with a maximum phase error of 2π, the Tracking range is calculated as:

$$\Delta\omega_{hold-in} = K \cdot \phi_{e,max} = \left(\frac{I_p \cdot K_{VCO} \cdot P}{2\pi \cdot N}\right) \cdot (2\pi)$$

The **Lock-in Range** is the range of frequencies over which the loop can acquire lock **without cycle slipping**. Cycle slip is caused when the Phase detector is off by one cycle. A "spike" will appear for every cycle slip that occurs, indicating that the current goes negative for some time:

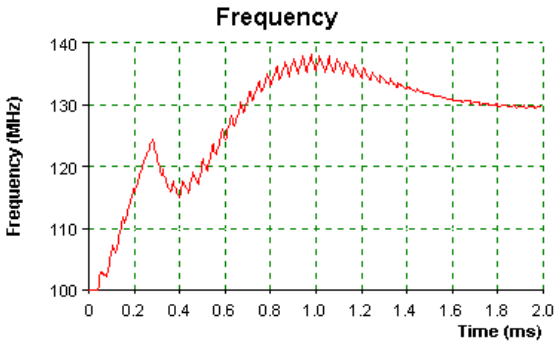

Figure 4. Example of a cycle slip, taken from **[3]**

For a second-order PLL and higher, the Lock-in range holds the following condition:

$$\Delta\omega_{lock-in} < \Delta\omega_{hold-in}$$

If the difference between the free-running and the locked VCO frequencies is less than 3-dB bandwidth of the closed-loop transfer function H(s), then the loop will lock up without slipping cycles, and the maximum lock-in range can be written as:

$$\omega_c \approx \frac{I_p \cdot K_{VCO} \cdot R}{2\pi \cdot N} \cdot \frac{C_1}{C_1 + C_2} \cdot P$$

$$\Delta\omega_{lock-in} = \frac{I_p \cdot K_{VCO} \cdot R}{2\pi \cdot N} \cdot \frac{C_1}{C_1 + C_2} \cdot P$$

The 3dB loop bandwidth:

$$\omega_1 = \omega_{3dB} = \frac{1}{RC_1}$$

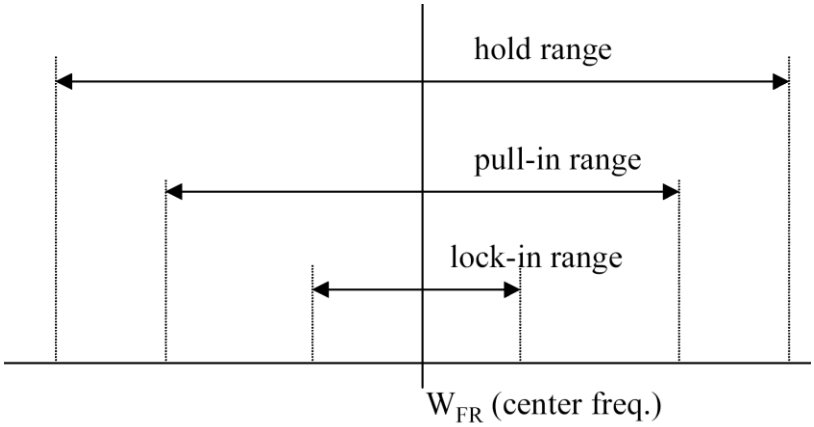

Figure 5. Representation of the Hold, Pull, and Lock-in ranges, taken from **[4]**.

The phase error can be estimated using a frequency step response. This yields the following equation:

$$\Delta\omega = K\phi_e$$

One way to obtain the Tracking Range and the VCO gain is to perform a Parametric Analysis with the settings shown in **Figure 6**.

The idea is to sweep the input Reference Frequency to see what is how the VCO Output Frequency looks like. From Figure 1, the nodes that are taken as Outputs are *vCNTL* and *VCO_CLK*.

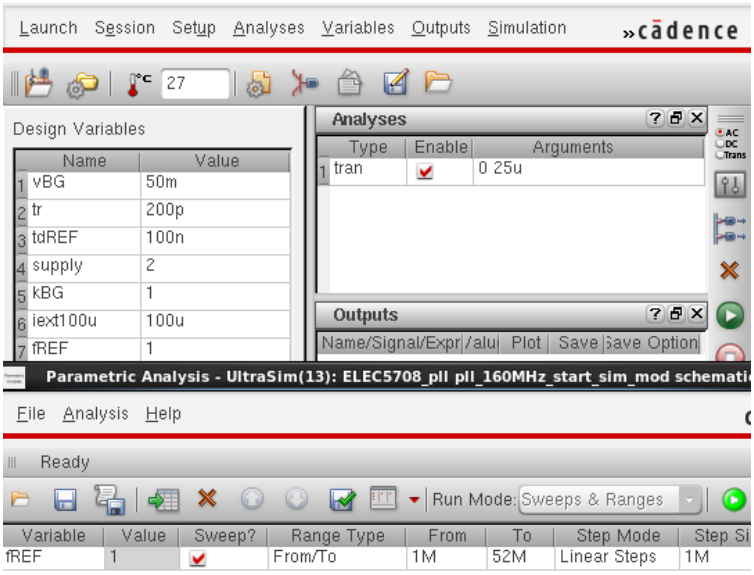

Figure 6. ADE settings for the simulation

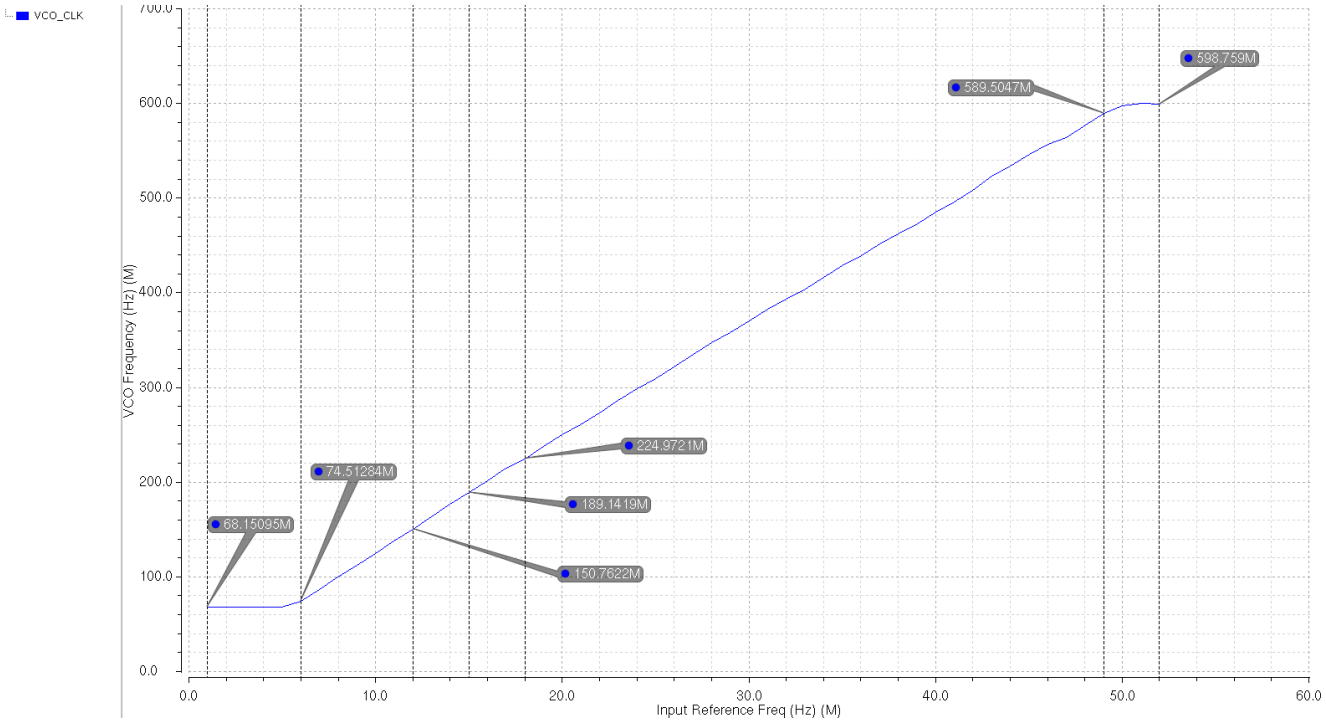

Figure 7. VCO Output Frequency vs Reference Frequency

The VCO Frequency Range, based on simulation, goes from 74.5128 MHz to 589.5 MHz, approximately.

After running the command “Y vs Y”, leaving vCNTL as the x-axis, the VCO Gain can be determined as the slope of the curve in **Figure 8.**

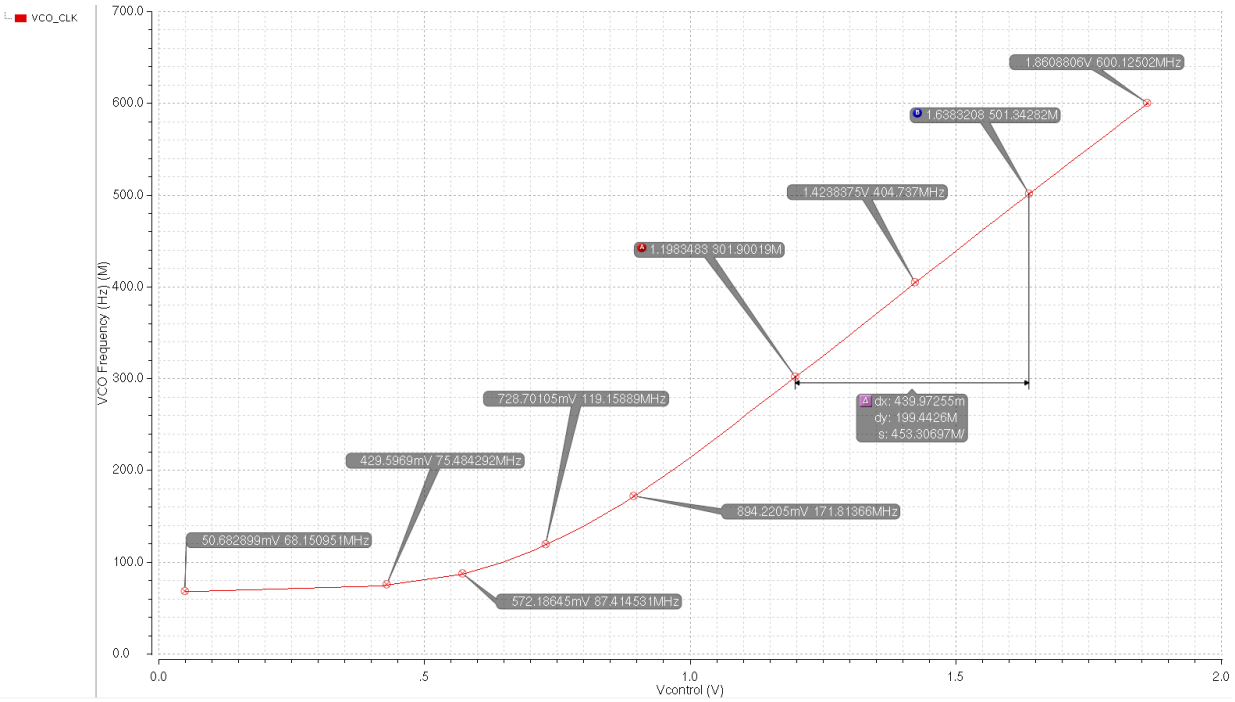

Figure 8. VCO Output Frequency vs Voltage Control

The Voltage Controlled Oscillator Gain is:

$$K_{VCO} = 453.30697 \times 10^6 \ \frac{Hz}{Vs} \quad \rightarrow \quad K_{VCO} = 2.84821 \ \times 10^9 \ \frac{rad}{Vs}$$

The Phase Detector Gain is:

$$K_d = 3.97887 \times 10^{-6} \quad \text{V/rad}$$

The Loop Gain is:

$$K = K_d \cdot \frac{K_{VCO}}{N} \cdot P$$

$$K = \frac{(3.97887 \times 10^{-6} \quad \text{V/rad})(2.84821 \ \times 10^9 \ \frac{\text{rad}}{\text{Vs}})(5)}{(64)} = \ 885.364 \ \frac{rad}{s} \quad \rightarrow \quad K = 140.91 \ Hz$$

Based on the previous steps, the loop gain is: $K = 140.91\ Hz$

The Tracking Range, for a PD with a "sawtooth" characteristic and a maximum phase deviation of 2π, is calculated using the following (Ch 9.6.1 of **[1]**):

$$\Delta\omega_{hold-in} = K \cdot \phi_{e,max} = \left(\frac{I_p \cdot K_{VCO} \cdot P}{2\pi \cdot N}\right) \cdot (2\pi)$$

If $K = 885.364\ \ \frac{rad}{s}$:

$$\Delta\omega_{hold-in} = (885.364\ \ rad/s)(2\pi\ ) = 5.56291\ \ Krad/s$$

$$\Delta f_{hold-in} = 885.364\ Hz$$

The Lock-in Range, for a Second-order PLL and higher, holds the following condition:

$$\Delta\omega_{lock-in} < \Delta\omega_{hold-in}$$

$$\Delta f_{lock-in} < 885.364\ Hz$$

The cross-over frequency, also mentioned as the loop gain:

$$\omega_c \approx \frac{I_p \cdot K_{VCO} \cdot P}{2\pi \cdot N} \cdot \frac{RC_1}{C_1 + C_2}$$

Then:

$$\omega_c = \frac{(3.97887 \times 10^{-6}\ \ \text{V/rad})(2.84821\ \times 10^{9}\ \frac{\text{rad}}{\text{Vs}})(5)}{64} \cdot \frac{29.99K\Omega \cdot 44.0256\ \text{pF}}{1.40019\ \text{pF} + 44.0256\ \text{pF}}$$

$$\omega_c = 2.57336 \times 10^{7}\ \ \ rad/s$$

$$f_c = 4.09563\ MHz$$

The 3dB loop bandwidth:

$$\omega_1 = \omega_{3dB} = \frac{1}{RC_1} = \frac{1}{29.99K\Omega \cdot 44.0256\ \text{pF}}$$

$$\omega_{3dB} = 757.388\ Krad/s$$

$$f_{3dB} = 120.542\ KHz$$

The Phase Error transfer function:

$$\phi_e(s) = \phi_{in}(s) - \phi_{out}(s) = \frac{s\phi_{in}(s)}{s + KF(s)/N}$$

For a frequency step response, setting the limit of $s \to 0$ and $\phi_{in}(s) = \Delta\omega/s^2$:

$$\phi_e = \frac{\Delta\omega}{K} = \frac{\omega_i - \omega_0}{K}$$

If $\Delta\omega = \omega_{3dB}$:

$$\phi_e = \frac{\omega_{3dB}}{K} = \frac{757.388\ Krad/s}{885.364\ \ rad/s} = 855.45\ rad$$

To find out the Lock-in Range from simulation, a frequency step is performed during the transient analysis. **Figure 9** shows the testbench for this task.

First, the PLL is made to lock at a particular frequency (20MHz). After some time, a new frequency is being applied with a difference of 0 Hz to 120.5 KHz between the Input Reference and the VCO (feedback) frequency, which is the 3dB Bandwidth value.

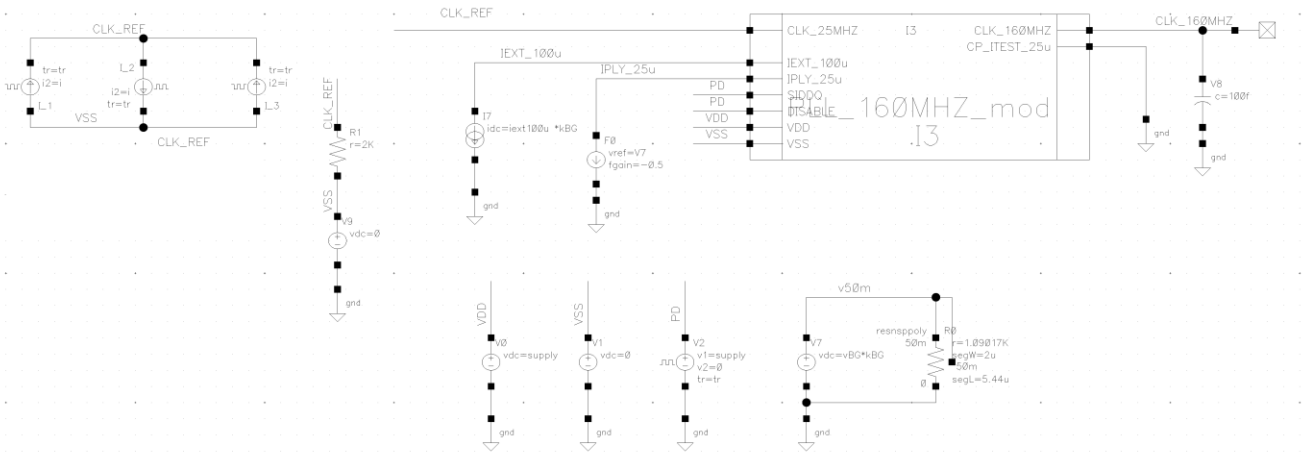

Figure 9. Testbench for frequency step simulation

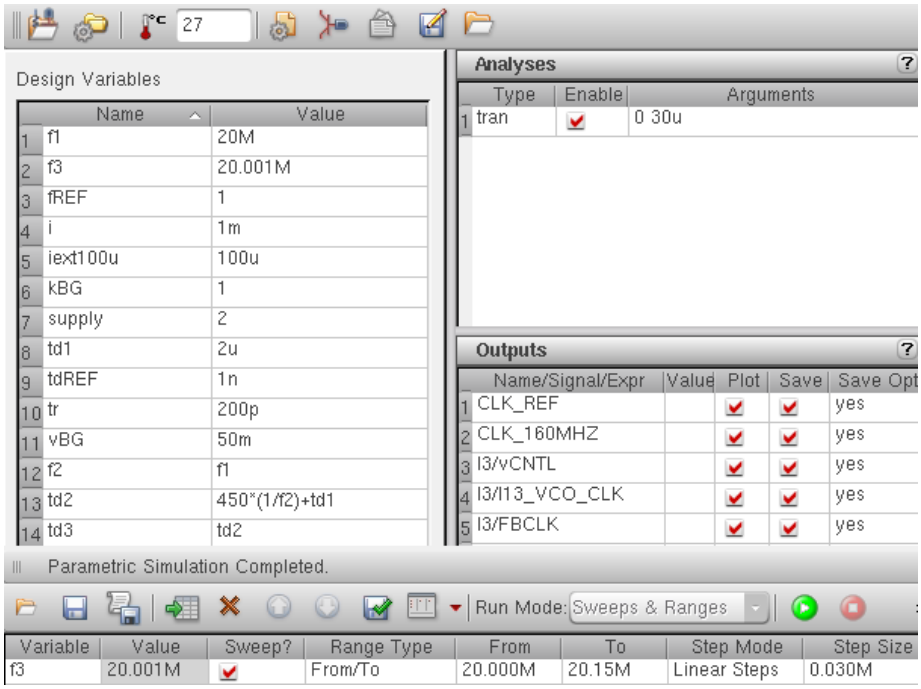

Figure 10. ADE settings for the frequency step.

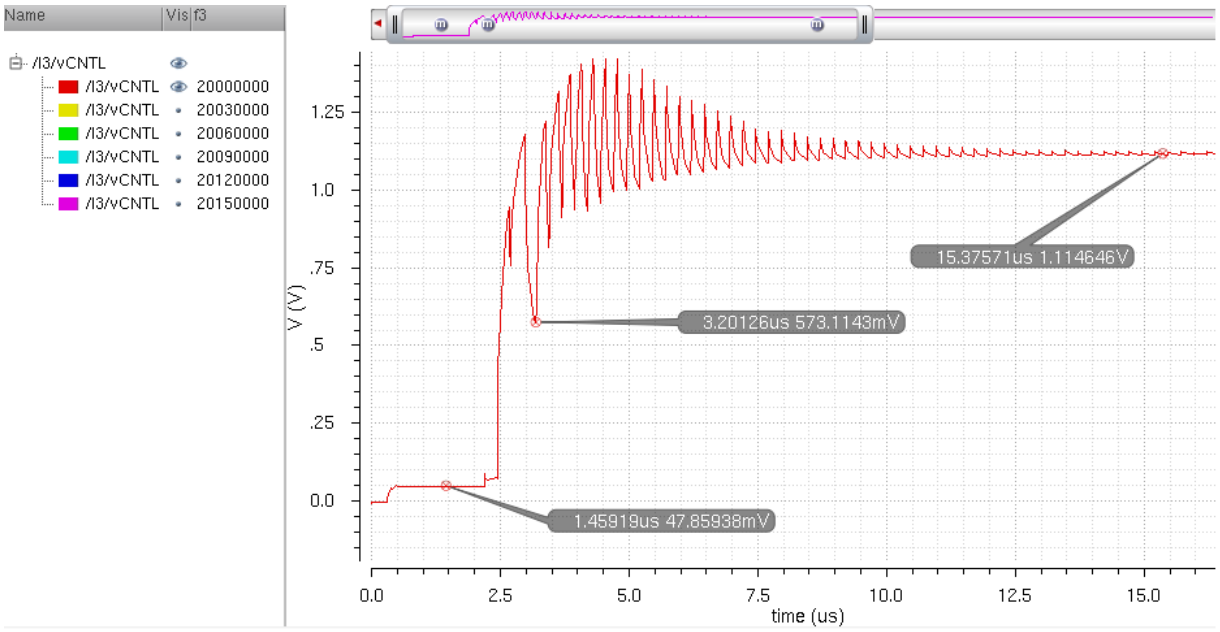

Figure 11. Plot of the first 15µs of the Voltage Control waveforms for different frequency changes.

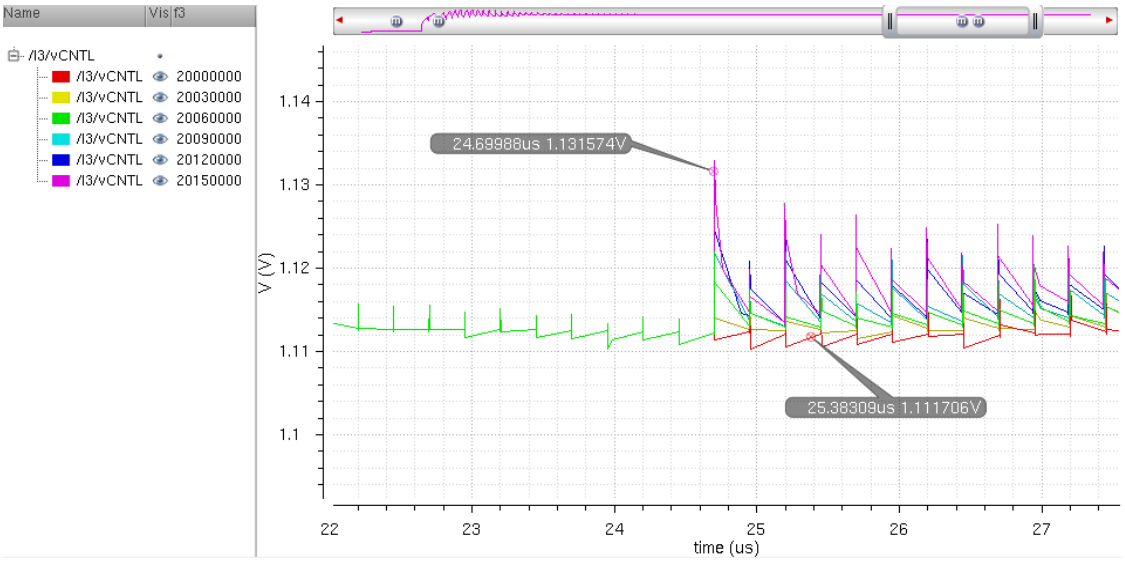

Figure 12. Plot of the section of the Voltage Control waveforms where the frequency change occurs.

As seen in **Figure 11**, there is an initial cycle slip around 3.2µs. In **Figure 12**, the frequency change starts at 24.69µs from the start. It is seen that there is no cycle slip.

2. Find Open Loop Transfer functions, determine Open Loop Bandwidth. Use duplicate circuits on the same simulation page to implement the Middlebrook method. Break the loop at the VCO input. Use results from two duplicate circuits and combine the results using Calculator.

Middlebrook's Method

It is a feedback analysis method used for analyzing the closed-loop gain. The gain may be calculated with either voltage or current gain.

It is not necessary to break the loop to measure these gains. The loop may be opened in its feedback path and the appropriate test signal injected.

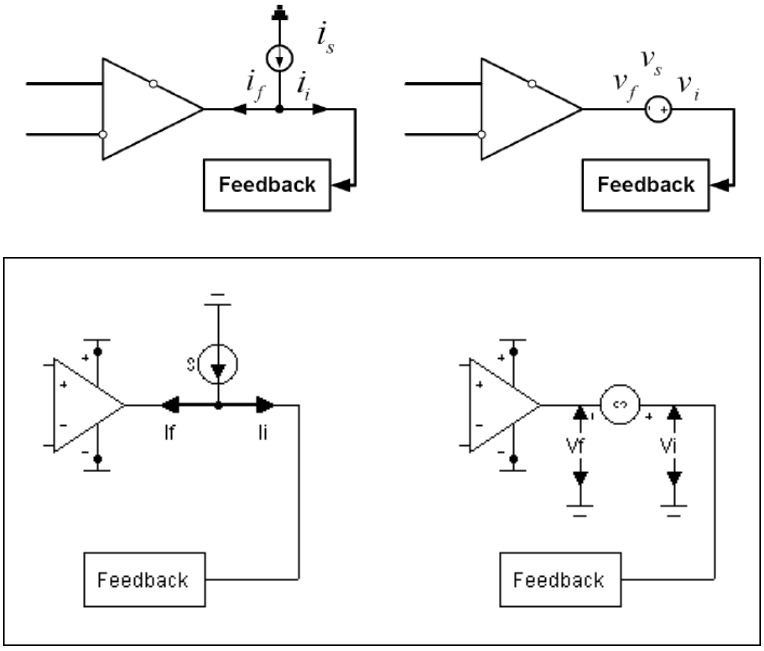

Figure 13. Middlebrook's Method setup.

Injecting a current into the signal path will split the current into its **input** and **feedback** currents. The ratio of the feedback and input current can then be measured to produce a current loop gain.

The voltage gain may also be measured by using the same technique with placing a voltage source in the loop.

$$G_v = \frac{v_f}{v_i} \quad \text{and} \quad G_i = \frac{i_f}{i_i}$$

Both the voltage and current loop gains must be taken into account in order to measure the total loop gain. They are related through the following equation:

$$G = \frac{G_v G_i - 1}{G_v + G_i + 2}$$

In order to implement the Middlebrook's Method, it is necessary to "model" the main components of the PLL since the original ones are nonlinear components. With these components present, it is not possible to perform the AC analysis required.

So, a new PLL schematic is designed mostly with dependent voltage sources and dependent current sources.

The PD is designed with a VCVS, with a gain of 1. The output feeds the Charge Pump, composed by a VCCS, which has a gain equal to Kd.

Then comes the Loop Filter, which is the only element left untouched.

Finally, the VCO is modeled as an integrator. It is formed by a VCVS and a capacitor in parallel. It has a gain of 1, but the capacitor has a value equal to 1/KVCO.

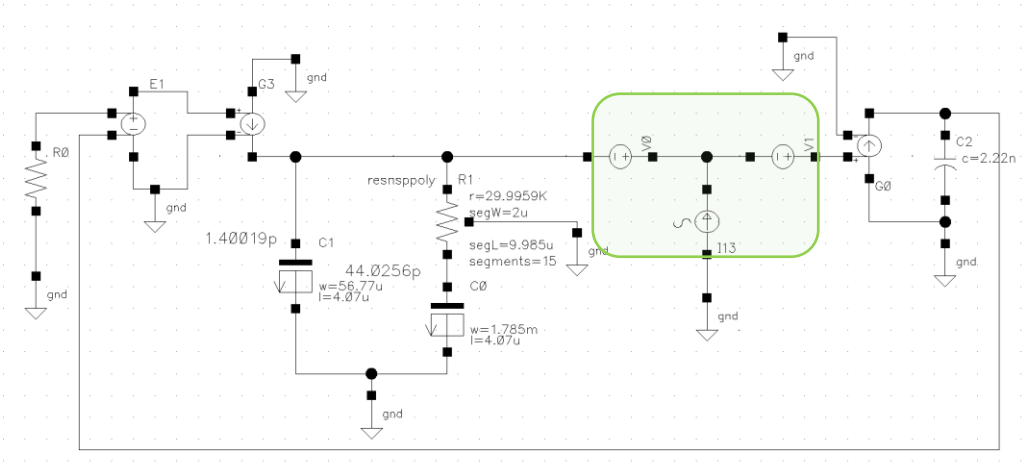

Figure 14. Schematic of the PLL with modeled components for obtaining Gi. The location where the loop is broken is marked with the green area.

Variables for G_i	Location on Figure 14
i_i	V1 negative pin
i_f	V0 positive pin

Table 2. Locations for measuring i_i and i_f

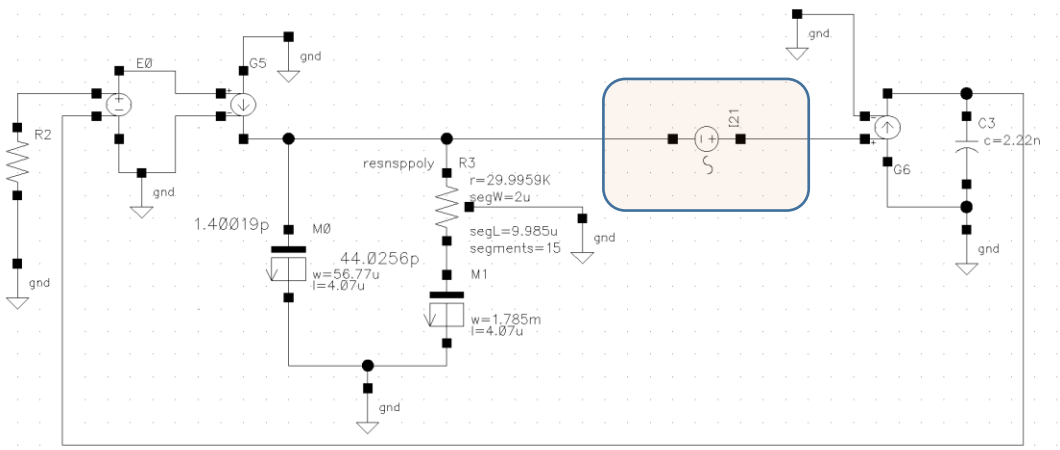

Figure 15. Schematic of the PLL with modeled components for obtaining Gv. The location where the loop is broken is marked with the red area.

Variables for G_v	Location on Figure 14
v_i	Positive node of I21
v_f	Negative node of I21

Table 3. Locations for measuring v_i and v_f

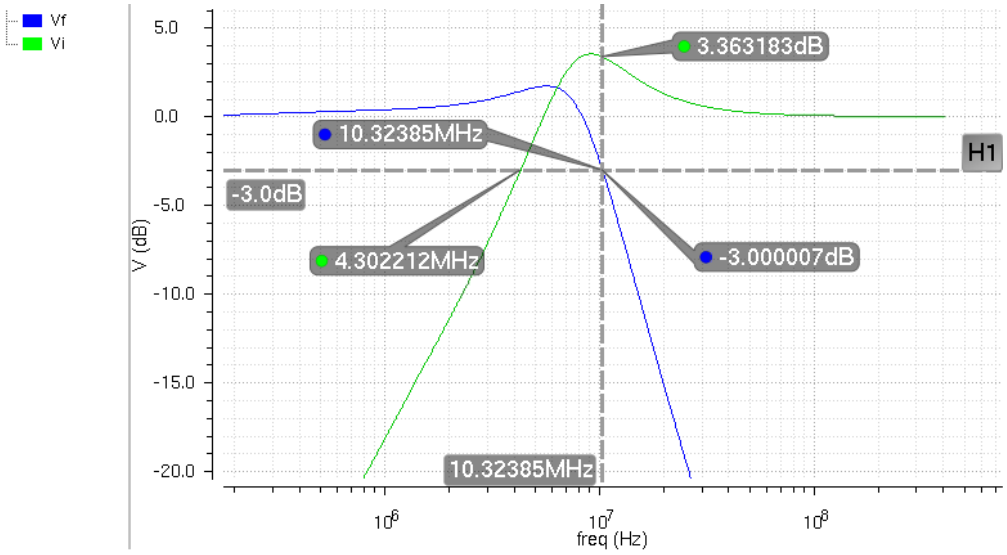

Figure 16. Plot of Vf and Vi frequency response.

Using the Calculator, and applying the equation for the Gain using Middlebrook's Method, the output is shown in **Figure 17**. Note that also the Phase can be plotted using the Calculator.

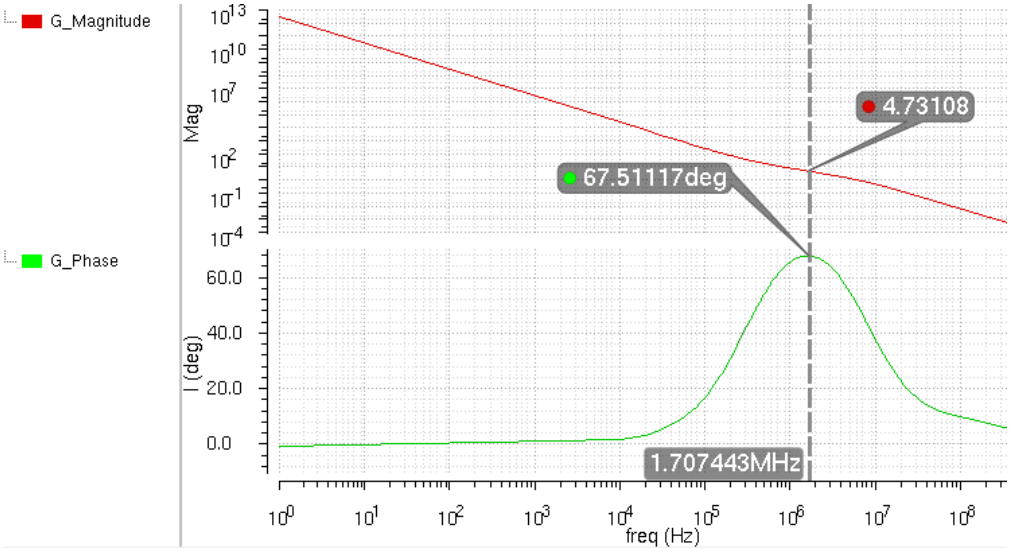

Figure 17. Plot of the Magnitude and Phase of the loop gain G.

References

[1] Grebennikov ,Andrei. Book: "RF AND MICROWAVE TRANSMITTER DESIGN". Wiley, 2011

[2] M. Niedzwiecki. Book: "Nonlinear Analog Circuits".

[3] http://www.radiolab.com.au/designfile/plldes/cycleslip.htm

[4]http://www.doe.carleton.ca/courses/ELEC5708/protected/CLASS%20MATERIAL/notes/Lecture8_PLL_DLL_11_14.ppt

[5] http://www.doe.carleton.ca/courses/ELEC5809/protected/Assignments&Exam/Guo VCO middlebrook 05338949.pdf