Assignment 2 ELEC 5708: ASIC for Telecommunications Carleton University November 3, 2014

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Phase-Locked Loop

Description

The assignment consist on simulating a pre-designed Phase-Locked Loop, based on the 90 nm Generic Process Kit from Cadence, following the tutorial file named *PLL_Tutorial* located at [1].

The software package is *StartCDS5b101*. The cellviews used for this assignment are described in **Table 1**.

Ether library cellviews	Description
PLL_160_MHZ	PLL circuit
PLL_160MHZ_LF	Low-Pass Filter
PLL_160MHZ_PDIV	Input Prescaler
PLL_160MHZ_MDIV	Output Prescaler
PLL_CP	Charge Pump
PLL_PFD	Phase Frequency Detector
VCO_320MHZ	Voltage Controlled Oscillator

Ether_sim library cellviews	Description
pll_160MHz_start_sim	PLL circuit testbench
pll_pfd_cplf_sim	PFD, CP and LPF testbench
pll_pfd_sim	PFD testbench
pll_vco_320MHz_sim	VCO testbench

Table 1. Cellviews used from *ether* and *ether_sim* libraries.

Phase-Locked Loop

The phase-locked loop is a closed-loop control system that synchronizes the phase of an output signal with the phase of an input signal, making the output signal to have the same frequency of the incoming signal.

The phase is the integral of the frequency. This implies that in locked state the phase difference between the input phase $\varphi_{in}(t)$ and output phase $\varphi_{out}(t)$ must be constant:

$$\frac{d\varphi_{out}(t)}{dt} - \frac{d\varphi_{in}(t)}{dt} = 0 \quad \rightarrow \omega_{out} = \omega_{in} \qquad (1)$$

The basic elements of a Phase-Locked Loop are:

- Phase-Frequency Detector
- Charge Pump
- Low-Pass Filter
- Voltage-Controlled Oscillator

Depending on the application, it may also be included a Frequency Divider to provide a Feedback signal back to the PFD instead of the VCO output.

The key parameters of a Phase-Locked Loop are:

- Free-running Frequency
- Capture Range
- Lock-in Range
- Open Loop Bandwidth
- Dead zone
- Power Consumption

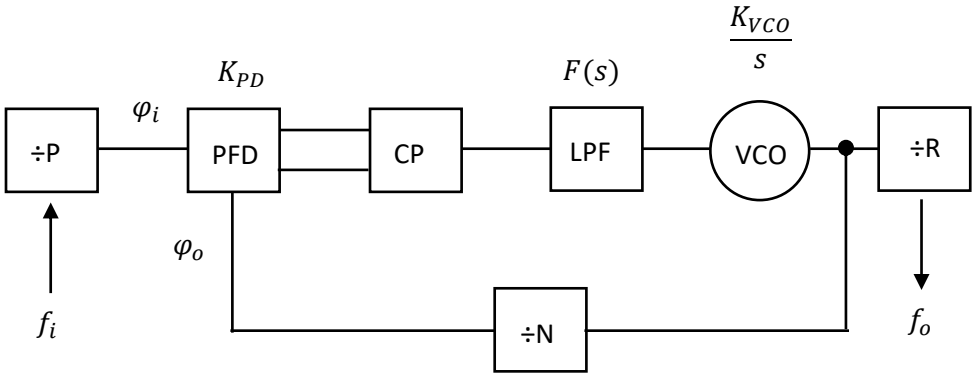


Figure 1. Block diagram of a Phase-Locked Loop system.

Phase-Frequency Detector

Its function is to detect the phase difference between two signals, and deliver a proportional output. It also responds to frequency difference to, hence the name phase-frequency detector.

It is a 3-state phase-frequency detector composed by two D-type Flip-Flops, and one AND gate.

It compares the input reference signal phase with the VCO output signal phase, and creates output pulses UP or DOWN which are used to steer the Charge Pump, as described on **Table 2**.

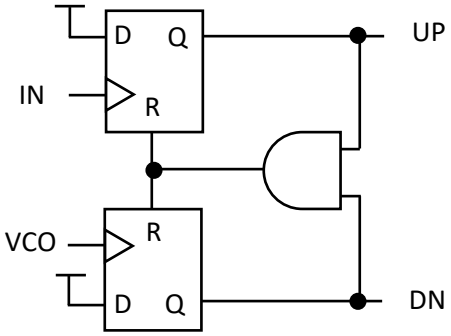


Figure 2. Diagram of a Flip-Flop PFD.

IN	VCO	UP	DOWN	Status
0	0	0	0	Initial condition
0	1	0	1	Out leads In , VCO too fast
1	0	1	0	In leads Out , VCO too slow
1	1	1->0 , Z	1->0, Z	RESET (High Z), VCO Drifts

Table 2. Truth table of the Flip-Flop PFD.

Charge Pump

The Charge Pump is a "transducer", composed of two controllable current sources connected to one common output, which takes the phase difference response output current from the PFD and translates it into a control signal voltage to change the frequency of the VCO.

This signal is the result of charge pulses being integrated by a loop filter capacitance, a Low-Pass Filter.

The current being sink/sourced is proportional to the maximum available current and a Gain coefficient K_{PD} in V/rad.

$$i_{ave} = I_{CP} \cdot \frac{\tau_{diff}}{T_{period}} = I_{CP} \cdot \frac{|\Delta\varphi|}{2\pi} \qquad (2)$$

$$K_{PD} = \frac{I_{CP}}{2\pi} \qquad (3)$$

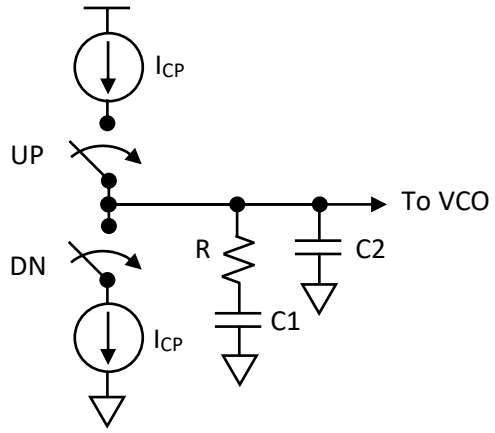


Figure 3. Diagram of a Charge Pump connected to a 2nd Order LPF.

Dead Zone

As the PLL tries to synchronize the Input Reference and the Feedback signals, the phase difference reduces. The control signal changes as UP or DOWN pulses change proportionally.

Under lock condition, there is almost no phase difference, and RESET input for both Flip-Flops is driven through the AND gate (OR gate if the signals are taken from the $\bar{Q}$'s). This sets the UP and DOWN into a high impedance state, making the Charge Pump to produce neither a positive charge nor a negative charge pulses.

The phase error $\Delta\varphi_e$ may be so small that the PFD output pulses, either UP or DOWN, are not long enough to drive the Charge Pump. The VCO would drift, possibly for a long time, until a significant phase error is developed making the CP to start producing either positive or negative current pulses once again.

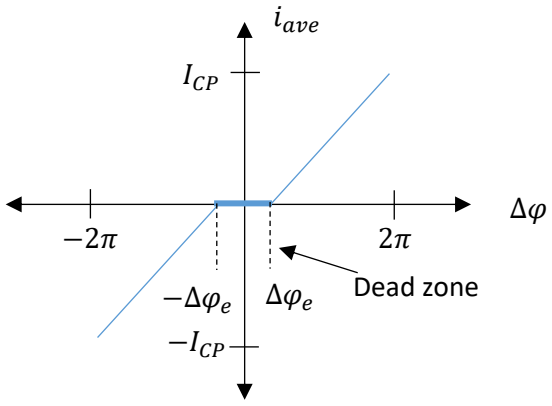


Figure 4. Diagram of the phase range showing the dead-zone (no current output).

To overcome this condition, the tri-state PFD is forced to operate with a minimum finite output pulse duration. This is done by inserting a "Delay cell" between the RESET input of both Flip-Flops and the output of the AND gate.

The combined delay of the AND gate, the Delay cell, and any phase difference (one leading the other) will determine the time both pulses will remain "asserted" before they are both reset.

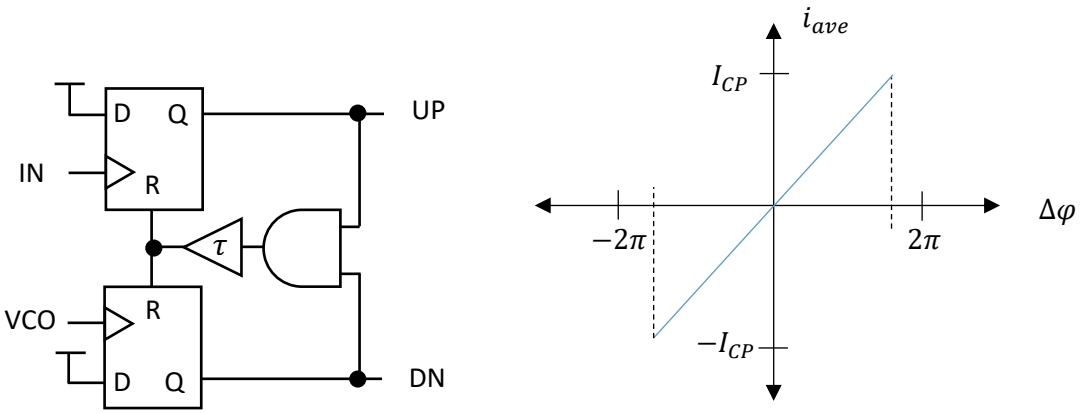


Figure 5. PFD corrected and the linearization of the phase range.

Therefore, for very small phase differences even when $\Delta\varphi = 0$, both outputs of the PFD (UP and DN) send pulses to the charge pump of approximately equal width and amplitude. These pulses inject to and sink from the loop filter the respective amount of current. As a consequence, the dead zone is eliminated without modifying the VCO control voltage.

This method improves PFD gain linearity, but reduces the usable phase range from 4π. The delay has to be large enough to reduce the impact of noise at very low phase differences.

Low-Pass Filter

A 2nd Order LPF is used to convert the Charge Pump output current into a voltage to control the VCO.

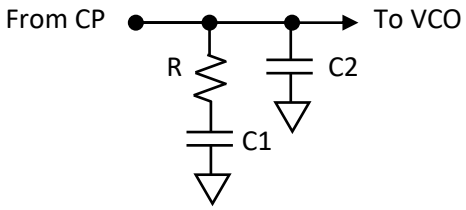


Figure 6. Diagram of a 2nd Order LPF.

The transfer function is given as:

$$F(s) = \frac{sRC_1 + 1}{s^2RC_1C_1 + s(C_1 + C_2)} = \frac{sRC_1 + 1}{s(C_1 + C_2)(sRC_a + 1)} \qquad (4)$$

$$C_a = \frac{C_1C_1}{C_1 + C_2} \qquad \omega_1 = \frac{1}{RC_1} \qquad \omega_{p3} = \frac{1}{RC_a} \qquad (5), (6), (7)$$

The function of C_2 at the LPF transfer function is to attenuate or "smooth" discrete voltage steps or ripples of the series RC network, due to the sudden change of current from the output of the Charge Pump. Normally $C_2 \ll C_1$ to minimize the influence of its pole.

Voltage-Controlled Oscillator

The Voltage-Control Oscillator is an oscillator which delivers an output frequency that may be increased or decreased according to an input voltage. The relationship generally is non-linear, but it behaves linearly for some smaller range called VCO tuning range.

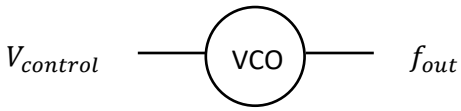


Figure 7. VCO block.

The VCO oscillates at an angular frequency ω_{out}, defined by the free-running frequency ω_o and a control voltage $V_{control}$ times the gain coefficient K_{VCO} (in rad/V/s) shown in equation (8).

$$\omega_{out} = \omega_o + K_{VCO} \cdot V_{control} \qquad (rad/s) \qquad (8)$$

When $V_{control} = 0$, the VCO oscillates at its free-running frequency ω_o.

The gain K_{VCO} is approximately equal to the slope of the linear part of the ω_{out} vs $V_{control}$ curve.

The $V_{control}$ range where the ω_{out} has a linear behaviour is defined as the $V_{control}$ tuning range.

Frequency Divider

It is a circuit that takes an input frequency, divides it by an integer N, and generates an output frequency which is a multiple of the input frequency.

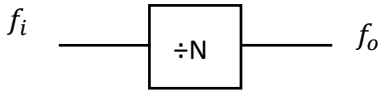


Figure 8. Frequency Divider or Prescaler.

$$f_o = \frac{f_i}{N} \qquad (9)$$

In the PLL circuit for this assignment, the frequency divider cell PLL_PDIV divides the incoming frequency by 5. The frequency divider PLL_MDIV divides the VCO output frequency by 64. The resulting signals are fed into the phase detector to be compared.

Free Running frequency

It is the frequency of the VCO output when there is no input reference signal.

Frequency range (capture range)

It is defined as the range of input frequencies in which the PLL can acquire a lock condition from an unlocked state (free-running VCO). The frequency range cannot be greater than the locking range.

Locking range

It is defined the range of frequencies that the VCO can track after it has acquired locking. The range is limited by the capacity of the VCO.

Procedure

For the assignment purposes, the following modifications from the original circuit were done:

- The PLL_LPF cellview was modified by removing the two NMOS transistor.
- The PLL_160_MHz_sim was modified by removing the AutoReset Block (PLL_ARST and PLL_ARST_DIG), and replacing the original LPF circuit with a modified one.

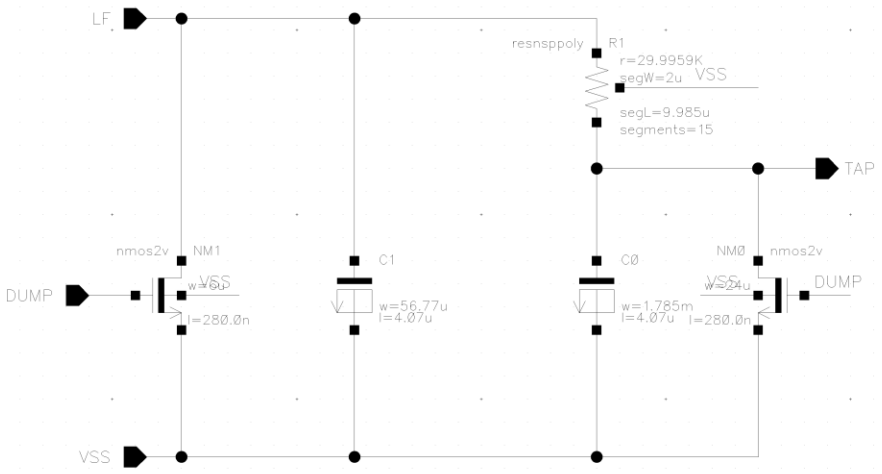


Figure 9. Schematic of the original LPF circuit PLL_160MHZ_LF.

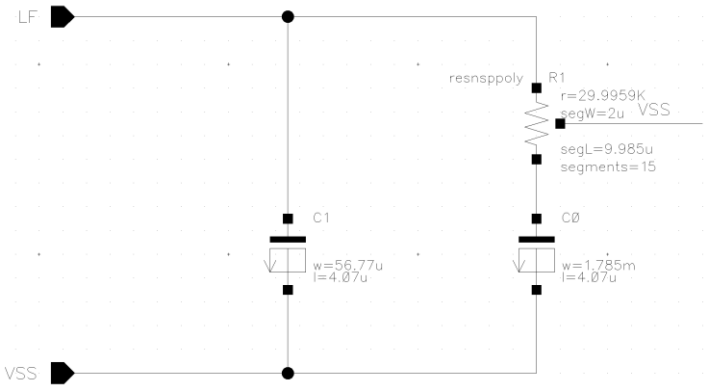


Figure 10. Schematic of the modified LPF circuit named PLL_160MHZ_LF_mod.

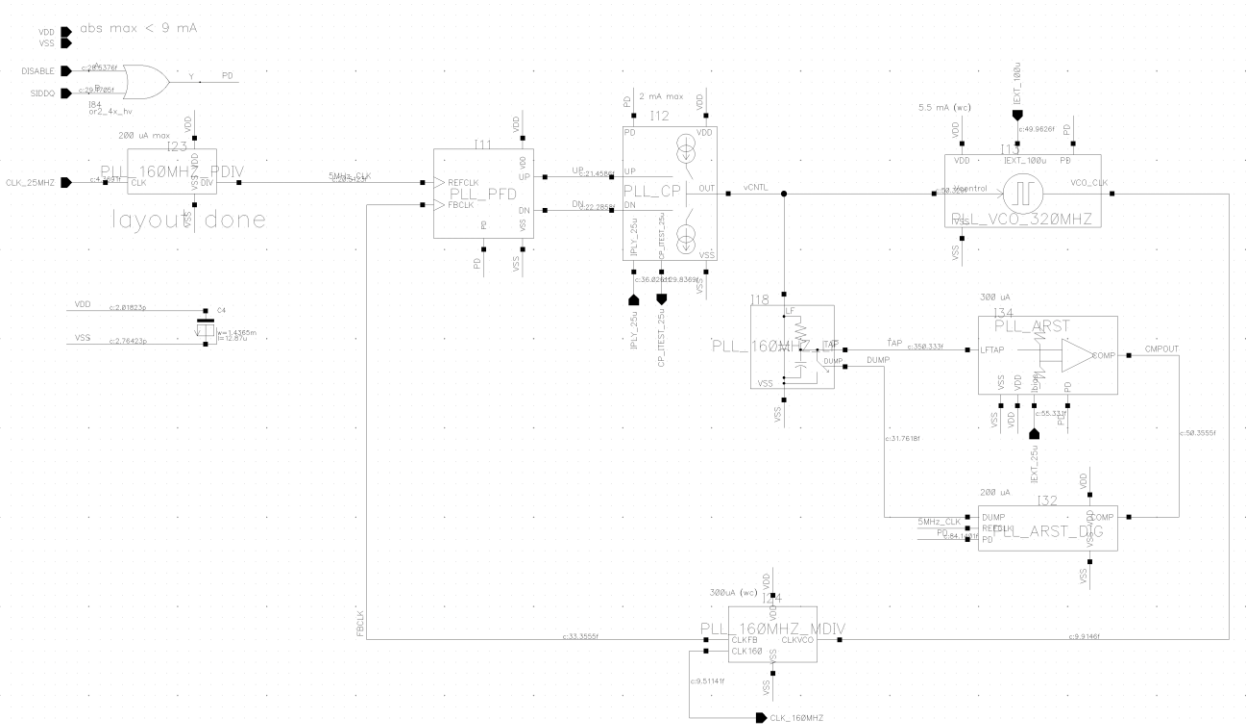


Figure 11. The original circuit of the PLL.

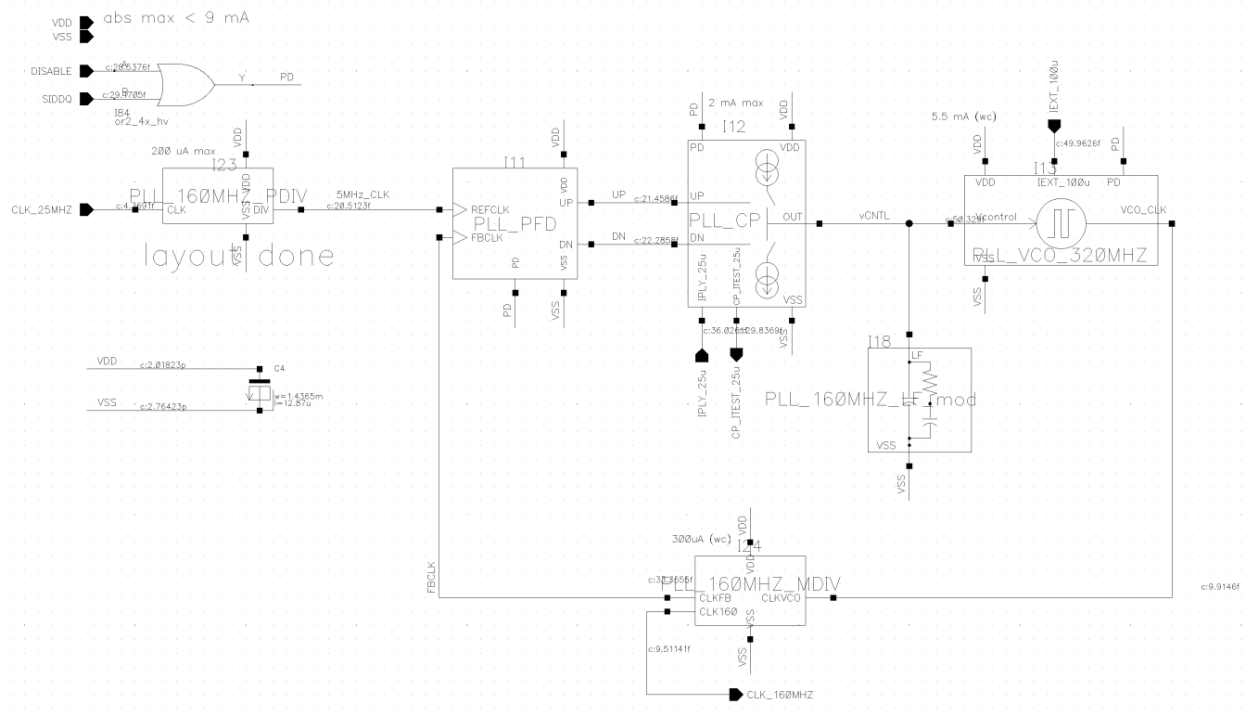


Figure 12. The modified circuit of the PLL.

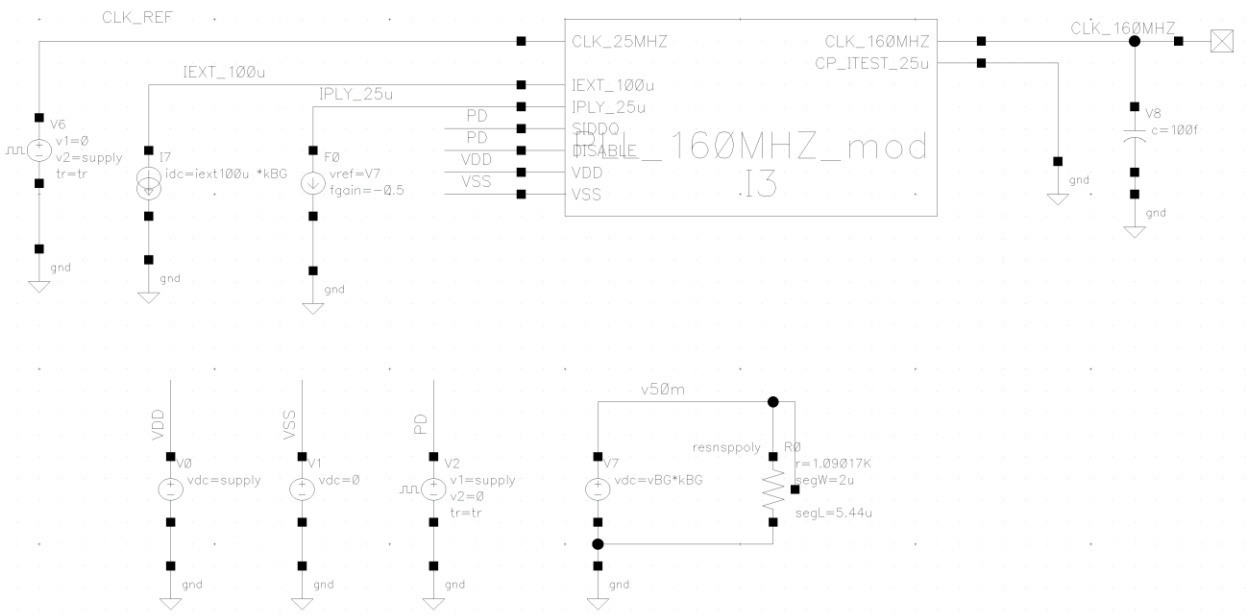


Figure 13. PLL test-bench block.

Setting the rise time and fall time for the Input Signal

To give a realistic shape of the pulse for the input signal, the rise and fall times are set based on the slowest values found among the output signals of the blocks that compose the PLL. The rise time will be set equal to the fall time.

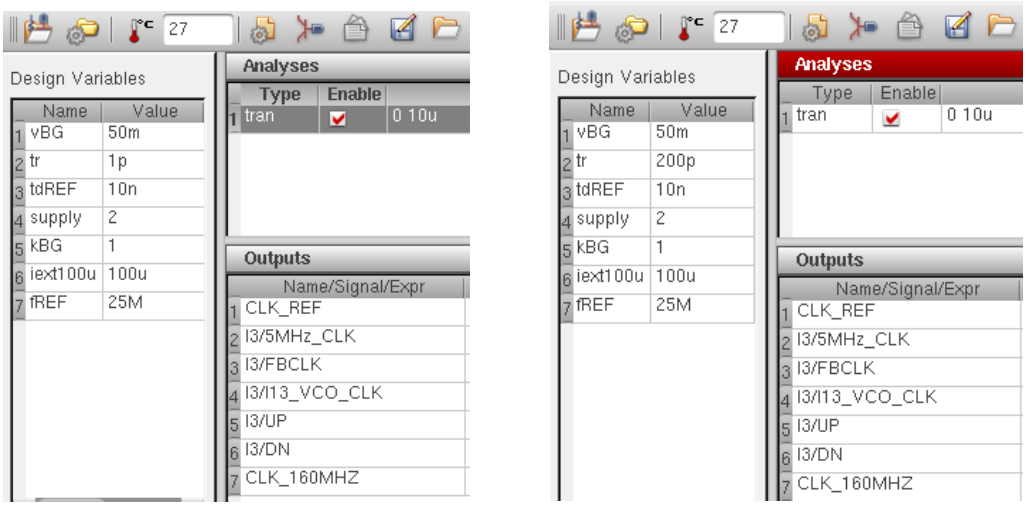


Figure 14. ADE settings for rise and fall time calculation from the waveforms.

Rise times:

Outputs	T-rise = 1ps	T-rise = 200ps
160MHz_CLK:	198 ps	192.819 ps
5MHz_CLK:	56.2145 ps	55.398 ps
DN:	34.8115 ps	35.6261 ps
UP:	33.67 ps	33.4346 ps
FBCLK:	54.12 ps	54.87 ps
CLK_REF:	159 fs	160 ps
VCO:	63.4297 ps	63.772 ps

Table 2. Rise time of different output for an input.

The rise time and fall time for the input signal is set to 200 ps.

Phase Detector Dead Zone

The test-bench for calculating the dead-zone is composed by the CP, the LPF and a dummy load, shown in **Figure 15**.

The calculation is done in two steps: first for the positive side of the phase margin where the input signal leads the feedback, and then for the negative side of the phase margin where the input signal lags the feedback.

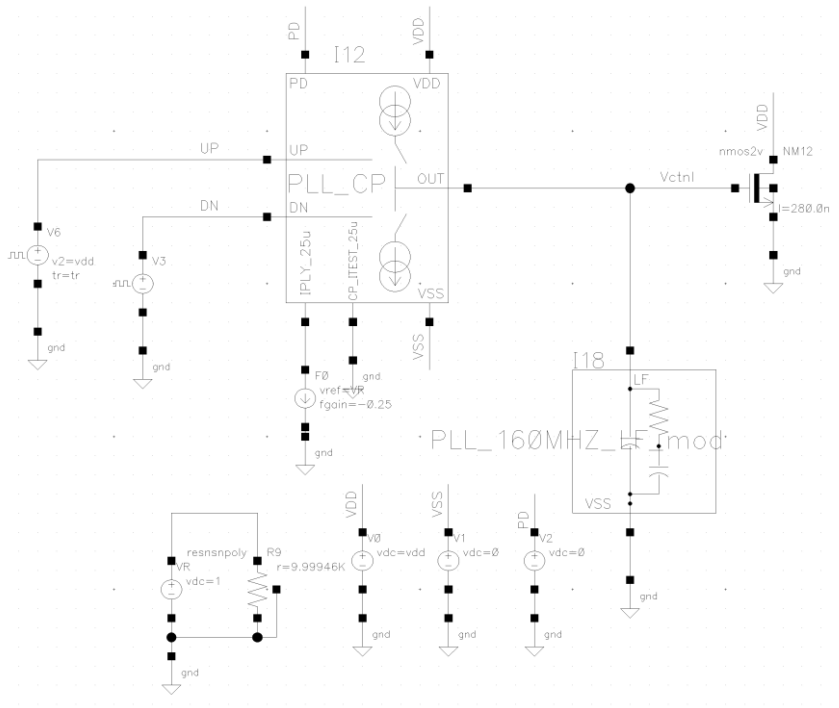


Figure 15. Test-bench for computing the dead-zone band.

*Input signal **leads** feedback signal*

The DN input is set as 0V. The pulse width of the UP input signal is set by fREF_pulsew. Using the setting in **Figure 16**, a Parametric Analysis is run for 1ps to 500ps, in linear steps of 10ps. The result will be a family of waveforms of Vcntl. The curve in **Figure 17** can be plotted using the following equation:

average(getData("/Vctnl" ?result "tran"))

By setting DN input to zero (no pulses), there will always be a phase difference present, and the limit of the dead-zone will be easier to point out. The Vcontrol will start to rise until a minimum phase difference (pulse width) condition is met.

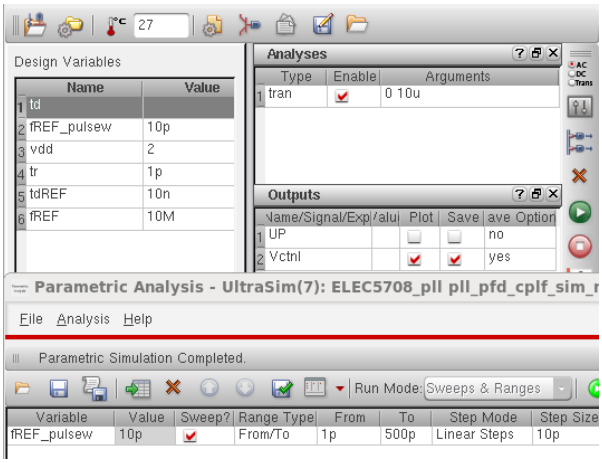


Figure 16. ADE settings for Phase Detector Dead Zone simulation.

For a frequency f, the dead-zone portion where reference input signal **leads** the feedback output signal of the VCO lies between $0 \leq \Delta\varphi \leq 2\pi f \cdot \Delta t$, where $\Delta t = 90\ ps$ as seen in **Figure 17**.

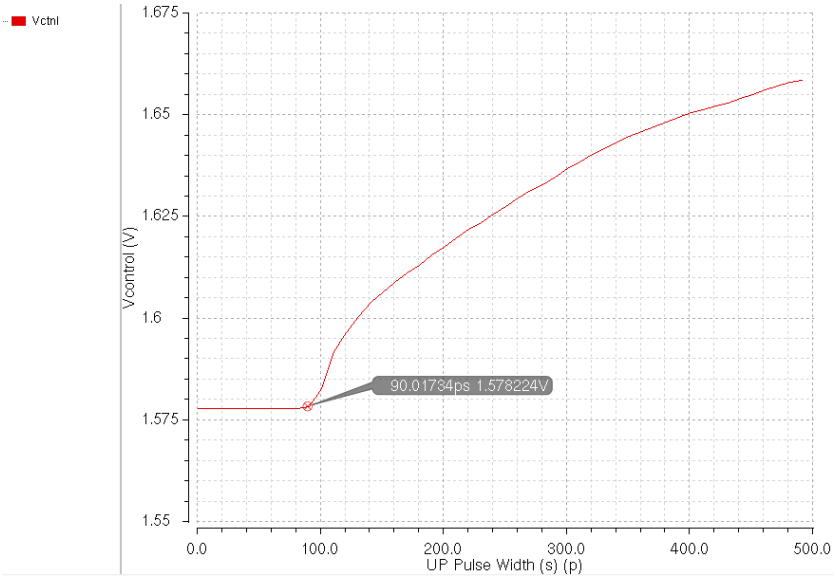


Figure 17. Input Reference signal leading the Feedback signal.

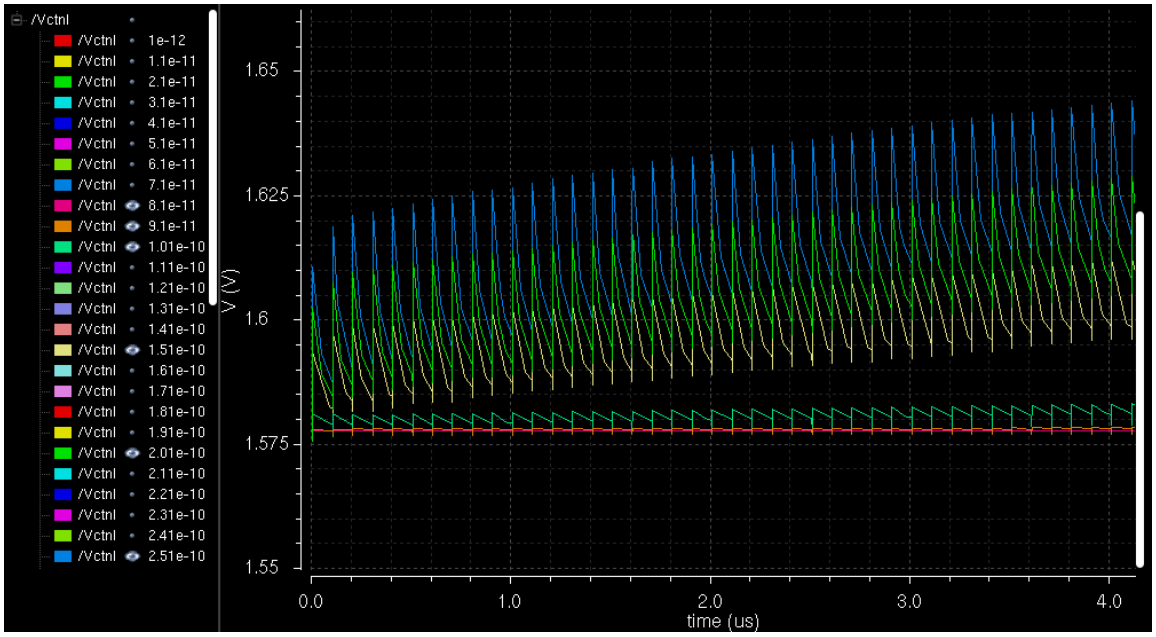


Figure 18. Input Reference signal leading the Feedback signal.

*Input signal **lags** feedback signal*

Same steps as the previous simulation, except that the UP input is set as 0V. The pulse of the DN input signal is set by fREF_pulsew.

For the same frequency f, the dead zone portion where reference input signal **lags** the feedback output signal of the VCO lies between $-2\pi f \cdot \Delta t \leq \Delta\varphi \leq 0$, where $\Delta t = 116.3\ ps$ as seen in **Figure 19**.

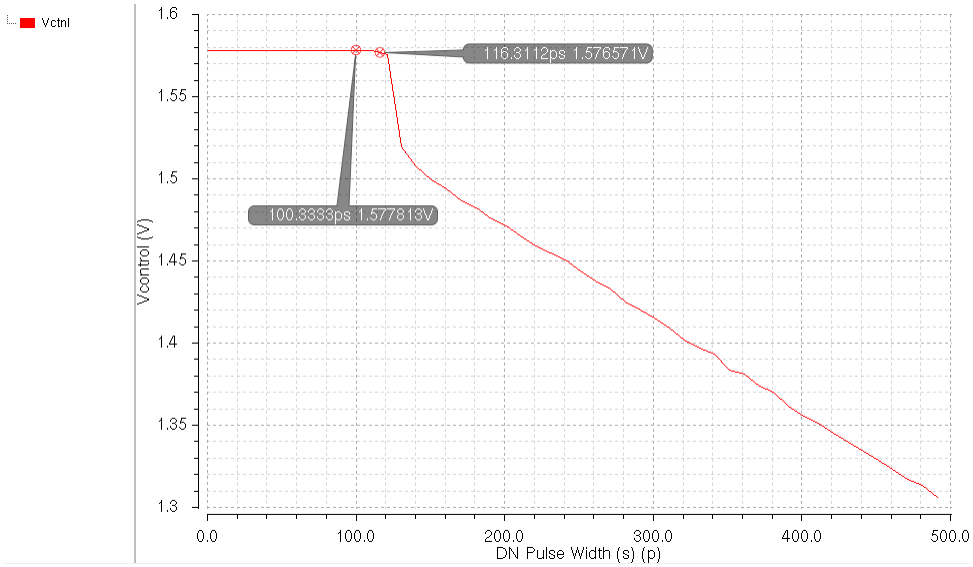


Figure 19. The Feedback signal leading the Input Reference signal.

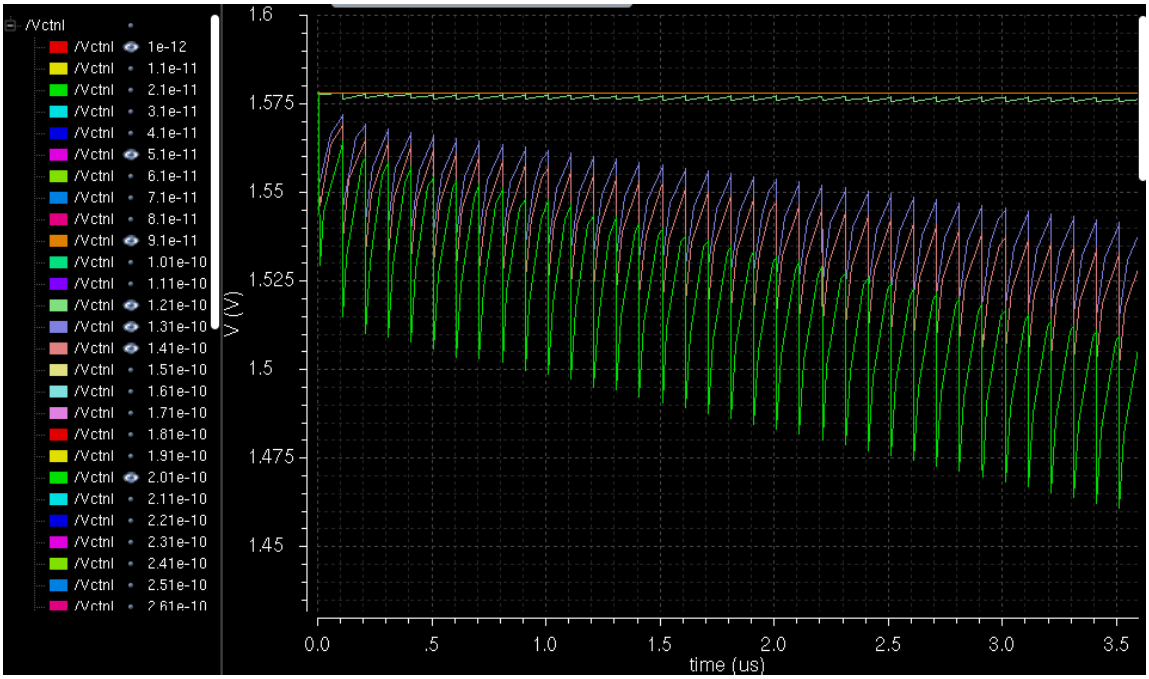


Figure 20. Input Reference signal lagging the Feedback signal.

VCO Output Frequency Range

Two test-benches will be used to compute the VCO Output Frequency Range for a $V_{control}$ range, and then compare the results.

First Test-Bench

The first test-bench involves only the VCO block, shown in **Figure 21**. For simulation, *Ultrasim* simulator was used instead of *Spectre.*

Setting the Analog Design Environment with the settings shown in **Figure 22**, a Parametric Analysis is being run by sweeping the parameter vCNTL from 0V to 2V with a step size of 0.1V. A family of VCO output signals will be generated as seen in **Figure 23**.

The plot in **Figure 24** is being generated by typing the following command in the Calculator:

frequency(getData("/VCO_CLK" ?result "tran"))

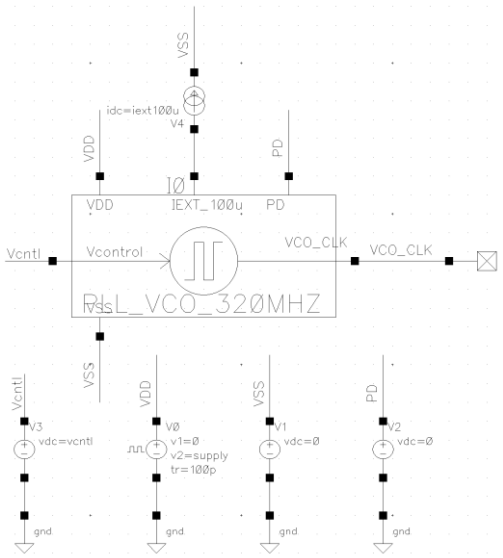


Figure 21. VCO block test-bench to calculate the VCO frequency range.

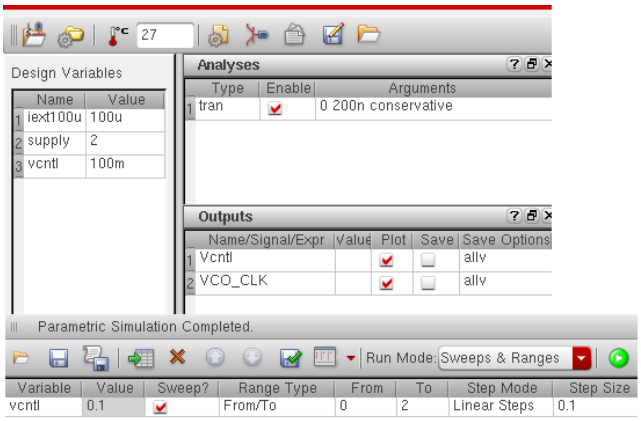


Figure 22. ADE simulation settings for the first test-bench for the VCO frequency range.

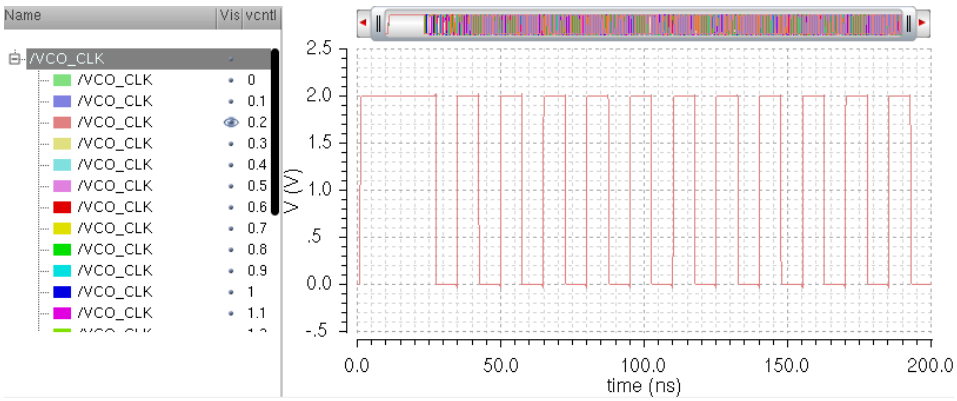


Figure 23. Plot of waveform of VCO output for a control voltage of 0.2V.

	vcntl	frequen...0E-9))
1	0.000	66.60E6
2	100.0E-3	66.60E6
3	200.0E-3	66.60E6
4	300.0E-3	66.61E6
5	400.0E-3	66.77E6
6	500.0E-3	68.42E6
7	600.0E-3	75.82E6
8	700.0E-3	92.95E6
9	800.0E-3	120.4E6
10	900.0E-3	156.5E6
11	1.000	196.6E6
12	1.100	238.4E6
13	1.200	281.0E6
14	1.300	324.2E6
15	1.400	367.7E6
16	1.500	411.0E6
17	1.600	454.2E6
18	1.700	496.9E6
19	1.800	538.8E6
20	1.900	579.4E6
21	2.000	618.4E6

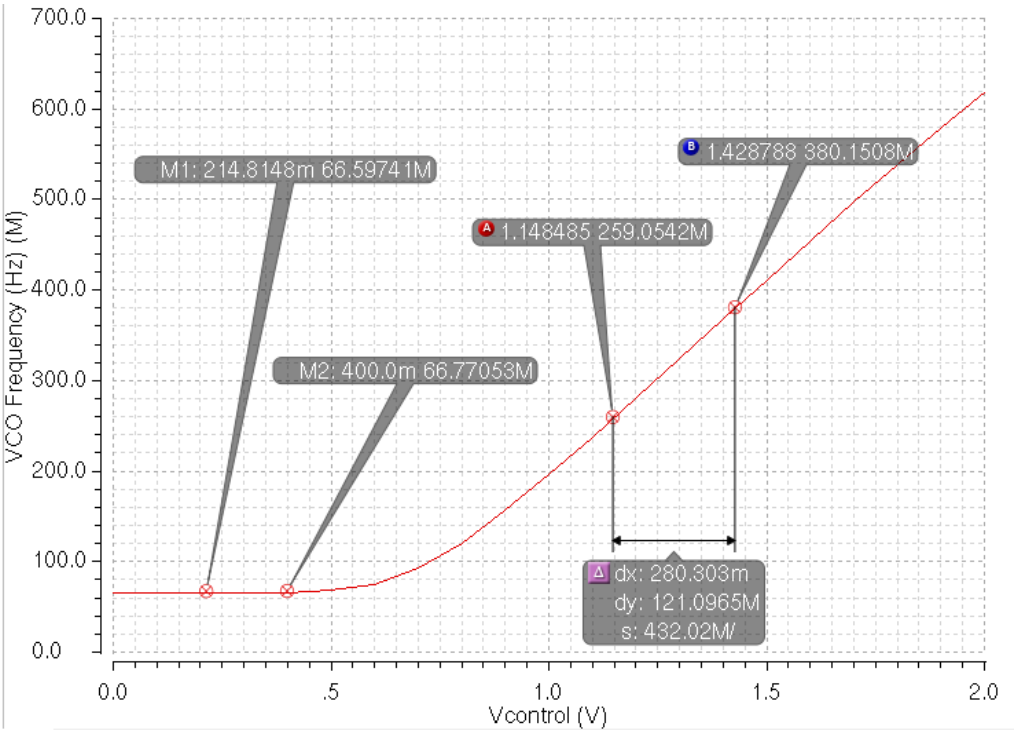


Figure 24. Plot of the VCO output frequency vs control voltage with the first test-bench.

From the results in **Figure 24** using the test-bench on **Figure 21**, the following points can be observed:

- For a $V_{control}$ range between 0V and 0.4V, the VCO output frequency ω_{out} doesn't vary significantly and is between 66.6 MHz and 66.77 MHz.
- For a $V_{control}$ range between 0.5V and 2.0V, f_{out} behaves linearly between 68.42 MHz and 618.4 MHz. This $V_{control}$ range will be the $V_{control}$ tuning range.
- The value of the VCO gain K_{VCO} is 432.02 MHz/V.
- For a $V_{control} = V_{DD} = 2V$, the VCO output frequency ω_{out} is set around 618.4 MHz.

The VCO output frequency range for the first test-bench goes from 68.42 MHz to 618.4 MHz.

Input Frequency Range and PLL Output Frequency Range

From **Figure 24**, it can be pointed out the following:

- A Frequency Divider is located between the input of the PLL and the PFD. The Reference Input at the PFD is the result of dividing the incoming input frequency by N=5.
- So, the incoming frequency is 5 times larger than the frequency being compared at the PFD.
- The Feedback input at the PFD is the VCO output frequency being divided by N=64.
- There is a Frequency Divider that divides the VCO output by 2. This is located within the PLL_160MHZ_MDIV block. The resulting division is the output of the PLL.

To calculate the Input Frequency Range and the PLL Output Frequency Range, the Prescalers have to be included.

The minimum incoming input frequency that the PLL can follow is:

- At Feedback input N=64: (68.42 MHz / 64) = 1.06906 MHz approximately.
- If PLL is locked, the Reference input has to be equal to the feedback: 1.06906 MHz.
- The incoming input frequency will be: (1.06906 MHz * 5) = 5.34531 MHz.

The maximum incoming input frequency that the PLL can follow is:

- At Feedback input N=64: (618.4 MHz / 64) = 9.6656 MHz approximately.
- If PLL is locked, the Reference input has to be equal to the feedback: 9.6656 MHz.
- The incoming input frequency will be: (9.6656 MHz * 5) = 48.328 MHz.

If the Frequency Dividers are included, then input frequency range goes from 1.069 MHz to 48.328 MHz and the resulting PLL output frequency range (where $f_{out} \div 2$) goes from 34.21 MHz to 309.2 MHz, based on a $V_{control}$ tuning range between 0.5V and 2.0V.

Second Test-Bench

The second test-bench, shown back in **Figure 12**, involves the complete PLL circuit used for the assignment.

This time, the approach is different:

For simulation, *Ultrasim* simulator is used instead of *Spectre.* Setting the Analog Design Environment with the settings shown in **Figure 25,** a Parametric Analysis is being run by sweeping the PLL input frequency fREF from 1MHz to 52MHz in steps of 1MHz.

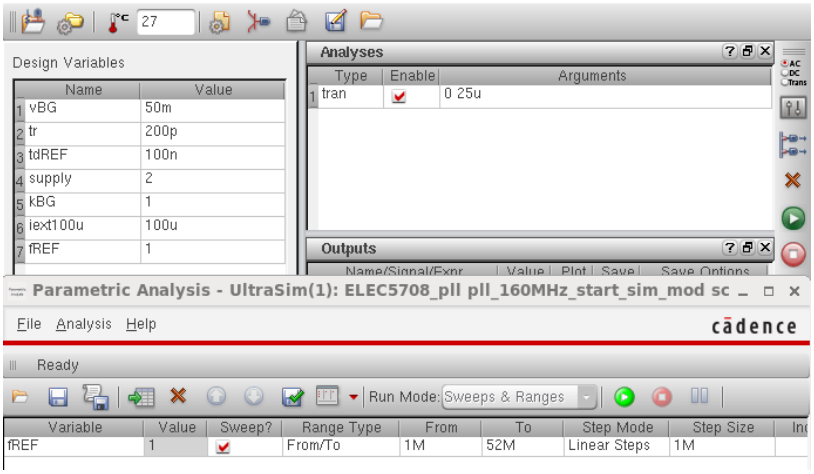


Figure 25. ADE settings for the second test-bench to find the VCO frequency range.

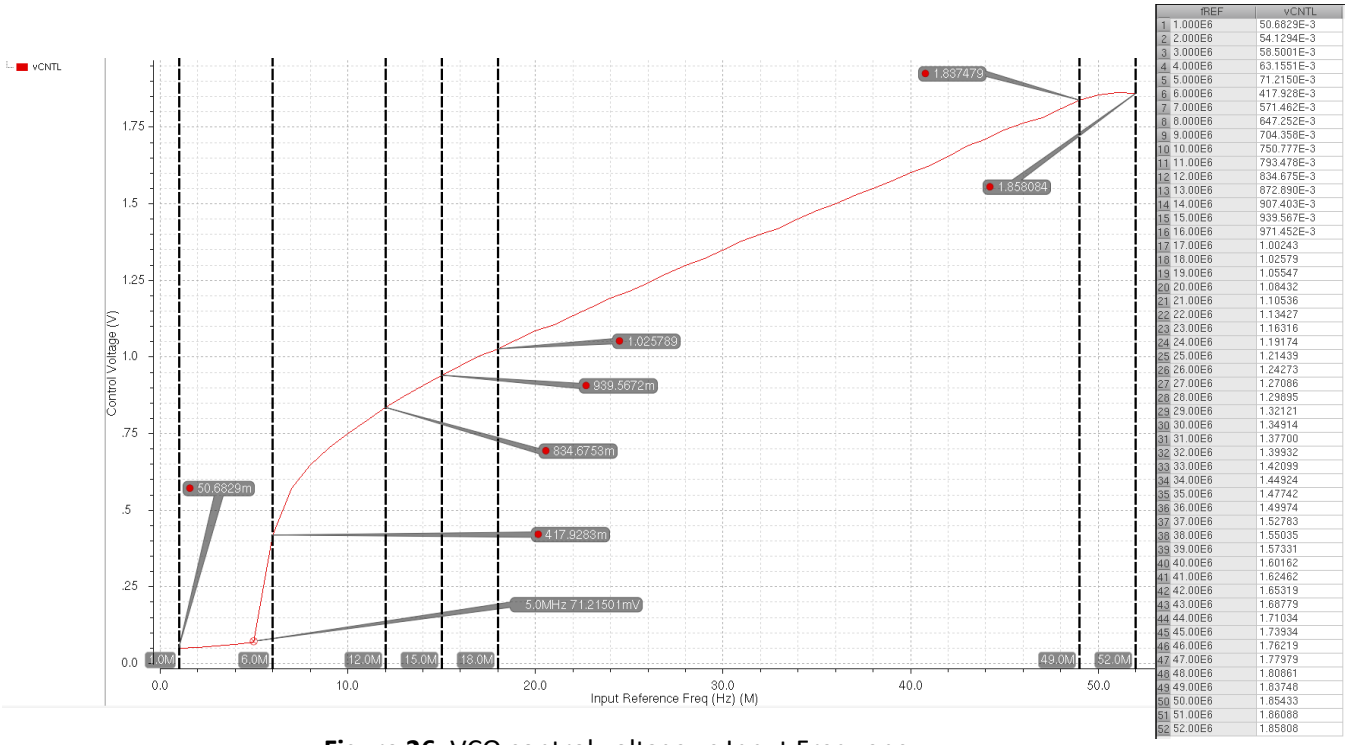
The simulation will generate a family of waveforms for the selected nodes, 52 waveforms for each node. Each waveform is referred to the input frequency parameter fREF (input frequency coming from outside the PLL). The focus right now is over the VCO_CLK and vCNTL nodes.

Taking the average of the family of waveforms for vCNTL will generate a curve of Vcontrol vs Input Frequency as shown in **Figure 26**, with the following command in the Calculator:

```
average(getData("/I3/vCNTL" ?result "tran"))
```

Also, **Figure 27** shows the plot of the VCO output frequencies vs Input Frequency with the following command in the Calculator:

```
frequency(getData("/I3/I13_VCO_CLK" ?result "tran"))
```



	tREF	vCNTL
1	1.000E6	50.6829E-3
2	2.000E6	54.1294E-3
3	3.000E6	58.5001E-3
4	4.000E6	63.1551E-3
5	5.000E6	71.2150E-3
6	6.000E6	417.928E-3
7	7.000E6	571.462E-3
8	8.000E6	647.252E-3
9	9.000E6	704.358E-3
10	10.00E6	750.777E-3
11	11.00E6	793.478E-3
12	12.00E6	834.675E-3
13	13.00E6	872.890E-3
14	14.00E6	907.403E-3
15	15.00E6	939.567E-3
16	16.00E6	971.452E-3
17	17.00E6	1.00243
18	18.00E6	1.02579
19	19.00E6	1.05547
20	20.00E6	1.08432
21	21.00E6	1.10536
22	22.00E6	1.13427
23	23.00E6	1.16316
24	24.00E6	1.19174
25	25.00E6	1.21439
26	26.00E6	1.24273
27	27.00E6	1.27086
28	28.00E6	1.29895
29	29.00E6	1.32121
30	30.00E6	1.34914
31	31.00E6	1.37700
32	32.00E6	1.39932
33	33.00E6	1.42099
34	34.00E6	1.44924
35	35.00E6	1.47742
36	36.00E6	1.49974
37	37.00E6	1.52783
38	38.00E6	1.55035
39	39.00E6	1.57331
40	40.00E6	1.60162
41	41.00E6	1.62462
42	42.00E6	1.65319
43	43.00E6	1.68779
44	44.00E6	1.71034
45	45.00E6	1.73934
46	46.00E6	1.76219
47	47.00E6	1.77979
48	48.00E6	1.80861
49	49.00E6	1.83748
50	50.00E6	1.85433
51	51.00E6	1.86088
52	52.00E6	1.85808

Figure 26. VCO control voltage vs Input Frequency.

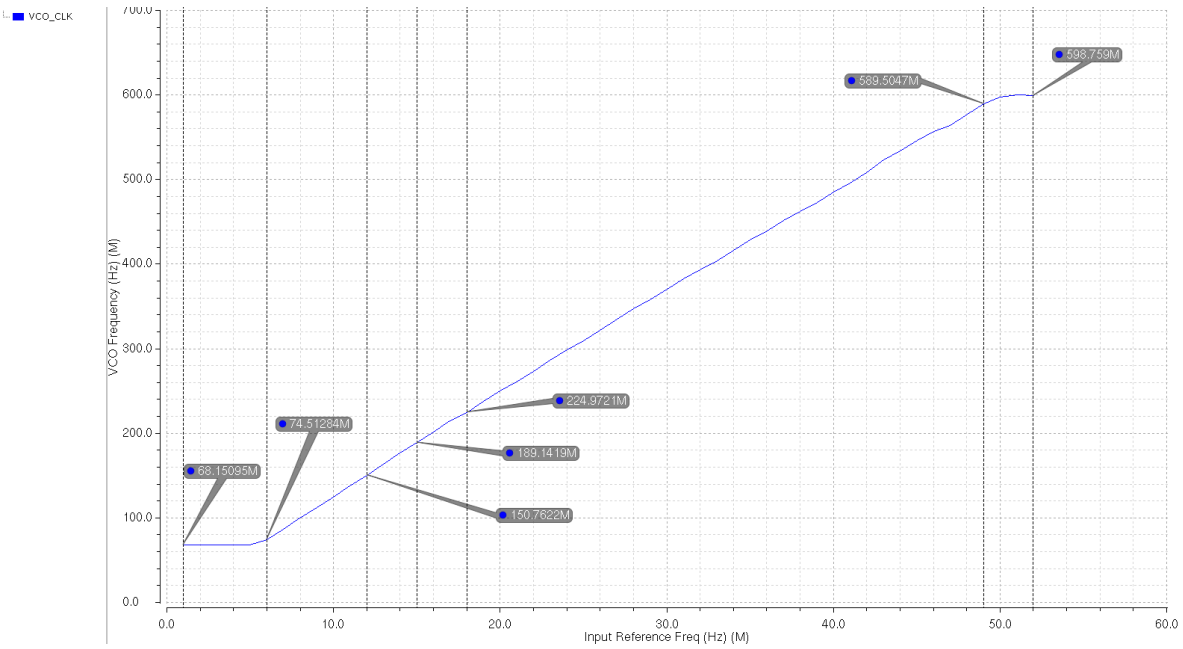
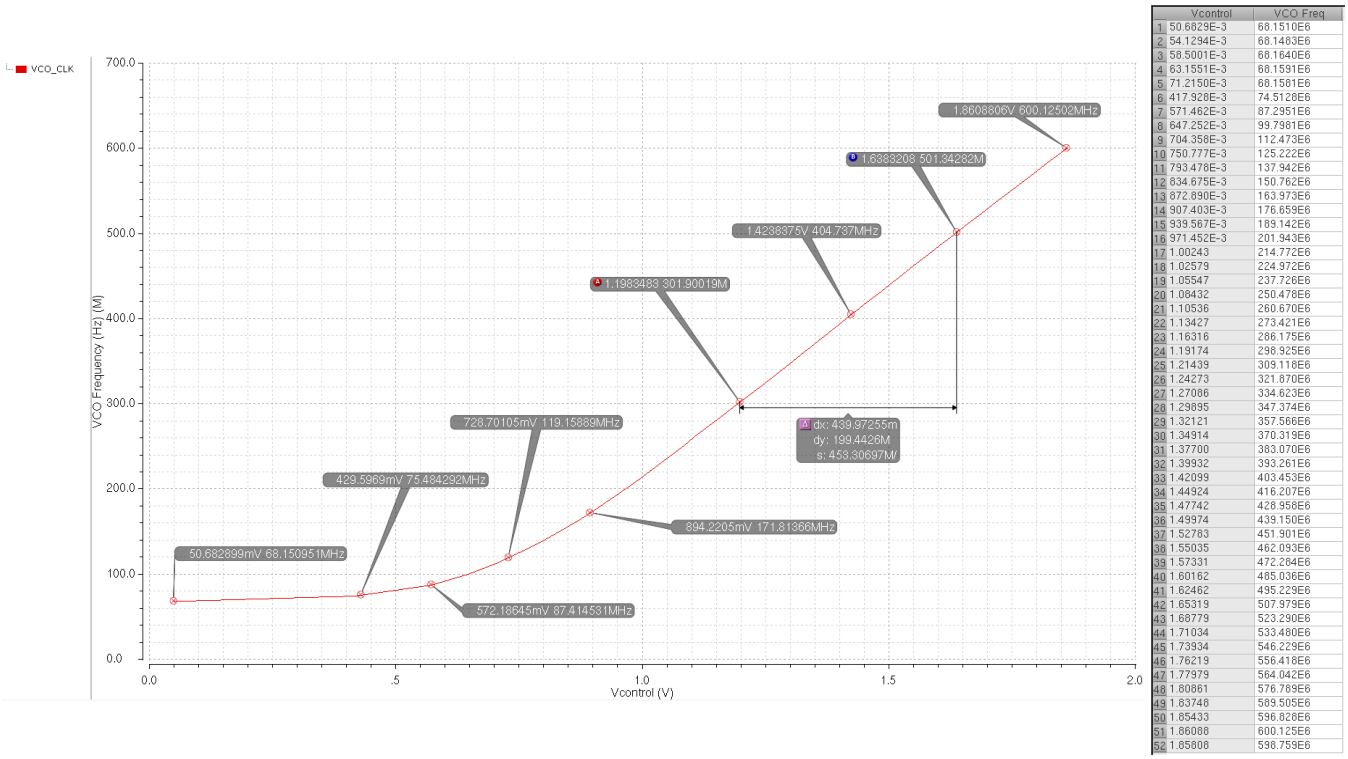


Figure 27. VCO Output Frequency vs Input Frequency.

To find the VCO frequency at a particular control voltage, the two previous plots have to be copied in a new window. Since they share a same axis, Input Reference Frequency, a “Y vs Y” function can be performed. This will generate a new plot in which the y-axis will be a selected y-axis of one plot, and the x-axis will be the y-axis of the other plot (by default). **Figure 28** shows the resulting plot with a table of the values for each point.



	Vcontrol	VCO Freq
1	50.6829E-3	68.1510E6
2	54.1294E-3	68.1483E6
3	58.5001E-3	68.1640E6
4	63.1551E-3	68.1591E6
5	71.2150E-3	68.1581E6
6	417.928E-3	74.5128E6
7	571.462E-3	87.2951E6
8	647.252E-3	99.7981E6
9	704.358E-3	112.473E6
10	750.777E-3	125.222E6
11	793.478E-3	137.942E6
12	834.675E-3	150.762E6
13	872.890E-3	163.973E6
14	907.403E-3	176.659E6
15	939.567E-3	189.142E6
16	971.452E-3	201.943E6
17	1.00243	214.772E6
18	1.02579	224.972E6
19	1.05547	237.726E6
20	1.08432	250.478E6
21	1.10536	260.670E6
22	1.13427	273.421E6
23	1.16316	286.175E6
24	1.19174	298.925E6
25	1.21439	309.118E6
26	1.24273	321.870E6
27	1.27086	334.623E6
28	1.29895	347.374E6
29	1.32121	357.566E6
30	1.34914	370.319E6
31	1.37700	383.070E6
32	1.39932	393.261E6
33	1.42099	403.453E6
34	1.44924	416.207E6
35	1.47742	428.958E6
36	1.49974	439.150E6
37	1.52783	451.901E6
38	1.55035	462.093E6
39	1.57331	472.284E6
40	1.60162	485.036E6
41	1.62462	495.229E6
42	1.65319	507.979E6
43	1.68779	523.290E6
44	1.71034	533.480E6
45	1.73934	546.229E6
46	1.76219	556.418E6
47	1.77979	564.042E6
48	1.80661	576.769E6
49	1.83748	589.505E6
50	1.85433	596.828E6
51	1.86088	600.125E6
52	1.85808	598.759E6

Figure 28. VCO Output Frequency vs Vcontrol.

From the results in **Figure 28**, the following points can be observed:

- For a $V_{control}$ range between 50.68 mV and 71.215 mV, the VCO output frequency ω_{out} doesn't vary linearly and goes from 68.151 MHz to 68.1581 MHz.
- For a $V_{control}$ range between 417.928 mV and 1.83748 V, f_{out} behaves linearly between 74.5128 MHz and 589.505 MHz. This $V_{control}$ range will be the $V_{control}$ tuning range.
- The value of the VCO gain K_{VCO} is 453.3 MHz/V.
- For a $V_{control} = V_{DD} = 1.858V$, the VCO output frequency ω_{out} is set around 589.505 MHz.

The VCO output frequency range for the second test-bench goes from 74.5128 MHz to 589.505 MHz, for a $V_{control}$ tuning range between 417.928 mV and 1.83748 V.

The input frequency range goes from 6 MHz to 49 MHz, and the resulting PLL output frequency range (where $f_{out} \div 2$) goes from 37.2564 MHz to 294.753 MHz.

Parameters	VCO Block only	Complete PLL
Min. f_{out} from VCO	68.42 MHz	74.5128 MHz
Max. f_{out} from VCO	618.4 MHz	589.505 MHz
Min. f_i	5.34531 MHz	6 MHz
Max. f_i	48.328 MHz	49 MHz
Min. f_{out} from PLL	34.21 MHz	37.2564 MHz
Max. f_{out} from PLL	309.2 MHz	294.753 MHz
Gain K_{VCO}	432.02 MHz/V	453.3 MHz/V
Min. $V_{control}$ (tuning)	0.5 V	417.928 mV
Max. $V_{control}$ (tuning)	2.0 V	1.83748 V
VCO free-running frequency f_o	66.6MHz	68.15 MHz

Table 3. Comparison of the result from both simulations.

Locking Range

To find the locking range, first the PLL has to acquire lock condition, and then move the input frequency to see if the PLL can acquire lock at the new frequency.

The test-bench is shown in **Figure 29**, where the input signal is composed by an odd number of ideal current pulse sources connected to the input node and a resistor as a load. The output will be in volts.

Starting with two current sources, they will run one after the other separated by some delay. They will have the same frequency, but they will be 180° apart. This will produce an output of zero just when the second current source starts.

The next current source will start exactly at the same time as the second current source, showing only the signal of the newest current source for some delay until another current signal, with the same frequency and a phase shift of 180°, adds up with the previous signal. The settings are shown in **Figure 30**.

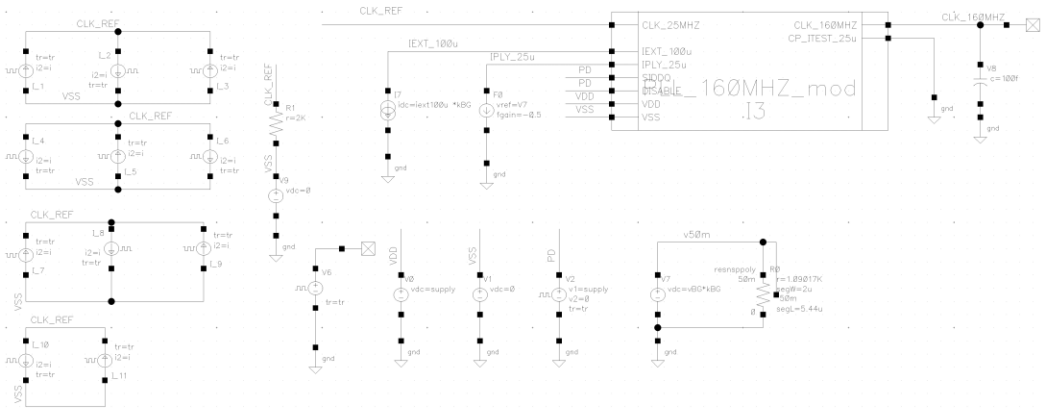


Figure 29. Test-bench to prove the Locking Range.

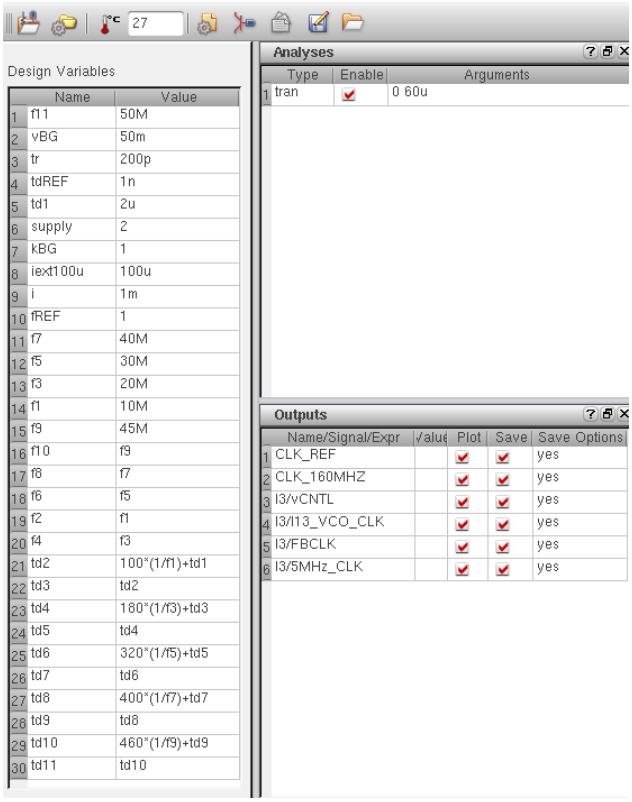


Figure 30. Settings for the Locking Range test-bench.

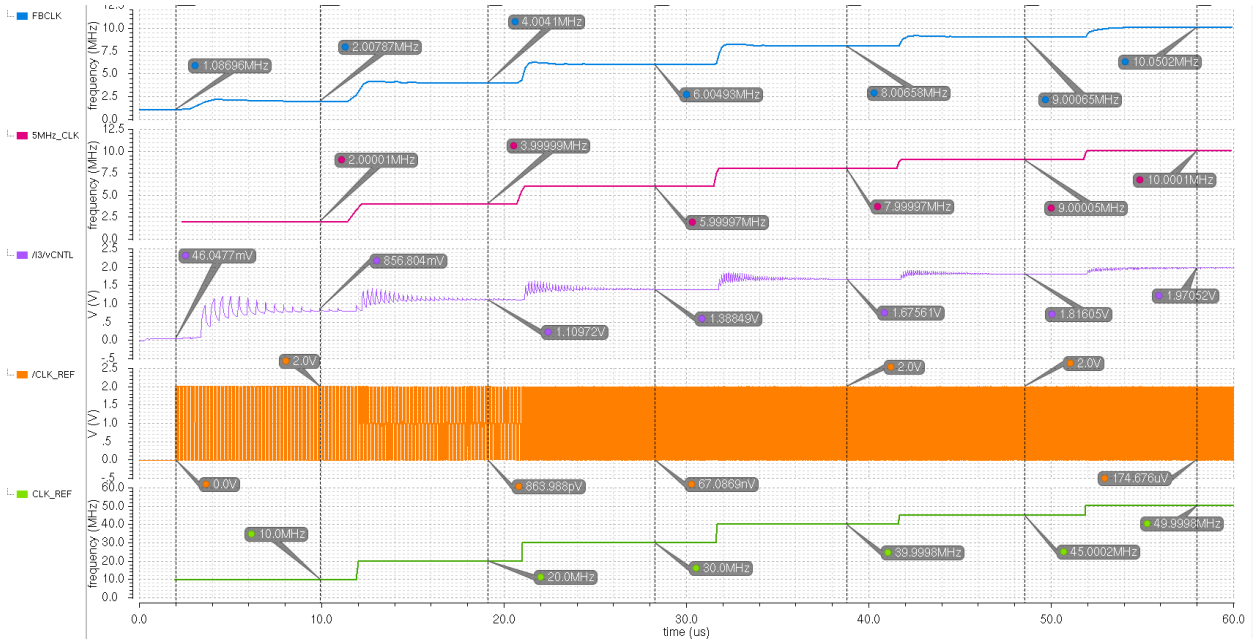


Figure 31. Plot of the different nodes for an input range between 10 MHz and 50 MHz.

The plot in **Figure 31** shows that the PLL can acquires lock condition for an input frequency of 10 MHz, and follows the input signal for subsequent input frequency changes up to 50 MHz. This means that it can lock 1 MHz more than previously established as for 49 MHz.

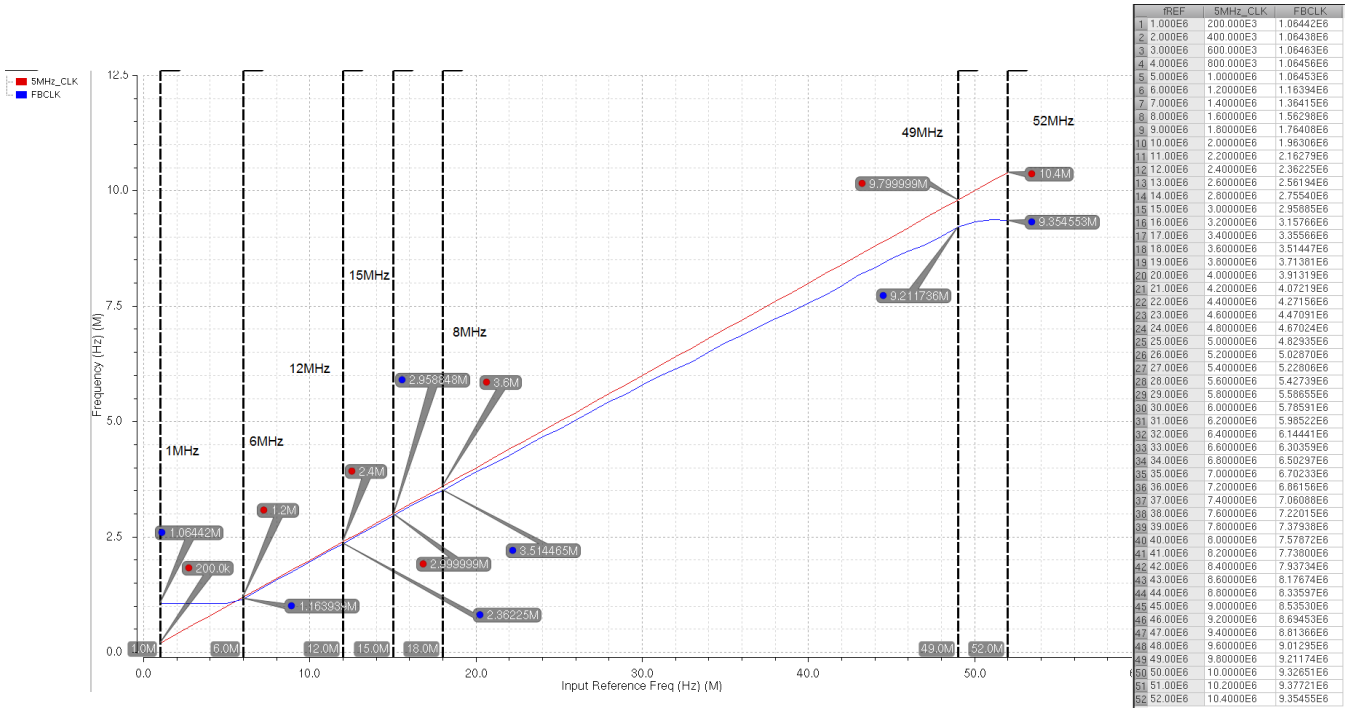
It is concluded that the locking range goes from 6 MHz up to 50 MHz.

Frequency Range (Capture Range)

To find the frequency range, a range of input frequencies is applied (one per simulation) while the VCO runs at free-running frequency and see at which frequencies the PLL can acquire lock.

From the simulation of the Complete PLL circuit done in the "VCO Frequency Range – Second Test-Bench" section, the input frequency -after the prescaler (5MHz_CLK)- and the feedback (FBCLK) are plotted vs the input reference frequency. The plot is shown in **Figure 32**.

A parametric analysis is done by sweeping the input frequency from 1 MHz up to 50 MHz, and observing at which frequencies the PLL acquires lock.



	fREF	5MHz_CLK	FBCLK
1	1.000E6	200.000E3	1.06442E6
2	2.000E6	400.000E3	1.06438E6
3	3.000E6	600.000E3	1.06463E6
4	4.000E6	800.000E3	1.06456E6
5	5.000E6	1.00000E6	1.06453E6
6	6.000E6	1.20000E6	1.16394E6
7	7.000E6	1.40000E6	1.36415E6
8	8.000E6	1.60000E6	1.56298E6
9	9.000E6	1.80000E6	1.76408E6
10	10.00E6	2.00000E6	1.96306E6
11	11.00E6	2.20000E6	2.16279E6
12	12.00E6	2.40000E6	2.36225E6
13	13.00E6	2.60000E6	2.56194E6
14	14.00E6	2.80000E6	2.75540E6
15	15.00E6	3.00000E6	2.95885E6
16	16.00E6	3.20000E6	3.15766E6
17	17.00E6	3.40000E6	3.35566E6
18	18.00E6	3.60000E6	3.51447E6
19	19.00E6	3.80000E6	3.71381E6
20	20.00E6	4.00000E6	3.91319E6
21	21.00E6	4.20000E6	4.07219E6
22	22.00E6	4.40000E6	4.27156E6
23	23.00E6	4.60000E6	4.47091E6
24	24.00E6	4.80000E6	4.67024E6
25	25.00E6	5.00000E6	4.82935E6
26	26.00E6	5.20000E6	5.02870E6
27	27.00E6	5.40000E6	5.22806E6
28	28.00E6	5.60000E6	5.42739E6
29	29.00E6	5.80000E6	5.58655E6
30	30.00E6	6.00000E6	5.78591E6
31	31.00E6	6.20000E6	5.98522E6
32	32.00E6	6.40000E6	6.14441E6
33	33.00E6	6.60000E6	6.30359E6
34	34.00E6	6.80000E6	6.50297E6
35	35.00E6	7.00000E6	6.70233E6
36	36.00E6	7.20000E6	6.86156E6
37	37.00E6	7.40000E6	7.06088E6
38	38.00E6	7.60000E6	7.22015E6
39	39.00E6	7.80000E6	7.37938E6
40	40.00E6	8.00000E6	7.57872E6
41	41.00E6	8.20000E6	7.73800E6
42	42.00E6	8.40000E6	7.93734E6
43	43.00E6	8.60000E6	8.17674E6
44	44.00E6	8.80000E6	8.33597E6
45	45.00E6	9.00000E6	8.53530E6
46	46.00E6	9.20000E6	8.69453E6
47	47.00E6	9.40000E6	8.81366E6
48	48.00E6	9.60000E6	9.01295E6
49	49.00E6	9.80000E6	9.21174E6
50	50.00E6	10.0000E6	9.32651E6
51	51.00E6	10.2000E6	9.37721E6
52	52.00E6	10.4000E6	9.35455E6

Figure 32. VCO Output Frequency vs Vcontrol.

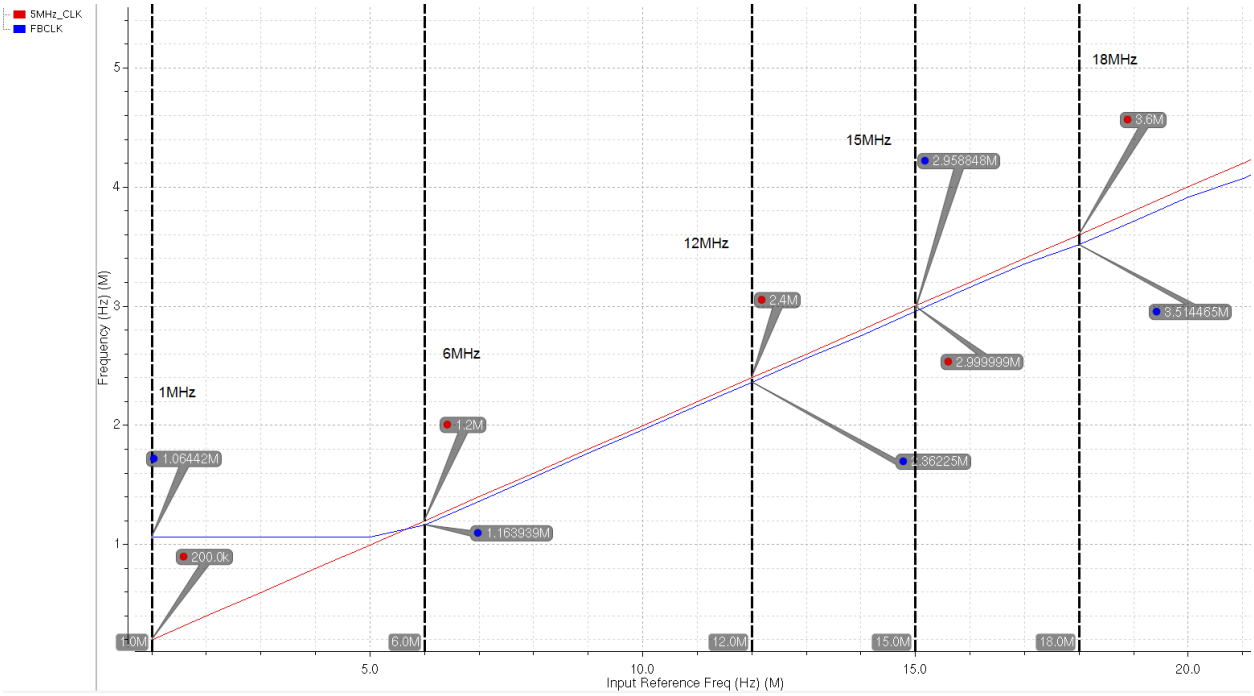


Figure 33. Zoomed portion of the plot in Figure 18.

From **Figure 33**, it seems that the PLL acquires lock, maintaining a "constant" frequency difference around 40 KHz, for an input frequency range from 6 MHz to 17 MHz.

Beyond 17 MHz, the PLL tries to lock with the Input Frequency but with an increasing phase difference, until it reaches the point it cannot follow it anymore (around 49 MHz), showing almost no increase in frequency as seen in **Figure 32**.

It can be concluded that the PLL can acquire lock for a frequency range that goes from 6 MHz to 49 MHz.

Plots of $V_{control}$, Feedback and "prescaled" Input Frequency for different Input Frequencies are shown from **Figure 34** to **Figure 40**. These plots show the time (phase) shift between the PFD inputs at those particular input frequencies.

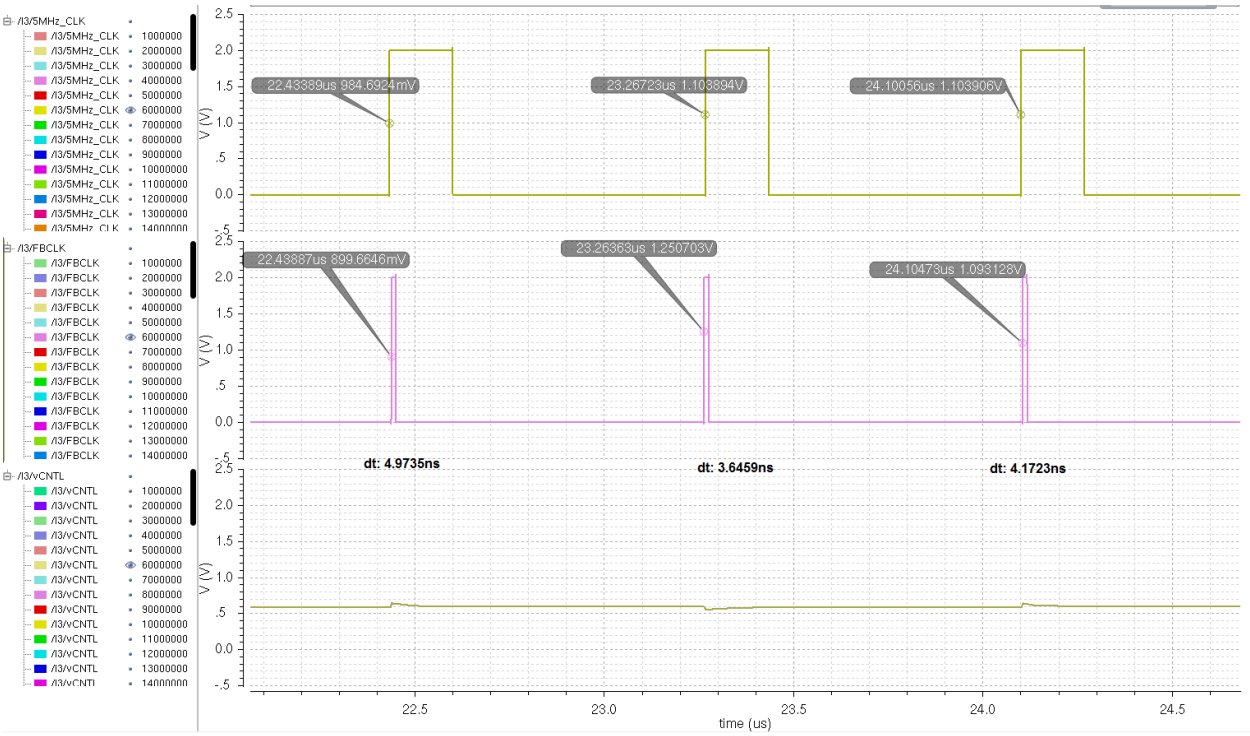


Figure 34. Phase difference plot for an input frequency of 6 MHz after 25µs of simulation.

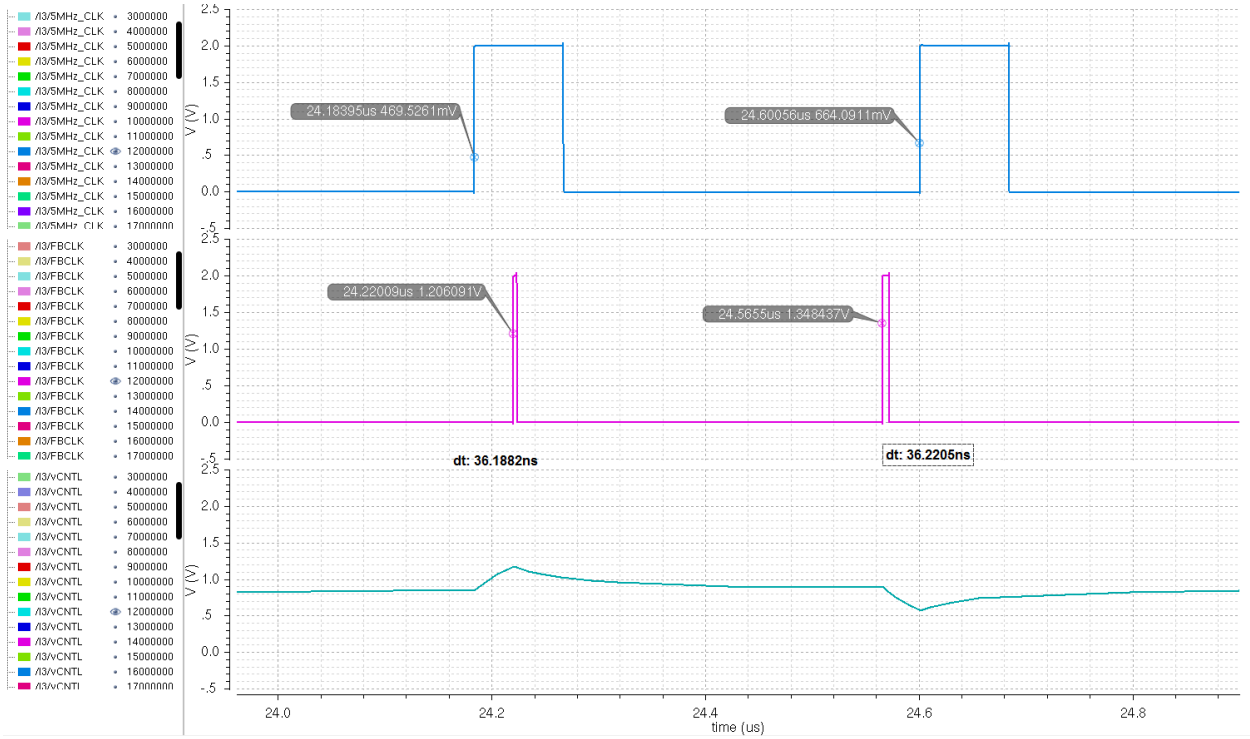


Figure 35. Phase difference plot for an input frequency of 12 MHz after 25µs of simulation.

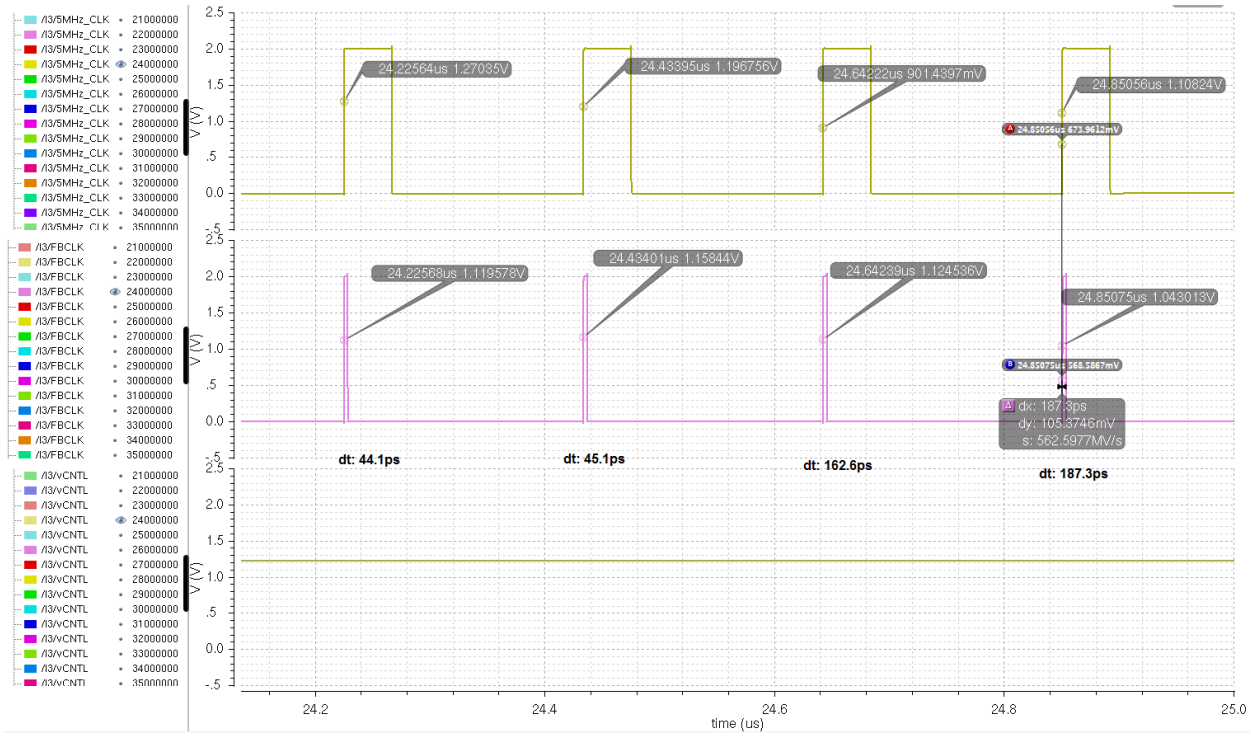


Figure 36. Phase difference plot for an input frequency of 24 MHz after 25µs of simulation.

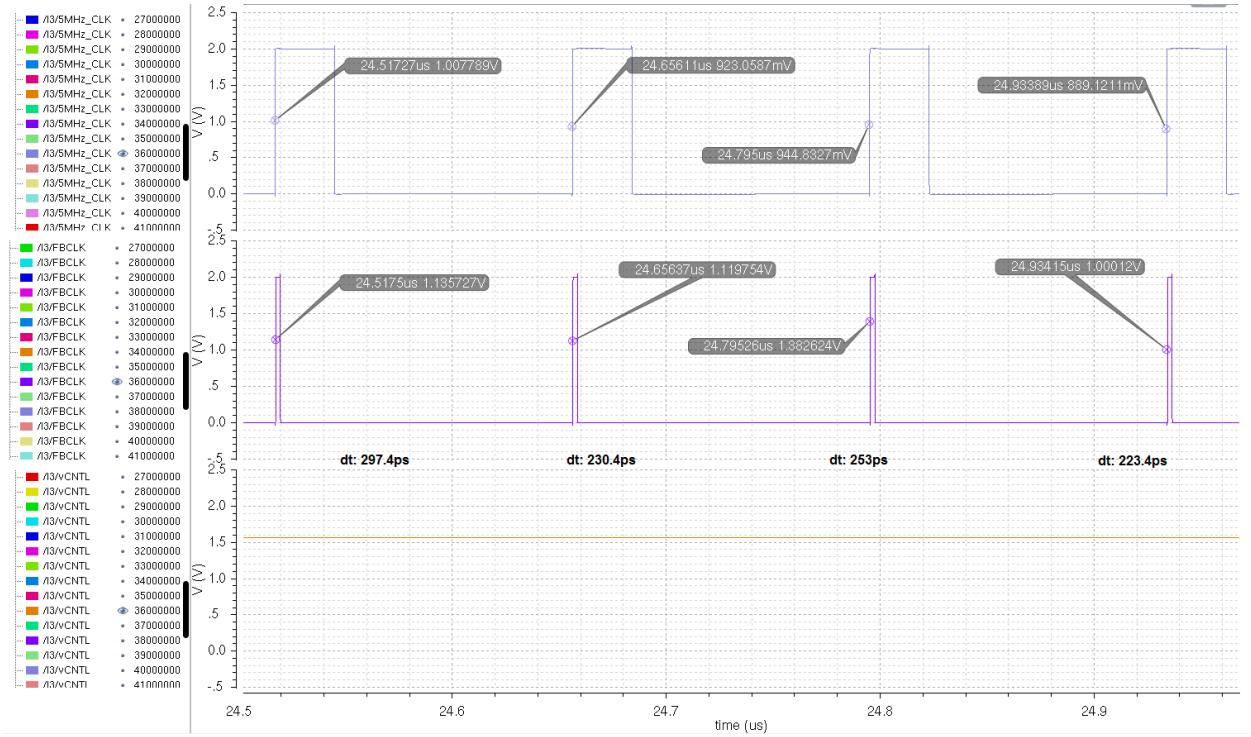


Figure 37. Phase difference plot for an input frequency of 36 MHz after 25µs of simulation.

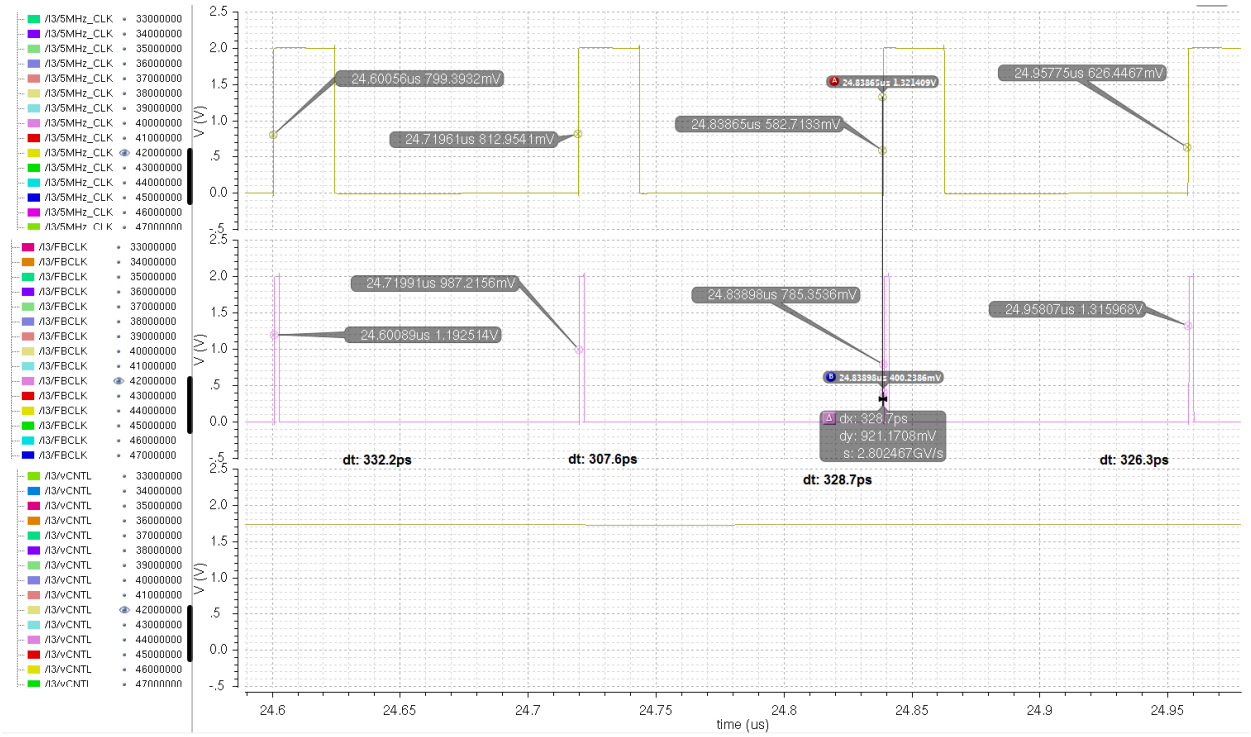


Figure 38. Phase difference plot for an input frequency of 42 MHz after 25µs of simulation.

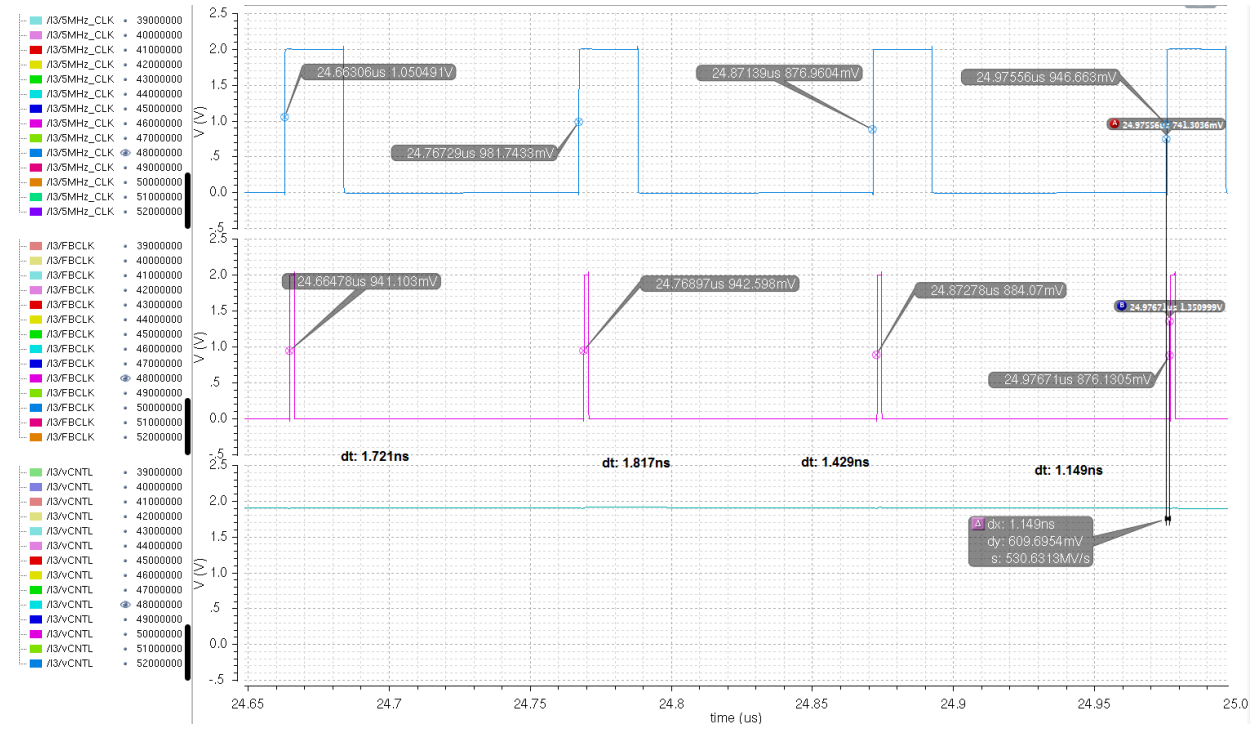


Figure 39. Phase difference plot for an input frequency of 48 MHz after 25µs of simulation.

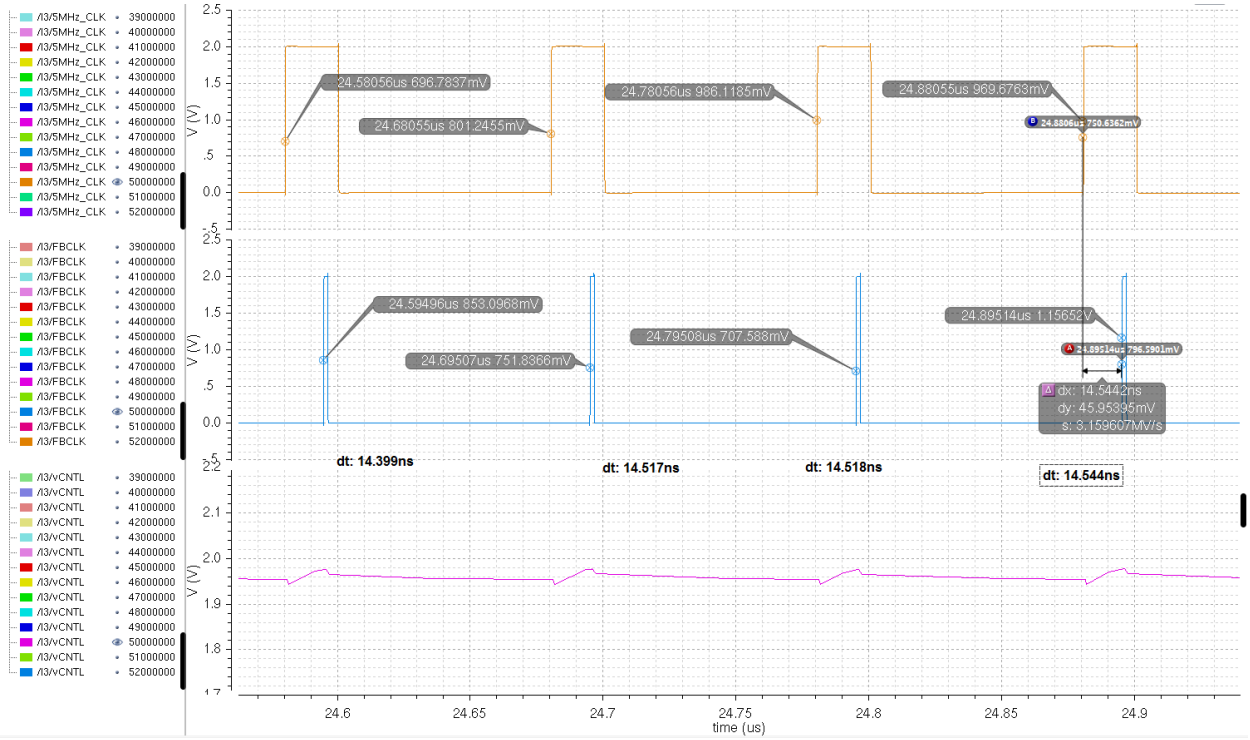


Figure 40. Phase difference plot for an input frequency of 50 MHz after 25µs of simulation.

Using the following formula to calculate the phase difference between the two signals, assuming they are "equal" in frequency since the PLL has acquired lock condition:

$$\Delta\varphi = 2\pi \cdot f \cdot \Delta t \qquad (10)$$

The phase shift $\Delta\varphi$ has to be smaller than a full period, or 2π. This means that the factor $f \cdot \Delta t$ has to be smaller than $\frac{1}{2\pi}$.

Here, the frequency is divide by 5 since it is the frequency coming from the input prescaler, which happens to be "the same" as the feedback.

$$\Delta\varphi = 2\pi \cdot \frac{f}{5} \cdot \Delta t \qquad (11)$$

Plots	f	Δt	$\Delta\varphi$	**PLL Locked**
Figure 34	6 MHz	4.9735 ns	0.037499rad	True
Figure 35	12 MHz	36.22 ns	0.546185 rad	True
Figure 36	24 MHz	187.3 ps	0.005649 rad	True
Figure 37	36 MHz	253 ps	0.011445 rad	True
Figure 38	42 MHz	328.7 ps	0.017348 rad	True
Figure 39	48 MHz	1.429 ns	0.086195 rad	True
Figure 40	50 MHz	14.518 ns	0.91219 rad	True

Table 4. Calculation of phase shift for different input frequencies to verify lock condition.

Loop Filter Bandwidth

The following formula describes the loop filter transfer function:

$$LF(s) = K_{PD} \cdot F(s)$$

Since C_2 is rated to be very small compared to C_1, it can be neglected, and the loop filter bandwidth can be approximated to the following equation:

$$\omega_1 = \omega_{3dB} = \frac{1}{RC_1}$$

Having $R = 29.9959\ K\Omega$ and $C_1 = 44.0256\ pF$:

$$\omega_{3dB} = \frac{1}{RC_1} = \frac{1}{(29.9959\ K\Omega)(44.0256\ pF)} = \ 757.2387\ Krad/s$$

$$f_{3dB} = \frac{\omega_{3dB}}{2\pi} = 120.518\ KHz$$

Power consumption

The Power Consumption can be measured from the power supply VDD, and it will be considered as the average power consumed during the time of a simulation.

Also, it is measured at two processing corners: TT (or NN) at 27 °C, and FF at 85 °C.

Process Corner: Typical-Typical @ 27 °C

The settings are shown in **Figure 40** for the Typical-Typical process corner at 27 °C

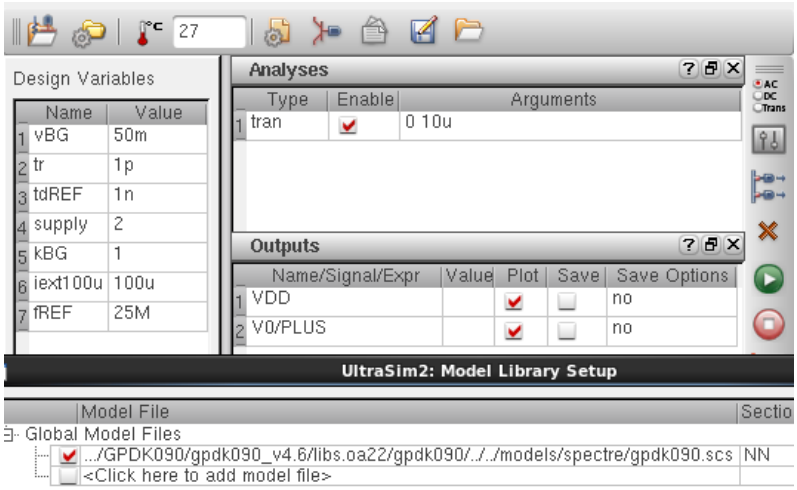


Figure 40. Analog Design Environment settings for the TT (NN) process corner.

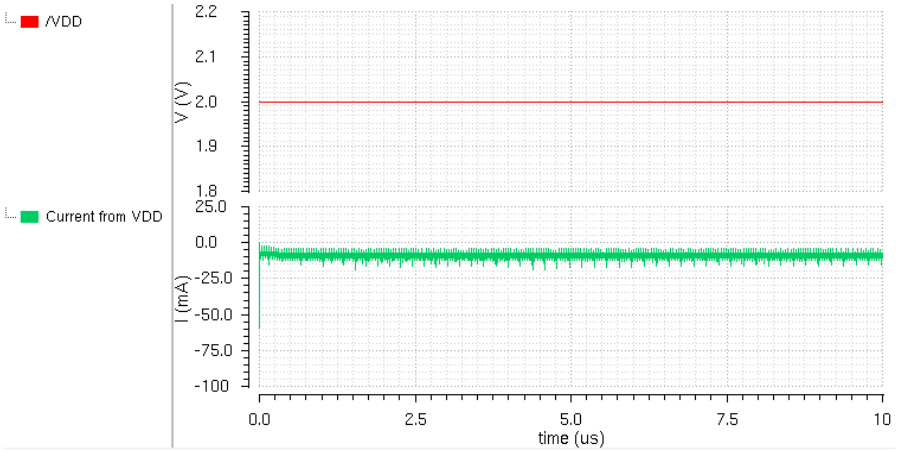


Figure 41. Plot of the transient current from VDD.

The power can be calculated using the following command on the Calculator:

```
average(v("/VDD" ?result "tran"))*average(i("V0.p" ?result "tran"))
```

The power consumption measured was 16.295 mW.

Process Corner: Fast-Fast @ 85 °C

The settings are shown in **Figure 42** for the Fast-Fast process corner at 85 °C

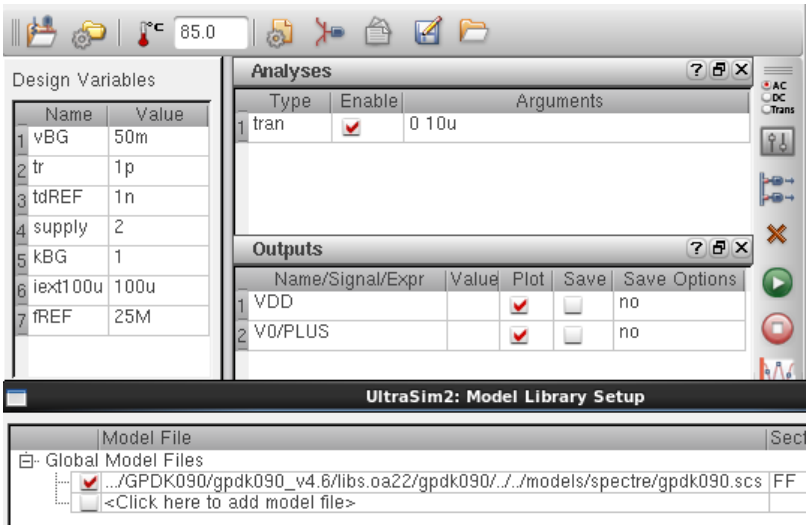


Figure 42. Analog Design Environment settings for the TT (NN) process corner.

The power consumption measured was 16.917 mW.

Assignment 2 ELEC 5708: ASIC for Telecommunications Carleton University November 3, 2014

Sergio Espinal 100926721

Phase-Locked Loop

Description

The assignment consist on simulating a pre-designed Phase-Locked Loop, based on the **90 nm Generic Process Kit** from Cadence, following the tutorial file named "***PLL_Tutorial***" located at Reference **[1]**.

The software package is ***StartCDS5b101***.

Results

Ether library cellviews	**Description**
PLL_160_MHZ	PLL circuit
PLL_160MHZ_LF	Low-Pass Filter
PLL_160MHZ_PDIV	Input Prescaler
PLL_160MHZ_MDIV	Output Prescaler
PLL_CP	Charge Pump
PLL_PFD	Phase Frequency Detector
VCO_320MHZ	Voltage Controlled Oscillator

Ether_sim library cellviews	**Description**
pll_160MHz_start_sim	PLL circuit testbench
pll_pfd_cplf_sim	PFD, CP and LPF testbench
pll_pfd_sim	PFD testbench
pll_vco_320MHz_sim	VCO testbench

Table 1. Cellviews used from *ether* and *ether_sim* libraries.

Process Corner	**Power Consumption**	**Reference**
Typical-Typical @ 27 °C	16.295 mW	Pg. 30
Fast-Fast @ 85 °C	16.917 mW	Pg. 30

Table 2-a. PLL parameters for the assignment.

Parameter	Value	Reference
Rise and Fall time	200 ps	Pg. 11
Frequency Range	6 MHz - 50 MHz	Pg. 24
Locking Range	6 MHz - 50 MHz	Pg. 23
Deadzone (lead)	90 ps	Pg. 12
Deadzone (lag)	116.3 ps	Pg. 13
Loop Filter Bandwidth	120.518 KHz	Pg. 29

Table 2-b. PLL parameters for the assignment.

Parameters	Value	Reference
Min. f_{out} from VCO	74.5128 MHz	Pg. 21
Max. f_{out} from VCO	598.759 MHz	Pg. 21
Min. f_i	5.82131 MHz	Pg. 21
Max. f_i	46.778 MHz	Pg. 21
Min. f_{out} from PLL	37.2564 MHz	Pg. 21
Max. f_{out} from PLL	299.38 MHz	Pg. 21
Gain K_{VCO}	453.3 MHz/V	Pg. 21
Min. $V_{control}$ (tuning)	417.928 mV	Pg. 21
Max. $V_{control}$ (tuning)	1.858 V	Pg. 21
VCO free-running frequency f_o	68.15 MHz	Pg. 21

Table 3. Comparison of the result from both simulations.

Plots	f_{in}	Δt	$\Delta \varphi$	PLL Locked
Figure 34	6 MHz	4.9735 ns	0.037499rad	True
Figure 35	12 MHz	36.22 ns	0.546185 rad	True
Figure 36	24 MHz	187.3 ps	0.005649 rad	True
Figure 37	36 MHz	253 ps	0.011445 rad	True
Figure 38	42 MHz	328.7 ps	0.017348 rad	True
Figure 39	48 MHz	1.429 ns	0.086195 rad	True
Figure 40	50 MHz	14.518 ns	0.91219 rad	True

Table 4. Calculation of phase shift for different input frequencies to verify lock condition.

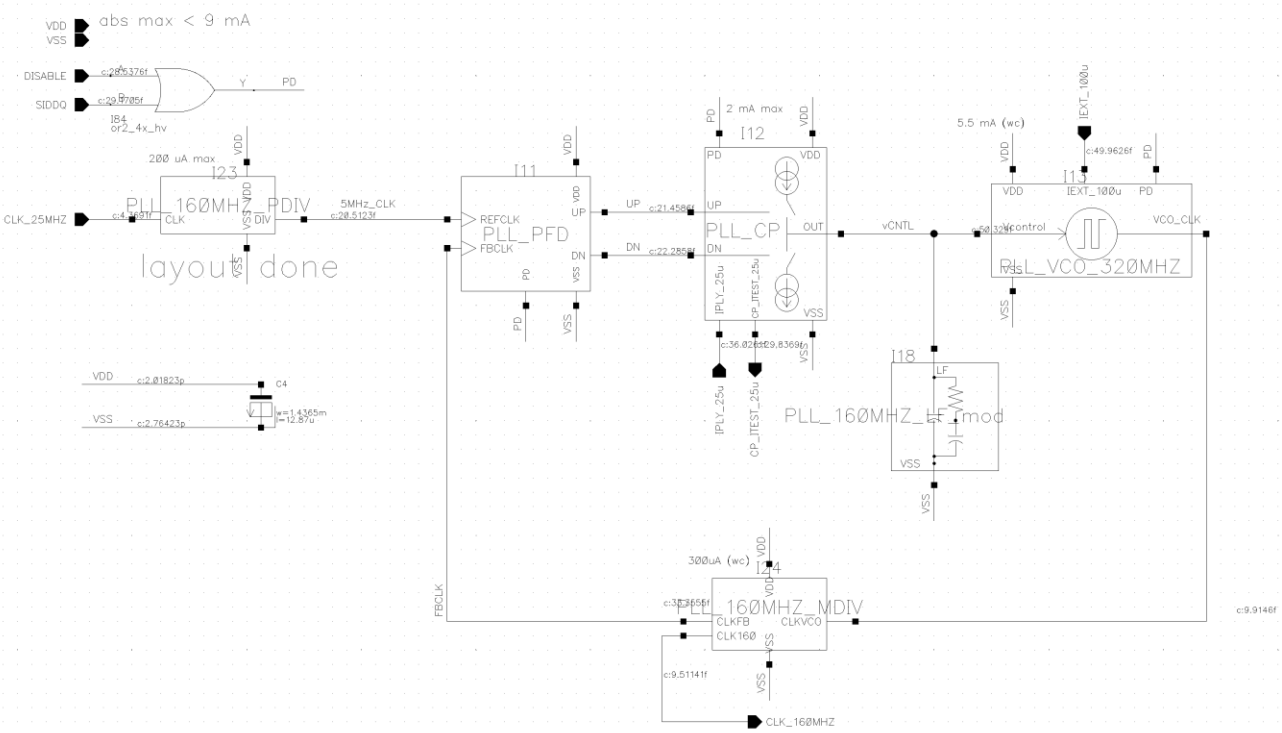


Figure A. The modified circuit of the PLL.

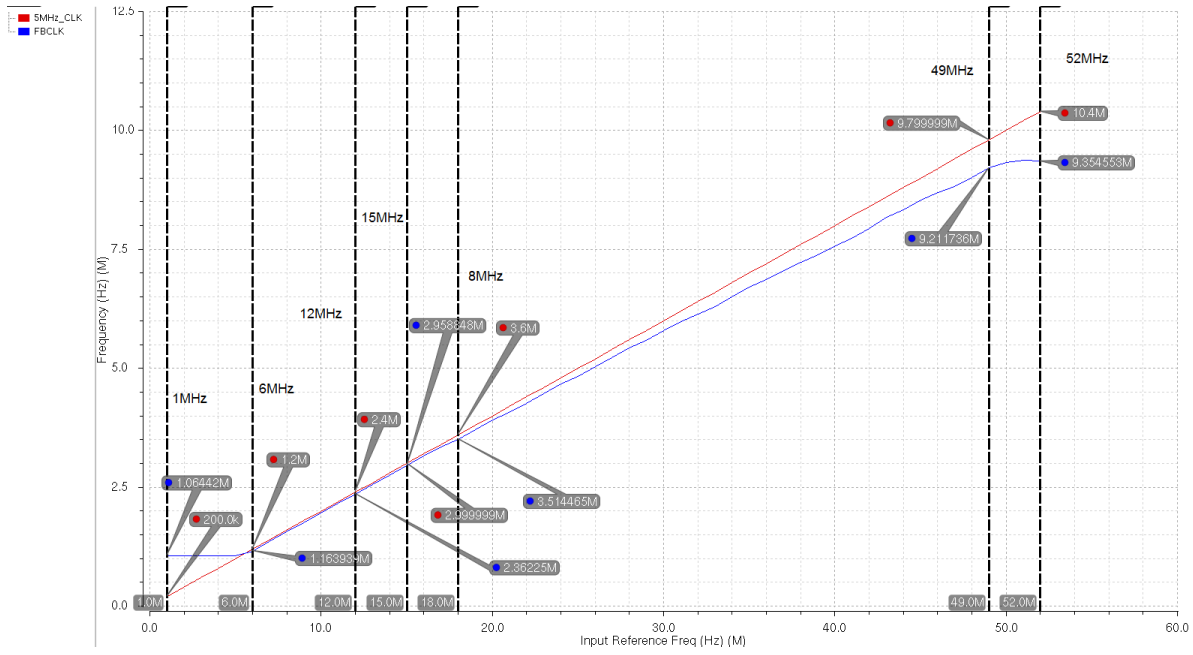


Figure B. VCO Output Frequency vs Vcontrol.

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