ELEC5509 Integrated Circuit Technology

Prof. N. Garry Tarr

Design Project:

3-week CMOS

Stage 1

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Sergio Raul Espinal Lopez

Carleton Id: 100926721

Carleton University

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Overview

The first stage of this project involves device designing to determine the gate oxide thickness, gate doping type, Silicon film thickness, and doping concentration to provide useful nMOS and pMOS device characteristics. This will begin with hand calculations which are refined through MINIMOS simulation.

Procedure

Hand Calculations

A1. Suppose the potential drop across the Si film is $2\phi_B$. What is the maximum film doping consistent with the complete depletion of the 200 nm thick film?

$N_A = \ ?$, where

$$V_{thermal} = \frac{kT}{q} = \frac{\left(1.3809 \times 10^{-23}\ C \cdot \frac{V}{^\circ K}\right)(300^\circ K)}{1.602 \times 10^{-19}\ C} = 0.02586\ V$$

$$n_i = 1.45 \times 10^{10} cm^{-3} = 1.45 \times 10^{16} m^{-3}$$

$$\chi_{depletion} = \sqrt{\frac{2\epsilon_{Si}\psi_{Si}}{qN_A}} \quad \rightarrow \quad \chi_{depletion} = \sqrt{\frac{2\epsilon_{Si}(2\phi_B)}{qN_A}}$$

$$\chi_{depletion} = \sqrt{\frac{4 \cdot (1.03368 \times 10^{-10} F/m\ )(0.02586\ V\ ) \cdot \ln(N_A\ /\ 1.45 \times 10^{16}\ m^{-3})}{(\ 1.602 \times 10^{-19}\ C\ )(N_A)}}$$

To solve this, it was used several doping concentrations, yielding several Si film thickness values, until one concentration was close enough for the complete depletion of the Si film thickness, which is $\chi_{depletion} = 200nm$.

$N_A = \ 2.40567 \times 10^{16} cm^{-3}$, for a Si film thickness of $2.0000019747920000007 \times 10^{-7} m$

A2. The textbook equation for threshold voltage given in the "MOSFET physics" notes doesn´t apply for FDSOI since the charge in the depleted silicon film is much smaller than it would be in a bulk device. Other approaches must therefore be used to estimate V_T. Suppose the nMOS device has an n+ poly gate and a very lightly doped Si film. With this very light well doping, suppose there is no electric field in the gate oxide at threshold. Estimate the gate bias which must be applied to produce a **surface electron concentration** of $10^{16} cm^{-3}$ (a reasonable value of threshold).

Using the following equations, and taking the Energy Band diagram for the n+ poly gate with n- substrate shown in **Figure 1** as reference, we proceed to solve:

$V_{FB} = \phi_{MS} = \phi_M - \phi_S$	$\phi_S = \chi_S + \frac{E_g}{2q} - \phi_B$ n-type
$E_i = \frac{E_g}{2q} = 0.56\ V$	$n_{surface} = n_i \cdot e^{(\phi_B)q/kT}$

$$n_{surface} = n_i \cdot e^{(\phi_B)q/kT} \quad \rightarrow \quad \phi_B = \frac{kT}{q} \ln\left(\frac{n_{surf}}{n_i}\right)$$

$$\phi_B = (0.02586\ V) \cdot \ln\left(\frac{1 \times 10^{16} cm^{-3}}{1.45 \times 10^{10} cm^{-3}}\right) = 0.3495\ V$$

$$V_{FB} = \phi_M - \left(\chi_S + \frac{E_g}{2q} - \phi_B\right) = \phi_M - \chi_S - \frac{E_g}{2q} + \phi_B \quad for\ n^- type\ sub$$

$$if\ \chi_S \approx \phi_M, \qquad V_{FB} = -\frac{E_g}{2q} + \phi_B$$

$$V_{Tn} = V_{FB} = -\frac{E_g}{2q} + \phi_B = -0.56\ V + (0.3495\ V) = -0.2105\ V$$

A3. The pMOS device could have either an n+ poly gate, or a p+ poly gate. For both cases, assuming no electric field in the oxide, **estimate the gate bias** which must be applied to produce a **surface hole concentration** of $10^{16} cm^{-3}$.

Having an n+ poly gate with a p-substrate as shown in **Figure 2**, the gate bias will be:

$V_{FB} = \phi_{MS} = \phi_M - \phi_S$	$\phi_S = \chi_S + \frac{E_g}{2q} + \phi_B$ p-type
$E_i = \frac{E_g}{2q} = 0.56\ V$	$p_{surface} = n_i \cdot e^{-(\phi_B)q/kT}$
$\frac{E_g}{q} = 1.12\ V$	

$$p_{surface} = n_i \cdot e^{(\phi_B)q/kT} \quad \rightarrow \quad \phi_B = \frac{kT}{q} \ln\left(\frac{p_{surf}}{n_i}\right)$$

$$\phi_B = -(0.02586\ V) \cdot \ln\left(\frac{1 \times 10^{16} cm^{-3}}{1.45 \times 10^{10} cm^{-3}}\right) = -0.3495\ V$$

$$V_{FB} = \phi_M - \left(\chi_S + \frac{E_g}{2q} + \phi_B\right) = \phi_M - \chi_S - \frac{E_g}{2q} - \phi_B$$

$$if\ \phi_M \approx \chi_S, \qquad V_{FB} = -\frac{E_g}{2q} - \phi_B$$

$$V_{Tp} = V_{FB} = -\frac{E_g}{2q} - \phi_B = -0.56\ V - (-0.3495\ V) = -0.2105\ V$$

Having a p+ poly gate with p-substrate as shown in **Figure 3**, the gate bias will be:

$V_{FB} = \phi_{MS} = \phi_M - \phi_S$	$\phi_S = \chi_S + \frac{E_g}{2q} + \phi_B$ p-type
$E_i = \frac{E_g}{2q} = 0.56\ V$	$p_{surface} = n_i \cdot e^{-(\phi_B)q/kT}$
$\frac{E_g}{q} = 1.12\ V$	

$$p_{surface} = n_i \cdot e^{-(\phi_B)q/kT} \quad \rightarrow \quad \phi_B = -\frac{kT}{q}\ln\left(\frac{p_{surf}}{n_i}\right)$$

$$\phi_B = -(0.02586\ V)\cdot \ln\left(\frac{1\times 10^{16} cm^{-3}}{1.45\times 10^{10} cm^{-3}}\right) = -0.3495\ V$$

$$V_{FB} = \phi_M - \left(\chi_S + \frac{E_g}{2q} + \phi_B\right) = \phi_M - \chi_S - \frac{E_g}{2q} - \phi_B$$

$$if\ \phi_M \approx \chi_S + \frac{E_g}{2q}, \qquad V_{FB} = \frac{E_g}{2q} - \phi_B$$

$$V_{Tp} = V_{FB} = \frac{E_g}{2q} - \phi_B = 0.56\ V - (-0.3495\ V) = 0.9095\ V$$

A4. Now suppose the Si film is doped with concentration N_A and fully depleted. This will shift V_T from the values found in A2 and A3 by an amount of:

$$\Delta V_T = \frac{qN_A t_{Si}}{C_{ox}}$$

This shift applies to both the nMOS and pMOS transistors, since in this simple process the Si film doping must be the same for both. **Find the Si film doping** required to give $V_{Tn} = -V_{Tp}$. Assume that $t_{ox} = 50nm$.

Which provides more useful values of V_{Tn} and V_{Tp}, using a p+ poly gate or n+ poly gate for the pMOS device? Use this choice in the simulations that follow.

$C_{ox} = \frac{\epsilon_{ox}}{t_{ox}}$	$\epsilon_{ox} = \epsilon_{r\_SiO_2} \cdot \epsilon_o$
$V_{Tn} = -V_{Tp}$	$\Delta V_T = \frac{qN_A t_{Si}}{C_{ox}}$

$$C_{ox} = \frac{\epsilon_{ox}}{t_{ox}} = \frac{(3.9)(8.85\times 10^{-12}\ F/m)}{50\times 10^{-9} m} = 690.3\times 10^{-6}\ F$$

$$\Delta V_T = \frac{qN_A t_{Si}}{C_{ox}}$$

$$0.2105\ \text{V} = \frac{N_A(1.6 \times 10^{-19}\ C)(200nm)}{690.3 \times 10^{-6}\ F}$$

$$N_A = 4.53 \times 10^{15} cm^{-3}$$

Since the CMOS is an enhancement mode type, the threshold for the nMOS transistor has to be positive. And to maintain the relationship of $V_{Tn} = -V_{Tp}$, the gate for the pMOS has to be made of n+ polysilicon.

B1. Run the example MINIMOS files to determine V_{Tn} and V_{Tp} for a very lightly doped Si film. Compare to the analytic estimates in A1 and A2 above.

After running the threshold simulation on MINIMOS for the files "soiVTn.inp" and "soiVTp.inp", and comparing these results with the calculated values, we have:

Calculated	Simulation	Deviation ΔV
$V_{Tn} = -0.2105\ V$	$V_{Tn} = -0.152\ V$	0.0585 V
$V_{Tp} = 0.2105\ V$	$V_{Tp} = -1.159\ V$	1.3695 V

Clearly they are different from the ones previously calculated.

B2. Find the Si film doping required to give $V_{Tn} = -V_{Tp}$. Compare to analytic estimates. Compute the implanted dopant dose in the film.

Here are the Si film doping concentrations for both nMOS and pMOS transistors, which gives a threshold of +0.5V and -0.5V respectively.

nMOS	pMOS
$N_A = 1.1 \times 10^{16}\ cm^{-3}$	$N_A = 1.1 \times 10^{16} cm^{-3}$
$V_{Tn} = 0.464\ V$	$V_{Tp} = -0.464\ V$

Also, the Arsenic dose implant for the pMOS was set to $8.4 \times 10^{10} cm^{-3}$.

For the following simulations, use the Si film doping found in B2.

B3. Determine the subthreshold swing *S* for the nMOS and pMOS devices. Compare to the theoretical minimum. A small subthreshold swing can compensate for a relatively small magnitude of V_{Tn}. Comment on and explain any differences in S for the nMOS and pMOS devices.

The subthreshold swing is the difference between two Vg voltages in the subthreshold region over one decade of the Drain current. It is used as a metric for turning the MOSFET off.

$$S = \frac{\Delta V_{GS}}{\Delta \log_{10}(I_d)}$$

The substhreshold swing was calculate between $I_D = 10nA$ and $I_D = 1nA$. And the values of the gate voltages were taken for each current, using VDD= 0.1 V for nMOS and VDD= -0.1 for pMOS.

Devices	$I_D = 10nA$	$I_D = 1nA$	S
nMOS	$V_G = 0.363\ V$	$V_G = 0.291\ V$	72 mV/dec
pMOS	$V_G = -0.15\ V$	$V_G = -0.051\ V$	99 mV/dec

The theoretical threshold swing is 60mV/dec. The S values for both devices, just below at their respective threshold voltage, are larger than the theoretical value, as it should be. In this case, the S value of the pMOS is greater than the S value of the nMOS.

B4. Verify that both nMOS and pMOS devices do not suffer from significant short channel effects down to $L = 2\mu m$. To answer this question, you will probably want to examine the subthreshold characteristics and determine Drain Induced Barrier Lowering in the devices.

As shown in **Figure 4** and **Figure 5**, both transistors suffer from some short-channel effects: channel-length modulation, skewing of threshold voltage.

Calculating the Drain Induced Barrier Lowering for both devices at $I_D = 100nA$, $I_D = 10nA$, and $I_D = 1nA$ yields:

Devices	$I_D = 100nA$	$I_D = 10nA$	$I_D = 1nA$
nMOS	215mV	210mV	214mV
pMOS	290mV	233mV	234mV

Beside the high values of DIBL, no other short-channel effects are visible. But having these values means that the threshold voltages have lowered, and there is more subthreshold leakage current present.

B5. It is difficult to simulate hot carrier effects in SOI devices with MINIMOS, since there is no way to access the avalanche-generated hole current injected into the p-well in an nMOS device (an analogous situation holds for pMOS devices). MINIMOS can still be used to determine the *peak avalanche generation rate*, and a rough estimate of the total hole current generated can be made by multiplying the peak rate over the volume in which generation is significant. Find the peak generation rate and estimate the current injected into the well for 5 V power supply operation for both nMOS and pMOS devices for $L = 2\mu m$.

Are hot carrier effects significant in these devices?

As shown in **Figure 6** and **Figure 7,** hot carriers are generated on the Drain-Si film junction on the nMOS and pMOS, respectively. At the peak avalanche generation rate, the substrate current estimated was about $3.157 \times 10^{-7} A/\mu m$, calculated as follows:

First, plot the peak Avalanche Generation Rate on MINIMOS for both devices, and check the peak rate. Second, zoom to the area where the peak avalanche is generated and calculate area. Calculate the volume by multiplying the area times the width of the device. Next, multiply the peak rate x Volume x electron charge to obtain the substrate current. Finally, divide by 1 µm to obtain A/µm.

$I_{Subs} = G_p \cdot q \cdot Volume_p/1\mu m$	L_p : Length of Av. peak rate	t_p Depth of APR
$Volume_p = L_p \cdot W_{Si} \cdot t_p$	W_{Si} : Width of device	G_p Avalanche peak rate

$$Volume_p = (0.056 \times 10^{-6}m)(1 \times 10^{-6}m)(0.134 \times 10^{-6}m)$$

$$Volume_p = 7.504 \times 10^{-21}m^{-3}$$

$$I_{Subs} = (2.63 \times 10^{26}\ m^{-3} \cdot s^{-1})(1.6 \times 10^{-19}\ A \cdot s)(7.504 \times 10^{-21} cm^{-3})/(1 \times 10^{-6} m)$$

$$I_{Subs} = 3.157 \times 10^{-7} A/\mu m$$

Using the same procedure for the pMOS, the substrate current calculated was:

$$I_{Subs} = 3.274 \times 10^{-8} A/\mu m$$

Figure 6 and **Figure 7** show the dimension of the avalanche generation rate on both devices. The peak rate is more concentrated on the pMOS in a smaller volume than on the nMOS. But the peak avalanche rate on the pMOS generates less substrate current than in the case of the nMOS. These amounts of leakage currents can be tolerable.

B6. Estimate the smallest channel length providing acceptable short channel and hot carrier behavior for both nMOS and pMOS devices.

Modifying the channel length to 2 μm or less, the devices will be suffering from some short-channel effects like increased DIBL (more than 200mV), leakage drain current at zero Gate voltage bias, associated channel-length modulation effect, significant avalanche peak generation rate, and increased leakage current into the substrate. Increasing the channel length more than 2 μm, these short-channel effects will be reduced.

B7. Investigate whether there are any significant advantages in device performance to using an oxide thickness less than 50 nm, and/or a Si film thickness less than 200 nm. A reasonable minimum for the gate oxide thickness is about 25 nm, and for the Si film thickness about 100 nm.

With L = 2.5 μm, tsi = 200nm, tox = 25nm at Id = $1x10^{-8}$ A

Devices	VDD=+/-0.1V	VDD=+/-5.0V	DIBL
nMOS	0.025V	-0.036V	61 mV
pMOS	-0.290V	-0.199V	94 mV

With L = 2.5 μm, tsi = 100nm, tox = 50nm at Id = $1x10^{-8}$ A

Devices	VDD=+/-0.1V	VDD=+/-5.0V	DIBL
nMOS	-0.002V	-0.096V	94 mV
pMOS	-0.566V	-0.490V	76 mV

With L = 2.5 μm, tsi = 150nm, tox = 40nm at Id = $1x10^{-8}$ A

Devices	VDD=+/-0.1V	VDD=+/-5.0V	DIBL
nMOS	0.062V	-0.021V	83 mV
pMOS	-0.360V	-0.274V	89 mV

It seems that with L = 2.5 μm, tsi = 150nm, and tox = 40nm offers good advantages: Not only the CMOS gets smaller but also the threshold voltages increases, which helps on having less leakage current, it also reduces the short-channel effects better than just lowering a single variable. **Figure 8** and **Figure 9** show the plotting for the nMOS and pMOS devices respectively.

Conclusions

Designing the first stage of the CMOS project is really demanding, especially with the established requirements and tools available.

MINIMOS has proven to be a good tool to start with the project, although it is simple on its interface but complicated in the way of adding the data.

With the proper configuration, a CMOS device can be scaled down, and on the same time reducing the short-channel effects due to the scaling nature.

Appendix

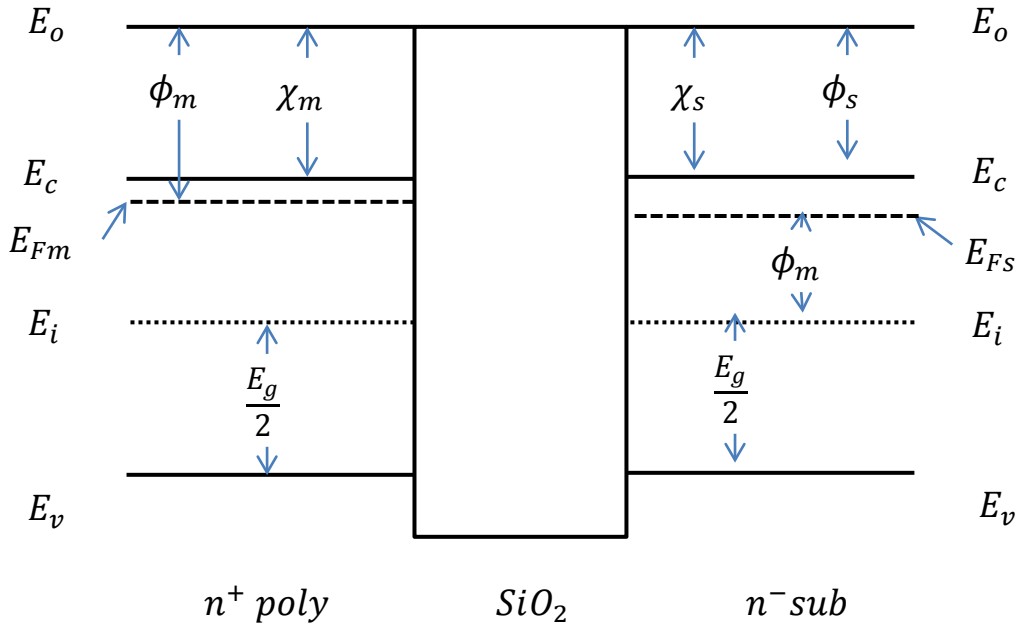

Figure 1 Energy band diagram of the nMOS transistor with n-substrate.

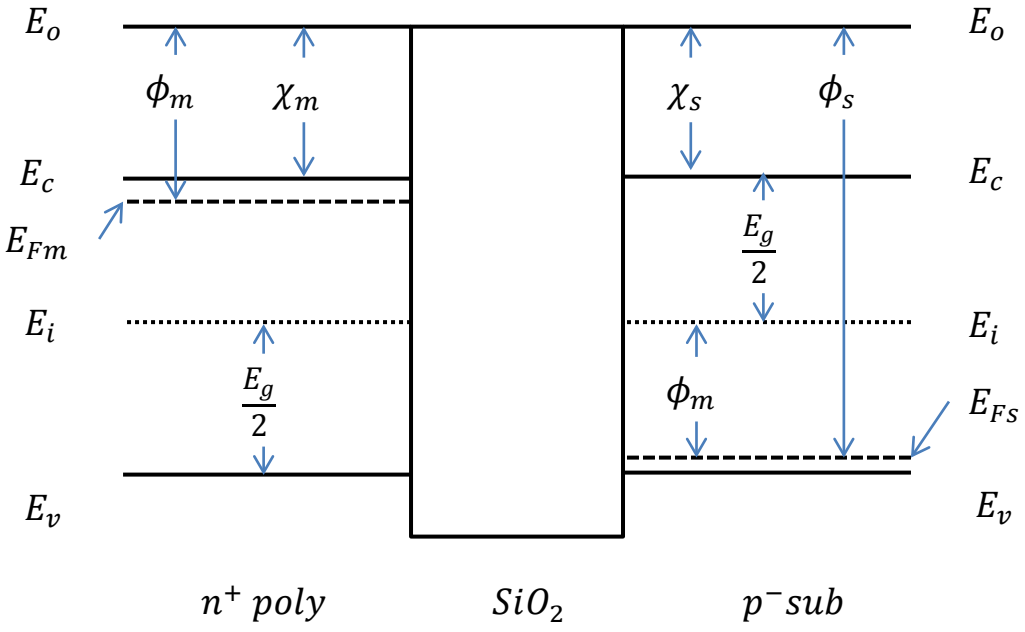

Figure 2 Energy band diagram of the nMOS transistor with p-substrate.

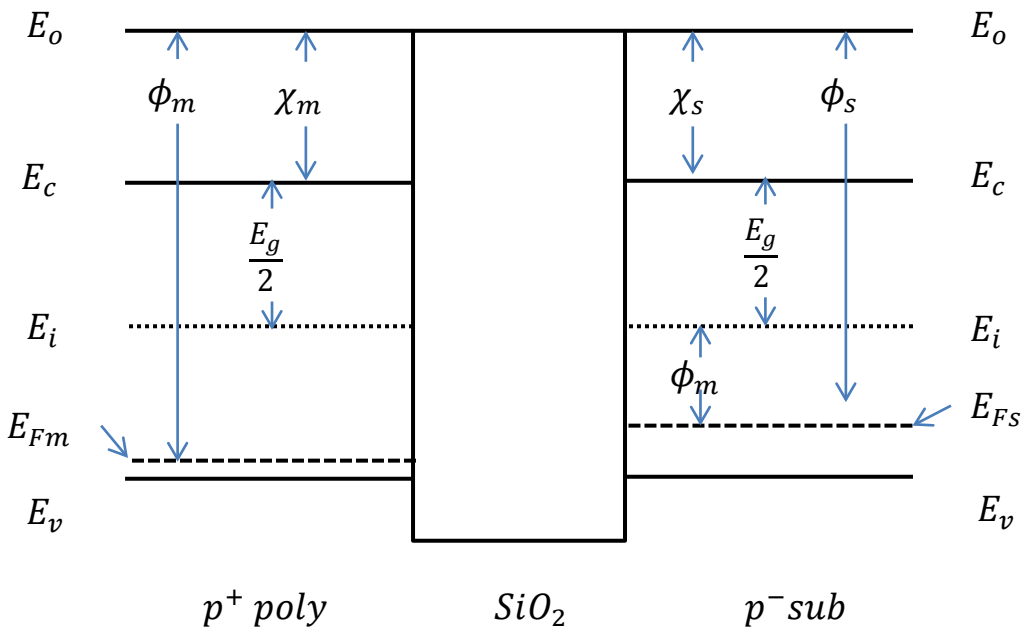

Figure 3 Energy band diagram of the pMOS transistor with p-substrate.

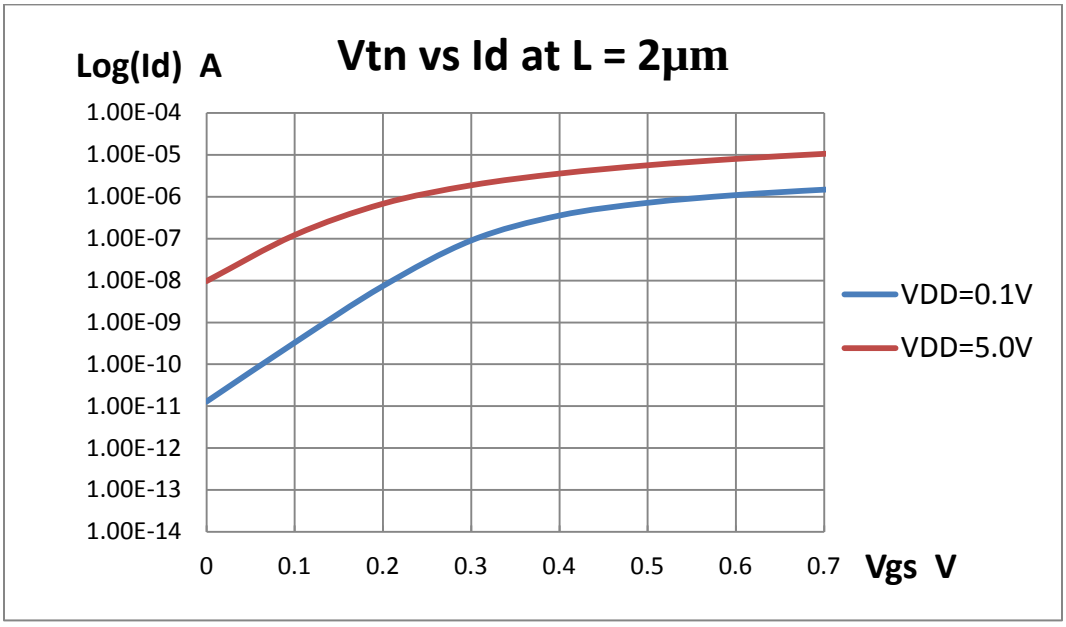

Figure 4. nMOS Subthreshold characteristic curve plot at L= 2µm.

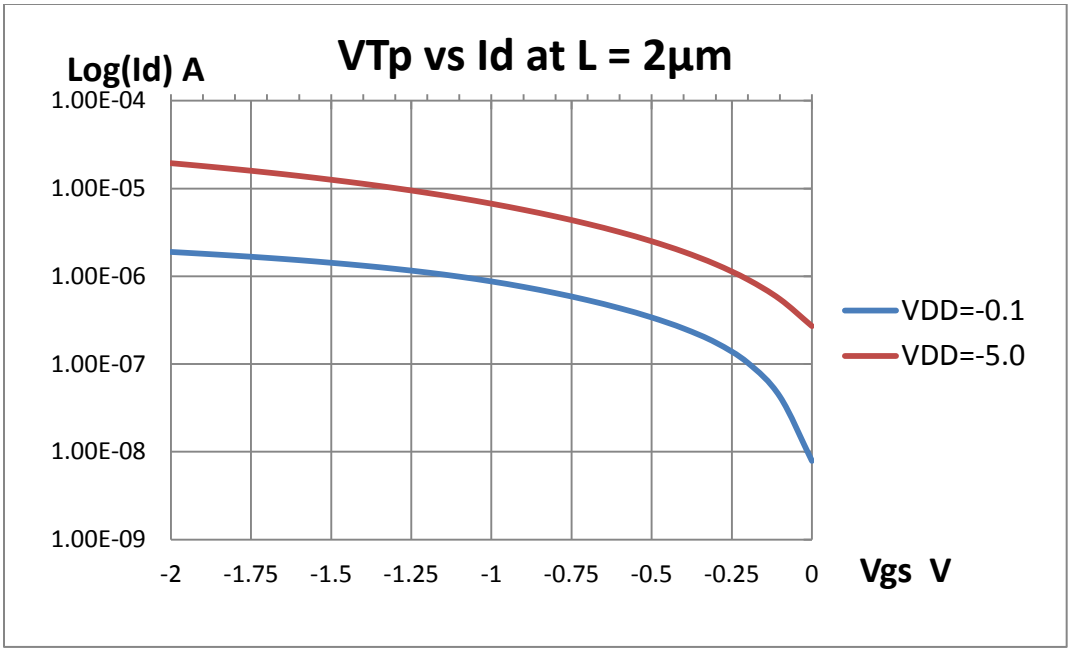

Figure 5. pMOS Subthreshold characteristic curve plot at L= 2µm.

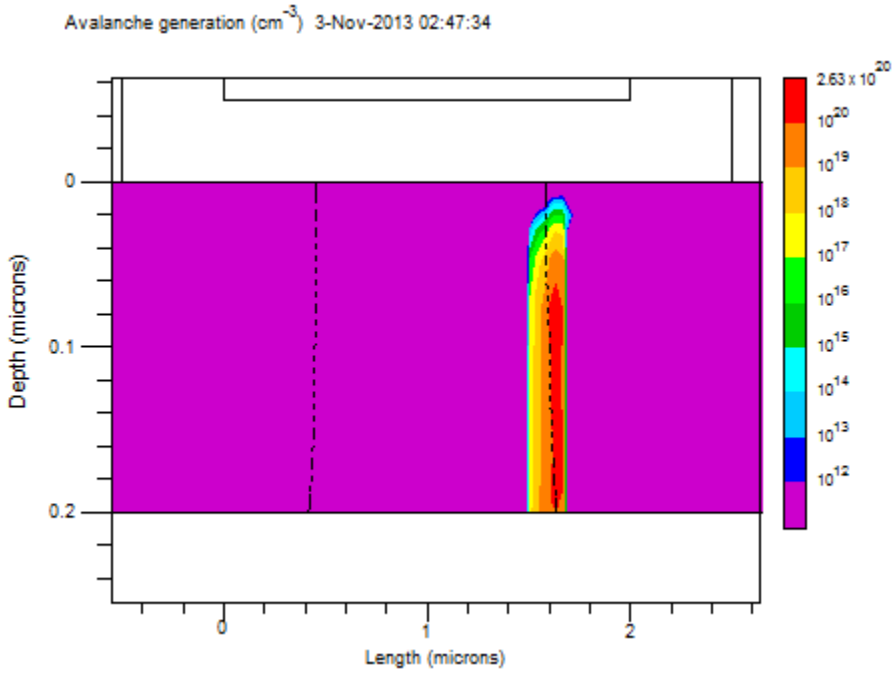

Figure 6. Peak Avalanche generation rate on the nMOS device.

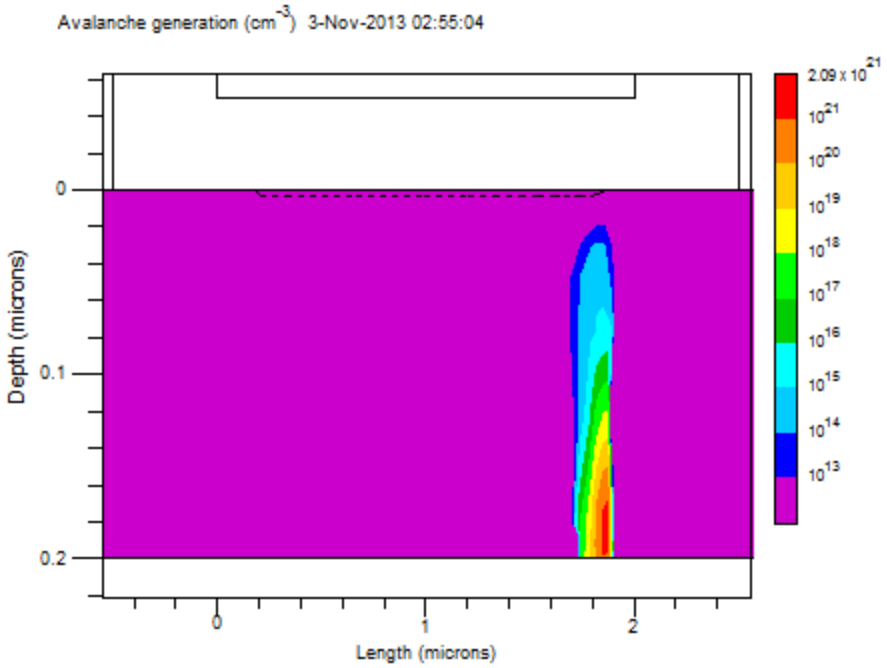

Figure 7. Peak Avalanche generation rate on the pMOS device

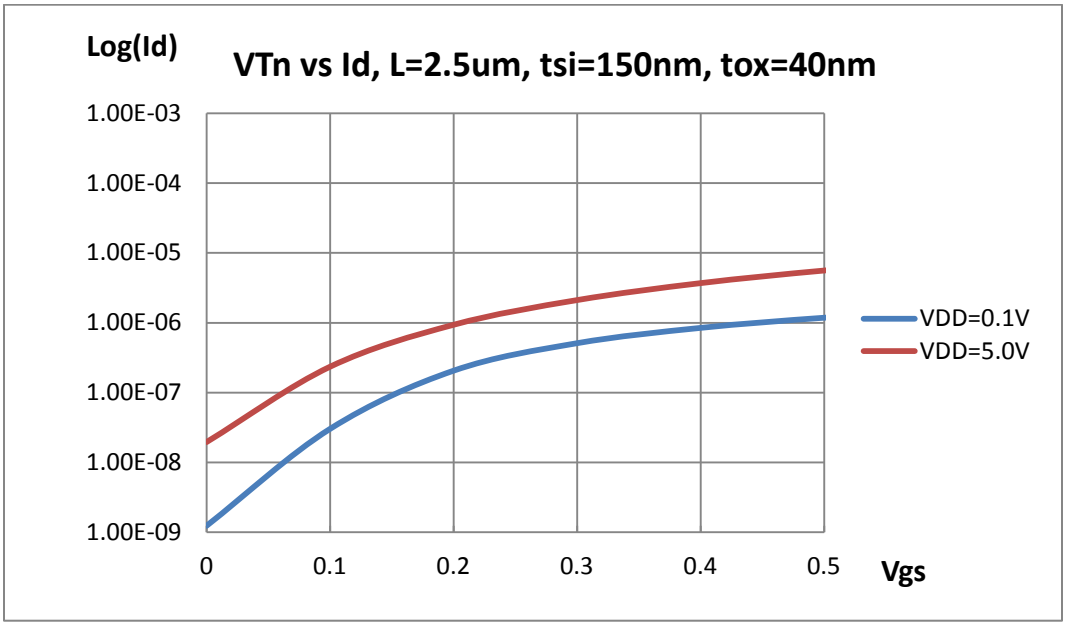

Figure 8. nMOS Subthreshold I-V curve plot with L= 2.5µm, tsi=150nm and tox=40nm.

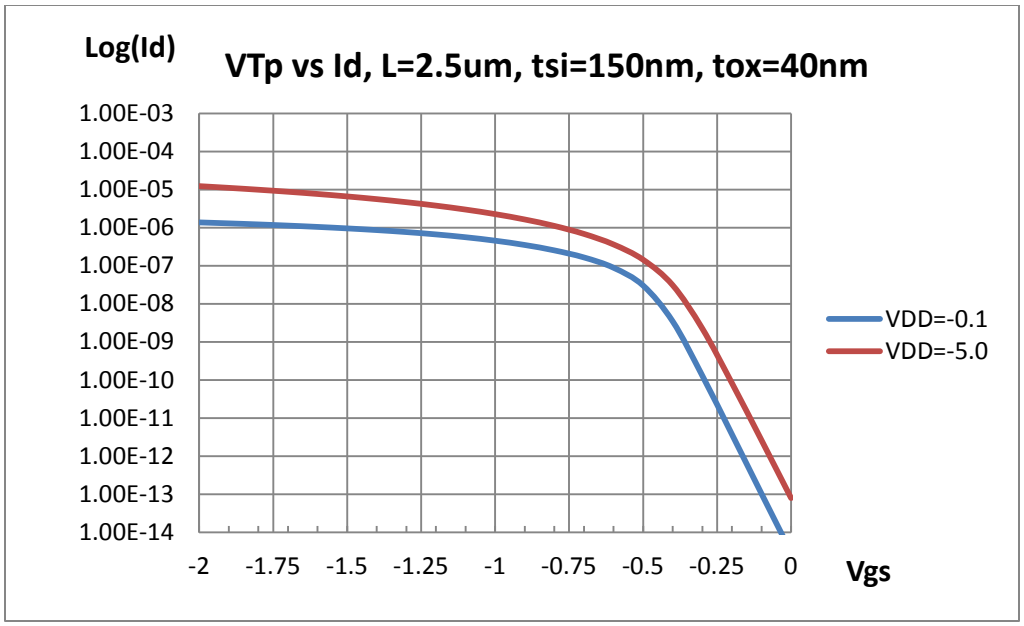

Figure 9. pMOS Subthreshold I-V curve plot with L= 2.5µm, tsi=150nm and tox=40nm.

SOI example
* Carleton SOI CMOS, NMOS device, lightly doped Si film

DEVICE CHANNEL=N GATE=NPOLY TINS=40E-7 BULK=1E-4 KBULK=3.9 FILM=0.15E-4 W=1.0E-4 L=2.5E-4
* source/drain diffusion

PROFILE NS=3E20 TEMP=1080 TIME=600 NB=1.1E16

* Compute VT, defined as value of VG giving ID=1E-7A
*OPTION MODEL=THRESH PHYSCHK=NO CU=1E-7
OPTION MODEL=2-D PHYSCHK=NO CU=1E-7

*OPTION MODEL=AVAL PHYSCHK=NO CU=1E-7
*BIAS UD=5 UG=0

STEP DG=0.1 NG=20
BIAS UD=0.1 UG=0

OUTPUT PSI=N ETRAN=N ELAT=N MIN=N DC=Y AVAL=N
*OUTPUT PSI=N ETRAN=N ELAT=N MIN=N DC=Y AVAL=Y
END ERR=0.001 BIN=Y

SOI example

```
* Carleton SOI CMOS pMOS

DEVICE CHANNEL=P GATE=NPOLY TINS=40E-7 BULK=1E-4 KBULK=3.9 FILM=0.15e-4 W=1.0E-4
L=2.5E-4
*OPTION MODEL=THRESH PHYSCHK=NO CU=1E-7
OPTION MODEL=2-D PHYSCHK=NO CU=1E-7
*OPTION MODEL=AVAL PHYSCHK=NO CU=1E-7

* source/drain implant
PROFILE ELEM=B DOSE=3E15 AKEV=50 TEMP=1000 TIME=600 NB=1.1E16 SUBS=P
* dummy implant to create an n-type region at Si film surface
IMPLANT ELEM=AS DOSE=8.4E10 AKEV=50 TEMP=900 TIME=60

STEP DG=-0.1 NG=20

BIAS UD=-0.1 UG=0.0
OUTPUT PSI=N ETRAN=N ELAT=N MIN=N DC=Y AVAL=N
*OUTPUT PSI=N ETRAN=N ELAT=N MIN=N DC=Y AVAL=Y
END ERR=0.001 BIN=Y
```