THE UNIVERSITY OF TEXAS AT ARLINGTON

COMPUTER SCIENCE AND ENGINEERIG

LABORATORY 5 REPORT

ELECTRONICS LABORATORY

Submitted toward the partial completion of the requirements for CSE 3323-002

Submitted by,

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Lab 5: BJT Amplifier, NPN & PNP

Part 1: Amplifiers Designs

NPN Design:

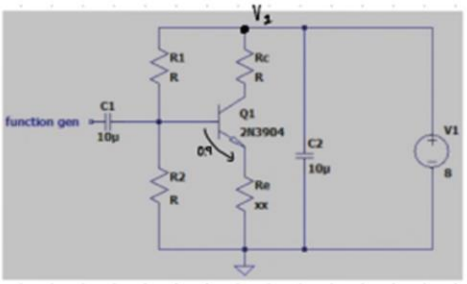
$V_{cc} = 8V$
$I_c = 10mA$
$V_{RE} = 1V$

NPN $V_c = 2-8V$ PNP $V_c = 0-6V$

Emitter and Collectors currents are very close to equal.
Base current is small compared to collector and emitter current.

$\alpha = \frac{\beta}{\beta+1}$, $\beta = \frac{\alpha}{1-\alpha}$

$\beta = 100$ $\alpha I_c = I_e$
$\alpha = 0.99$ $\beta I_b = I_c$



1) $I_e = I_e = 10mA$
$V_{RE} = 1V$

$V_{RE} = I_e \cdot R_E$

$R_E = \frac{V_{RE}}{I_E}$

$R_E = \frac{1}{10 \times 10^{-3}}$

$R_E = 100\ \Omega$

2) $V_{CNPN} = 5V$
$V_1 = 8V$
$I_c = 10mA$

$V_1 - V_{RC} = V_{CNPN}$
$8 - V_{RC} = 5V$
$V_{RC} = 3V$

$R_C = \frac{V_{RC}}{I_C}$

$R_C = \frac{3V}{10 \times 10^{-3}}$

$R_C = 300\ \Omega$

NPN

3) $I_c = \beta I_b$

$I_B = \frac{I_c}{\beta}$

$I_B = \frac{10 \cdot 10^{-3}}{100}$

$I_B = 0.1mA$

$I_{R_1} = I_{R_2} = 10 \cdot I_B$
$\simeq 10\,(0.1m)$
$I_{R1,R2} = 1mA$

$\frac{V_1 - 0}{R_1 + R_2} = 0.001$

$R_1 + R_2 = \frac{8}{0.001}$

$R_1 + R_2 = 8000\ \Omega$

4) $V_b = ?$
$V_{RE} = 1V$
$V_{eb} = 0.7$

$V_b = V_{eb} + V_{RE}$

$V_b = 0.7 + 1$

$V_b = 1.7V$

5) Using voltage divider equation

$V_b = V_{cc}\left(\frac{R_2}{R_1 + R_2}\right)$

6) $V_b = V_{cc}\left(\frac{R_2}{R_1 + R_2}\right)$

$1.7 = 8\left(\frac{R_2}{R_1 + R_2}\right)$

$\frac{1.7}{8} = \frac{R_2}{R_1 + R_2}$

$\left(\frac{1.7}{8}\right)(R_1 + R_2) = R_2$

$\frac{1.7}{8}(8000) = R_2$

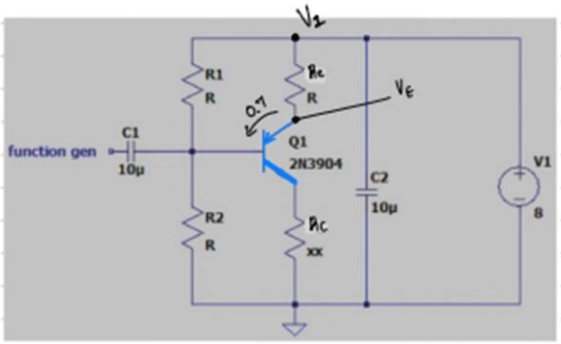
$R_2 = 1700\ \Omega$

$R_1 + R_2 = 8000$
$R_1 + 1700 = 8000$

$R_1 = 6300\ \Omega$

PNP Design:

PNP



1) $R_E = \frac{V_{RE}}{I_E} = \frac{1}{10 \times 10^{-3}} = \boxed{100}$

2) $V_{CPNP} = 3V$

$I_c = 10mA$ $\quad R_c = \frac{3V}{10 \cdot 10^{-3}}$

$V_{RC} = V_{CPNP}$ $\quad \boxed{R_c = 300\ \Omega}$

3) $I_c = \beta I_b$

$I_B = \frac{I_c}{\beta}$

$I_B = \frac{10 \cdot 10^{-3}}{100}$

$I_B = 0.1mA$

$I_{R_1} = I_{R_2} = 10 \cdot I_B$

$\simeq 10\,(0.1m)$

$I_{R_1,R_2} = 1mA$

$\frac{V_E - 0}{R_1 + R_2} = 0.001$

$R_1 + R_2 = \frac{8}{0.001}$

$\boxed{R_1 + R_2 = 8000\ \Omega}$

4) $V_b = ?$

$V_{eb} = 0.7$

$V_E = ?$

$V_E = V_1 - V_{RE}$

$V_E = 8 - 1$

$V_E = 7V$

$V_b = V_E - V_{eb}$

$V_b = 7 - 0.7$

$\boxed{V_b = 6.3\ V}$

5) Using voltage divider equation

$$\boxed{V_b = V_{cc}\left(\frac{R_2}{R_1 + R_2}\right)}$$

6) $V_b = V_{cc}\left(\frac{R_2}{R_1 + R_2}\right)$

$6.3 = 8\left(\frac{R_2}{R_1 + R_2}\right)$

$\frac{6.3}{8}(R_1 + R_2) = R_2$

$R_2 = \frac{6.3}{8}(8000)$

$\boxed{R_2 = 6300\ \Omega}$

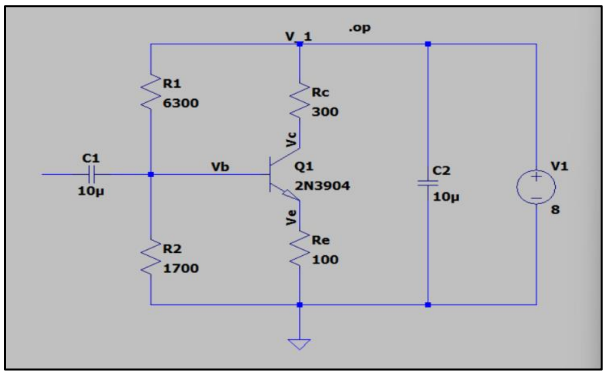
$R_1 + R_2 = 8000$

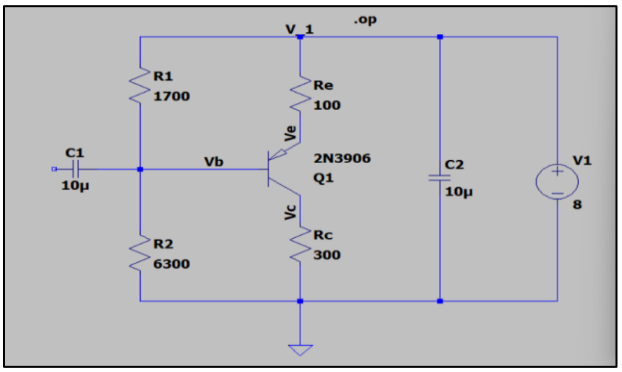
$R_1 + 6300 = 800$

$\boxed{R_1 = 1700\ \Omega}$

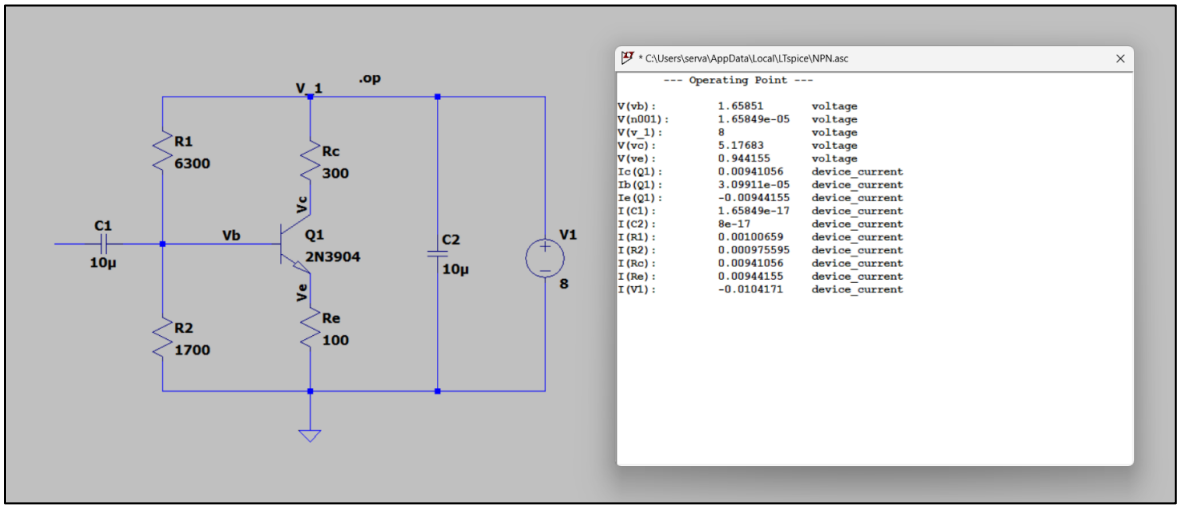
Part 2: LT Spice Simulations

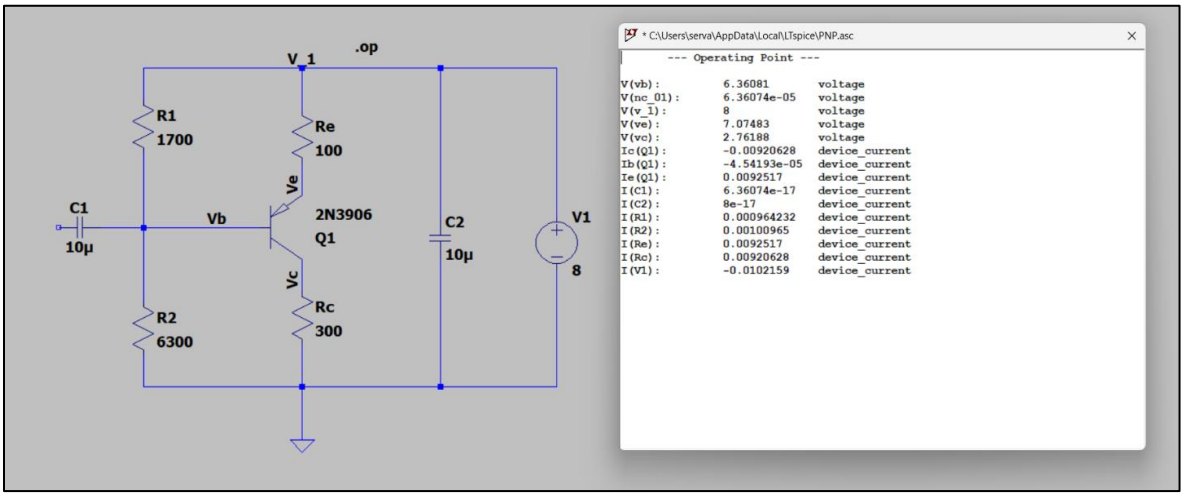
NPN and PNP Circuit Diagram:





.OP Simulations:





Findings:

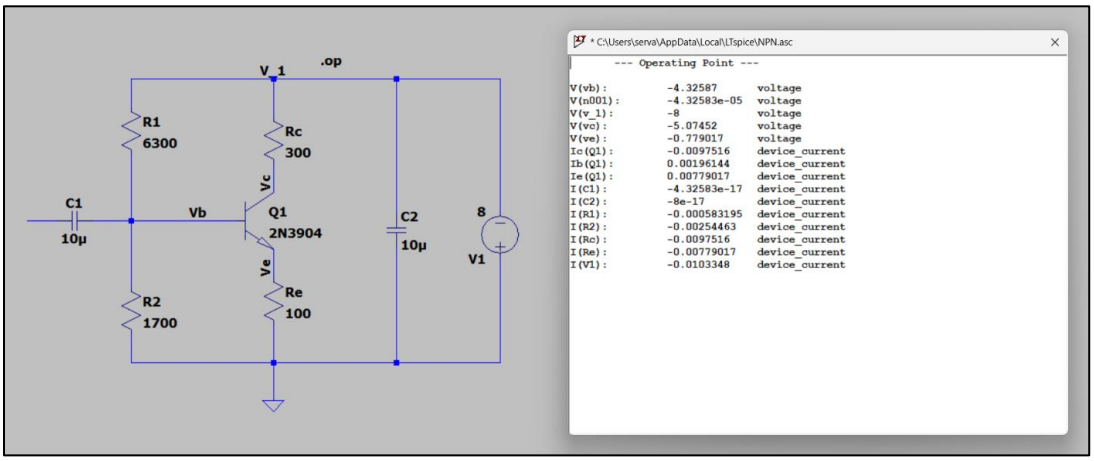
NPN	PNP
$V_c = 5.17$ V	$V_c = 2.7$ V
$I_c = 0.0094$ A	$I_c = 0.0092$ A
$V_e = 0.94$ V	$V_e = 7.01$ V
$V_b = 1.65$	$V_b = 6.36$ V
V_b % error = 2.95%	V_b % error = 0.95%

8) What observation can you make about the values for R1, R2, RC, and RE for the PNP design relative to the values determined for the NPN design?

Re and Rc swap values and so do R1 and R2, for PNP relative to the NPN design.

9) If a -8V supply was available, could the NPN design be converted to the PNP design be changing ONLY the device and by replacing the 8V supply with a -8V supply?

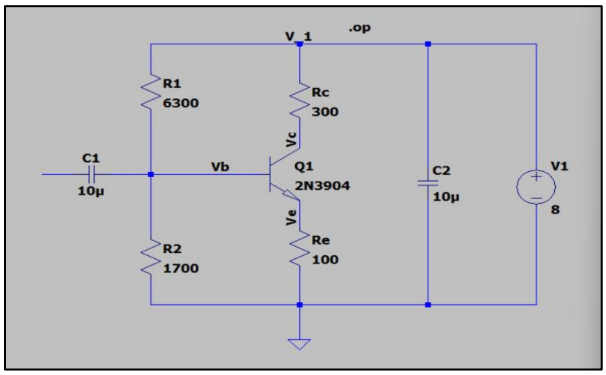
No, this wouldn't work since PNP and NPN behave differently regardless of a 8V or -8V supply

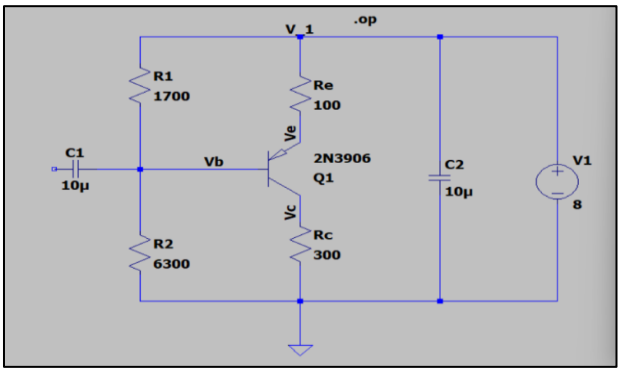


NPN -8V supply does not look similar in any way to value from PNP.

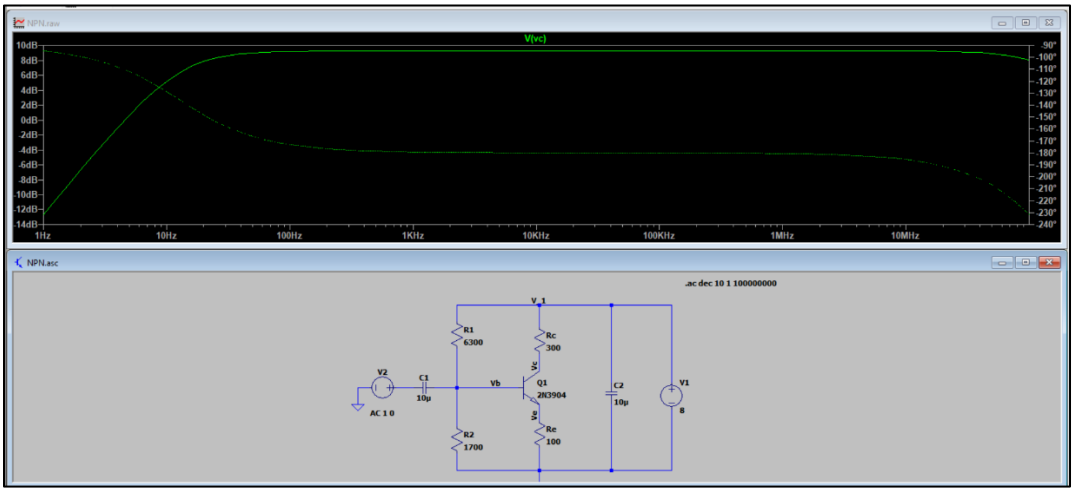
Part 3: AC LT Spice Analysis Simulations

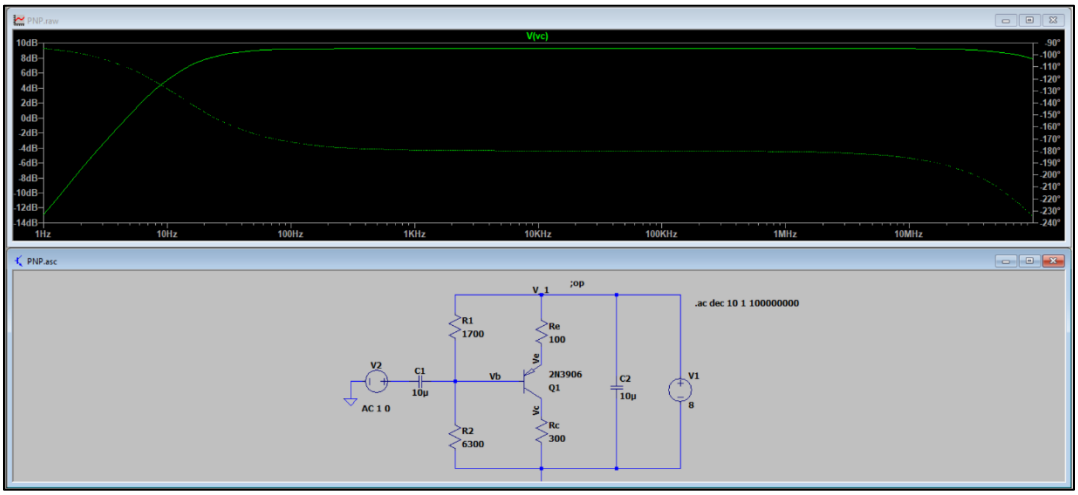
NPN and PNP Circuit Diagram:





AC Simulations:





Findings:

1) Do a .AC simulation (decade, 10 pts per decade) from 1 Hz to 100 MHz. What is the midband gain in dB (at 10KHz)?

NPN	PNP
@10KHz -> gain = 9dB	@10Hz -> gain = 9dB

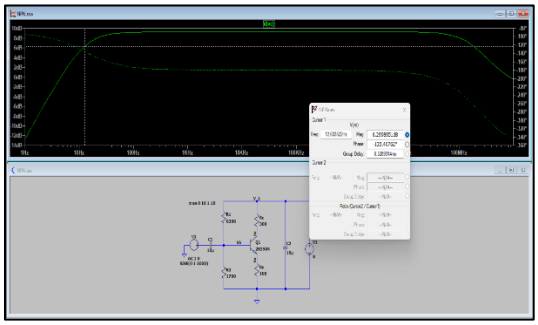
`

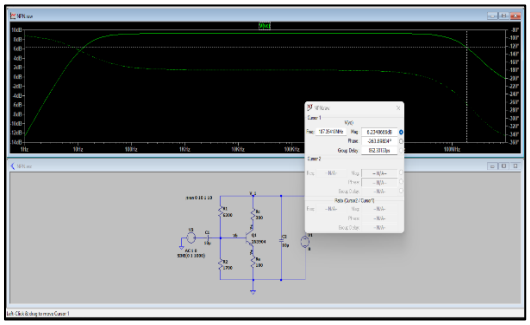
From this value, calculate numerical voltage gain and state the phase that goes with the gain.

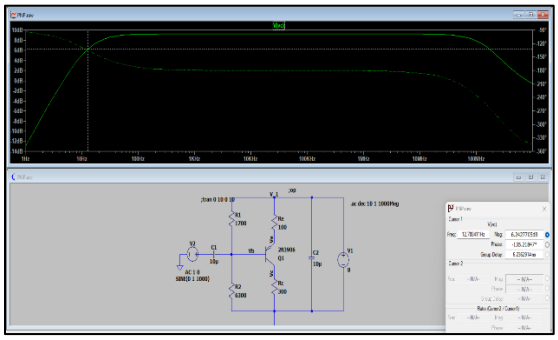
NPN	PNP
G = 20 log (Vout/Vin)	G = 20 log (Vout/Vin)
G/20 = log(Vout/Vin)	G/20 = log(Vout/Vin)
10^(G/20) = Vout/Vin	10^(G/20) = Vout/Vin
Vout/Vin = 10^(5/20)	Vout/Vin = 10^(5/20)
Vout/Vin = 1.78 V/V	Vout/Vin = 1.78 V/V
Phase Shift = -120	Phase Shift = -120

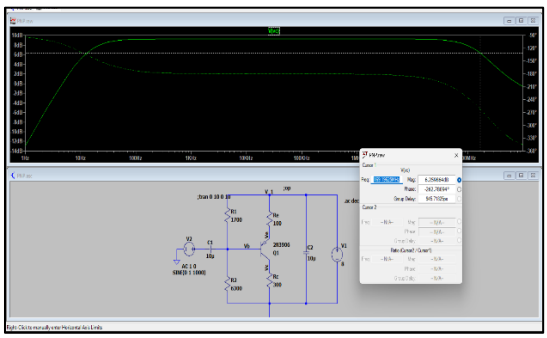
What are the approximate –3 dB frequencies low and high. Include a screen shot in your report.

NPN	PNP
High -> 12.6 Hz	High -> 12.8 Hz
Low -> 187.3 MHz	Low -> 169.2 MHz



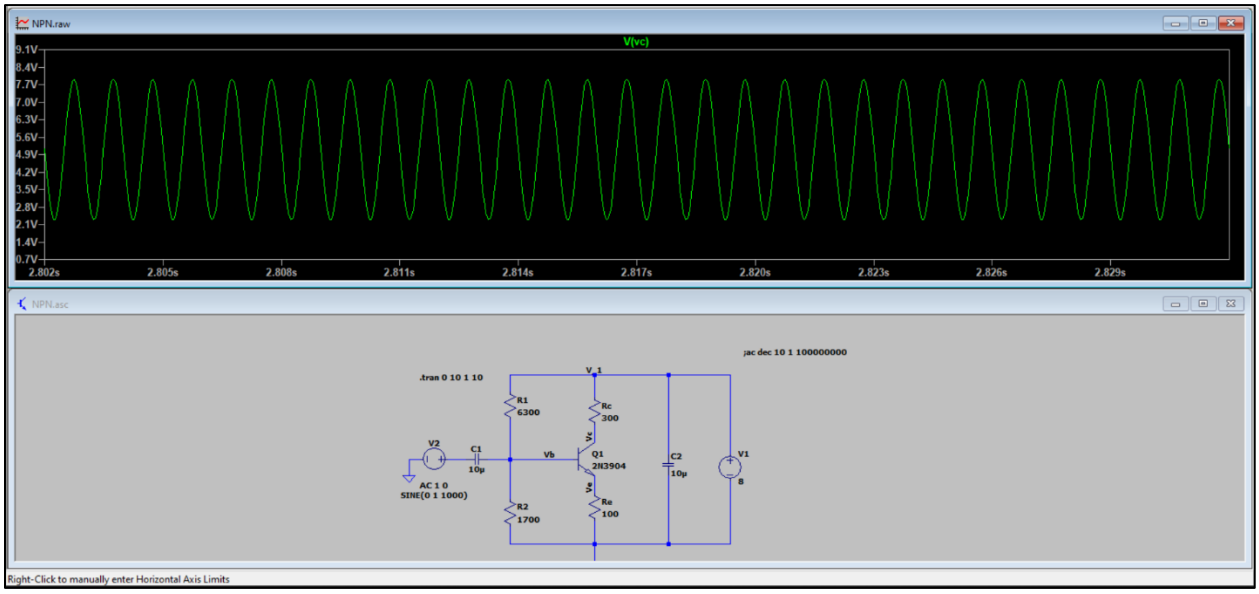


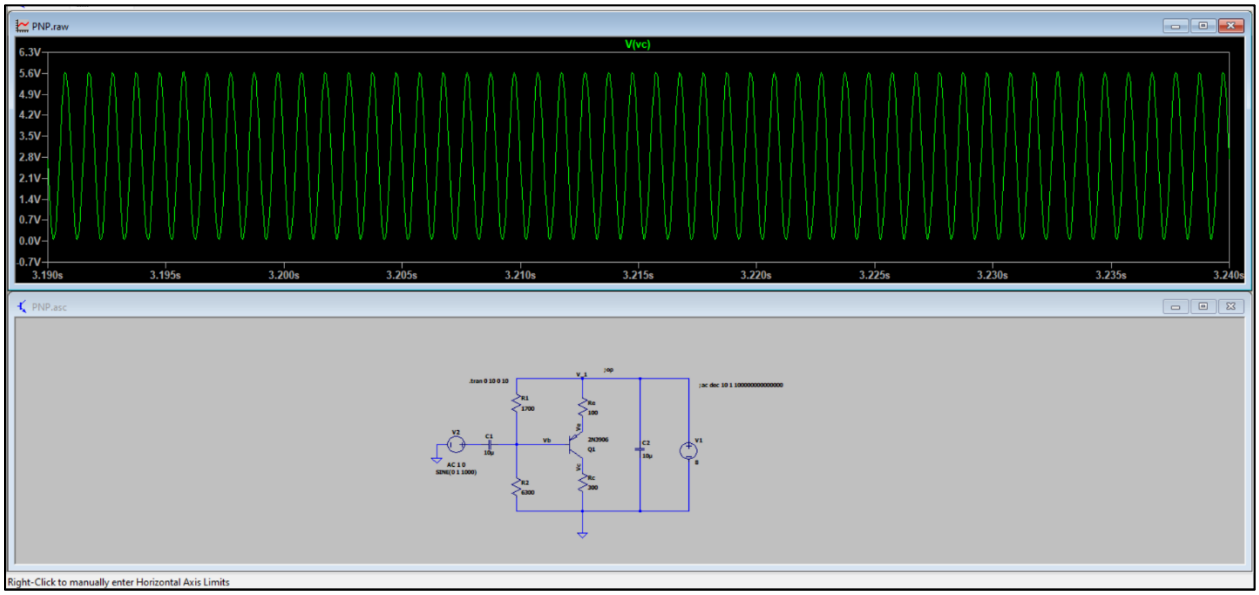




TRAN Simulation:

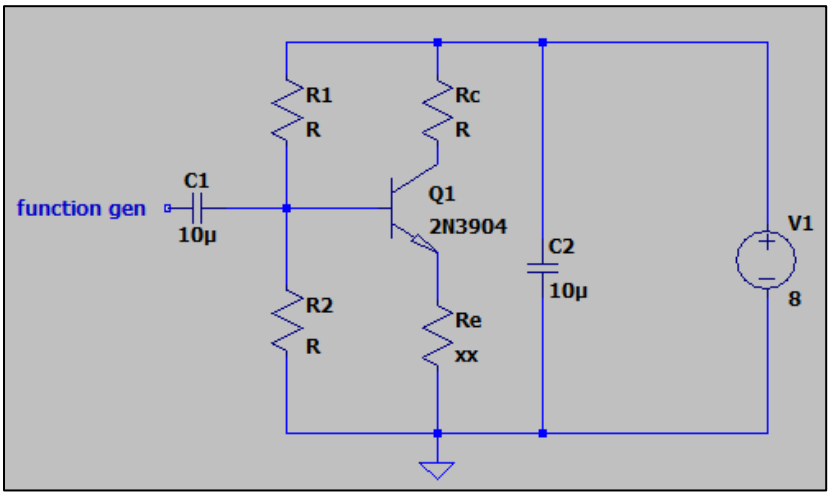
Do a .TRAN simulation with frequency = 1 KHz and amplitude = 1V.





Part 4: Building the Amplifiers

NPN Circuit Diagram:



Findings:

Measure V_c, V_b, V_e. Calculate I_c. Compare I_c and V_c to your goals.

$V_c = 4.98$ V
$V_b = 1.66$ V
$V_e = 0.98$ V
$I_c = (8-4.98)/330 = 9.13$ mA

Desired $V_c = 5$ V

Desired $I_c = 10$ mA

Measured values are close to desired values with some degree of error.

With function generator and scope, measure small signal midband gain / phase with output at collector, then f3dB low, and if possible f3dB high.

Frequencyy (Hz)	V_{in}	V_{out}	Gain	Phase
1	1	0.3	-10.4576	92
5	1	1.44	3.16725	96
10	1	1.9	5.575072	127
100	1	3.18	10.04854	176
500	1	3.22	10.15712	178
1k	1	3.22	10.15712	179

5k	1	3.22	10.15712	180
10k	1	3.22	10.15712	180
50k	1	3.38	10.57833	180
100k	1	3.44	10.73117	180
1M	1	3.38	10.57833	195
5M	1	2.28	7.158697	238
10M	1	1.42	3.045767	259

Mind-band Gain = 10 dB

F3dB low = 5 Hz
F3dB high = 10 MHz

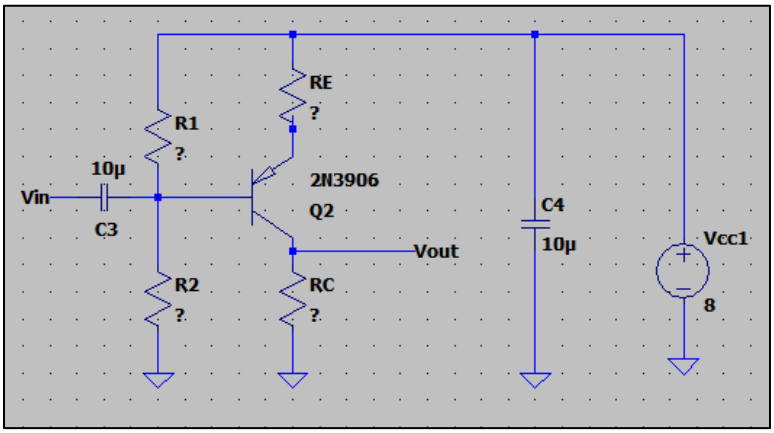
What is the gain with output taken at the emitter?

Mind-band Gain (@10 kHz) = -0.291 dB

What is the max ppk output level at 1 KHz without significant distortion (on collector).

Max ppk @ 1 KHz ➔ 2.3 Vpp

PNP Circuit Diagram:



Findings:

Measure V_c, V_b, V_e. Calculate I_c. Compare I_c and V_c to your goals.

V_c = 3.05 V
V_b = 6.4 V

$V_e = 7.12$ V
$I_c = (8\text{-}4.98)/330 = 9.13$ mA

Desired $V_c = 3$ V

Desired $I_c = 10$ mA

Measured values are close to desired values with some degree of error.

With function generator and scope, measure small signal midband gain / phase with output at collector, then f3dB low, and if possible f3dB high.

Frequency (Hz)	V_{in}	V_{out}	Gain	Phase
1	1	0.344	-9.26883	107
5	1	1.08	0.668475	128
6	1	1.38	2.797582	120
10	1	1.72	4.710569	131
100	1	2.98	9.484325	172
500	1	3.02	9.600139	178
1k	1	3.02	9.600139	179
5k	1	3.04	9.657472	180
10k	1	3.06	9.714429	180
50k	1	3.22	10.15712	180
100k	1	3	9.542425	171
1M	1	3.12	9.883092	195
5M	1	2.04	6.192603	243
10M	1	1.27	2.076074	266

Mind-band gain = 10 dB

F3dB low = 6 Hz
F3dB high = 10 MHz

What is the gain with output taken at the emitter?

Mind-band Gain (@10 kHz) = -0.283 dB

What is the max ppk output level at 1 KHz without significant distortion (on collector).

Max ppk @ 1 KHz ➔ 1.9 Vpp

Why do we *need* C1/C3 between the function generator and the base bias resistors?

Their function might be to couple the signal to and from the transistor but block the DC current from flowing into it.