CSE 3323 Lab 6

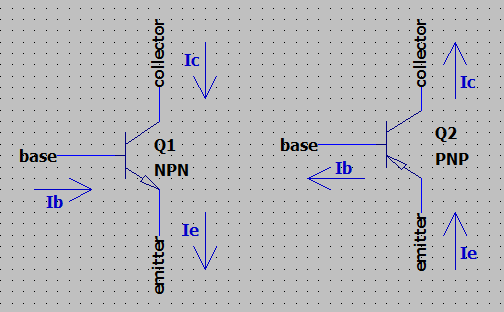
BJT Amplifier, NPN, PNP

For this lab, you will design two single transistor BJT amplifiers, first with an NPN, second with a PNP transistor. You will verify your design with LTSpice, then build and test the amplifiers. There is a lot to do here, but 3 weeks are allocated.

First read the tutorial on the BJT (bipolar junction transistor). This will help explain some of the symbols and parameters which you may or may not be familiar.

1. Tutorial

* BJTs come in two flavors, PNP and NPN, symbols shown below.
* Every BJT has an emitter (E), a base (B), and a collector (C).
* Vb, Vc, Ve, describe node voltages at the base, collector, and emitter respectively.
* Vbe / Veb and Vce / Vec are differences between the respective node voltages. For example, Vbe = Vb-Ve.
* Ib, Ic, and Ie describe base, emitter, and collector currents respectively. Note that current flows opposite direction in PNP and NPN devices. KCL does apply to the BJT (Ic+Ib=Ie).
* BJT Modes or Regions of Operation: Cutoff, **Active**, Saturation, and Inverse. Amplifiers in this course will be designed to operate in the **active** region.



* Parameters:
  + Alpha (a) => aIc = Ie, conservative value of alpha for active region operation (and devices we use) is 0.99. This means that emitter and collector currents are very close to equal.
  + Beta (b) => bIb = Ic, conservative value of beta for active region operation (and devices we use) is 100. This means that base current is small compared to collector or emitter current.
  + Conversion from alpha to beta: a = b/(b+1), b = a/(1-a)
* Active Region Operation: The emitter-base junction is forward biased and appears as a diode, while the collector base junction is reverse biased. Note that for the NPN device, the diode points from base to emitter, vs the PNP device from emitter to base. Hence Vbe (NPN) or Veb (PNP) is 0.7 V (@25C). Indeed, emitter current increases exponentially with Vbe / Veb as expected for a diode, BUT the current flows in the collector, with only a small base current.

Amplifier Design Requirements: Both amplifiers are to be designed to the following requirements. Note that gain is not listed in the requirements, as other parameters define the gain.

* Vcc=8V
* Ic = 10 mA
* VRE = 1V (voltage across emitter resisitor)
* Vc at the quiescent point (Q point) to be centered between Vc = 2V and 8V (approximately) for NPN, and between 0V and 6V for PNP Note: Q pt describes how the amplifier is “biased”. We must bias the amplifier prior to introducing the AC which is to be “amplified”. This Q point centering will maximize the peak to peak swing available on the collector without clipping.
* Bias divider (R1 and R2) current approximately 10x typical base current. Assume typical beta = 100.

3. Step-by-step procedure for biasing the device

Show calculations for lab report. After completing the design, do an operation point simulation on LTSpice to verify your design. Reference the schematics below.

1. Calculate Re from Ic and Vre requirements (Ohm’s Law). You may assume Ie = Ic for this calculation.
2. Calculate Rc: First find Vc from Q point centering requirement, then V across RC. Then use Ic requirement to calculate RC.
3. Calculate R1+R2: Start with the Ic design requirement, calculate Ib using typical beta, then calculate required current in the bias divider (R1 and R2) using the bias divider requirement. Lastly calculate R1+R2 from the Vcc requirement and bias divider current requirement.
4. Calculate Vb from Vre requirement and Vbe/Veb for silicon BJT (0.7V at room temp).
5. Write the voltage divider equation for Vb in terms of Vcc and R1 and R2.
6. Sub 3) into 5) and calculate R2, then calculate R1.
7. Verify your bias calculations by doing an operating point simulation (.OP) on LTSpice. Make sure you have replaced the generic NPN and PNP devices with the specified devices (2N3904 for NPN, 2N3906 for PNP). The Rs and Cs can be ideal components. Verify Q point (Vc, Ic), and Ve close to required values. What is the % error between the simulated Vb and the value calculated using the voltage divider relation (Vcc, R1, R2). Remember that the voltage divider equation assumes NO LOAD.

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| --- | --- |
| Vc = 5.17  Ic = 0.0094  Ve = 0.94  Vb = 1.65  % error = 2.95% | Vc = 2.7  Ic = 0.0092  Ve = 7.01  Vb = 6.36  % error = 0.95% |

1. What observation can you make about the values for R1, R2, RC, and RE for the PNP design relative to the values determined for the NPN design?

Re and Rc remain swap values and do R1 and R2, for PNP relative to the NPN design.

1. If a -8V supply was available, could the NPN design be converted to the PNP design be changing ONLY the device and by replacing the 8V supply with a -8V supply?

No.

AC Analysis with LTSpice

1. Do a .AC simulation (decade, 10 pts per decade) from 1 Hz to 100 MHz. What is the midband gain in dB (at 10KHz)?

|  |  |
| --- | --- |
| NPN  @10Hz -> gain = 9dB | PNP  @10Hz -> gain = 9dB |

From this value, calculate numerical voltage gain and state the phase that goes with the gain.

|  |  |
| --- | --- |
| NPN  G = 20 log (Vout/Vin)  G/20 = log(Vout/Vin)  10^(G/20) = Vout/Vin  Vout/Vin = 10^(5/20)  Vout/Vin = 1.78 V/V  Phase Shift = -120 | PNP  G = 20 log (Vout/Vin)  G/20 = log(Vout/Vin)  10^(G/20) = Vout/Vin  Vout/Vin = 10^(5/20)  Vout/Vin = 1.78 V/V  Phase Shift = -120 |

What are the approximate –3 dB frequencies low and high. Include a screen shot in your report.

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| --- | --- |
| NPN  High -> 12.6 Hz  Low -> 187.3 MHz | PNP  High -> 12.8 Hz  Low -> 169.2 MHz |

1. Do a .TRAN simulation with frequency = 1 KHz and amplitude = 1V. This is about the largest amplitude possible with this design. Include a screen shot with your report.

|  |  |
| --- | --- |
| NPN | PNP |

Building the Amplifiers

1. Build circuit with NPN (2N3904) transistor. Note that the exact resistor values you calculated may not be available. Consult the TA for values that are close enough. Pay attention to the polarity on the capacitors – the caps you will use are polarized electrolytics, not ideal caps as in LTSpice. For C1/C3, the negative side is on the left. Try to architect the circuit reasonably “small” for the loop made up of the following components: supply filter capacitor, Rc, transistor, Re
2. Measure Vc, Vb, Ve. Calculate Ic. Compare Ic and Vc to your goals.

Vc = 4.98

Vb = 1.66

Ve = 0.98

Ic = (8-4.98)/330 = 9.13 mA

1. With function generator and scope, measure small signal midband gain / phase with output at collector, then f3dB low, and if possible f3dB high.

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Frequecny | Vin | Vout | Gain | Phase |
| 1 | 1 | 0.3 | -10.4576 | 92 |
| 5 | 1 | 1.44 | 3.16725 | 96 |
| 10 | 1 | 1.9 | 5.575072 | 127 |
| 100 | 1 | 3.18 | 10.04854 | 176 |
| 500 | 1 | 3.22 | 10.15712 | 178 |
| 1k | 1 | 3.22 | 10.15712 | 179 |
| 5k | 1 | 3.22 | 10.15712 | 180 |
| 10k | 1 | 3.22 | 10.15712 | 180 |
| 50k | 1 | 3.38 | 10.57833 | 180 |
| 100k | 1 | 3.44 | 10.73117 | 180 |
| 1M | 1 | 3.38 | 10.57833 | 195 |
| 5M | 1 | 2.28 | 7.158697 | 238 |
| 10M | 1 | 1.42 | 3.045767 | 259 |

Mindband gain = 10 dB

F3dB low = 5 Hz

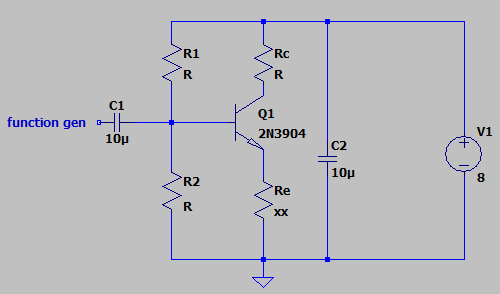
F3dB high = 10 MHz

1. What is the gain with output taken at the emitter?

Mindband Gain (@10 kHz) = -0.291 dB

1. What is the max ppk output level at 1 KHz without significant distortion (on collector).

Max ppk @ 1 KHz 🡺 2.3 Vpp



1. Build circuit with PNP transistor (2N3906).
2. Repeat measurements done on NPN transisitor for the PNP transisitor.

Vc = 3.05

Vb = 6.4

Ve = 7.12

Ic = 3.05/330 = 9.24 mA

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Frequecny | Vin | Vout | Gain | Phase |
| 1 | 1 | 0.344 | -9.26883 | 107 |
| 5 | 1 | 1.08 | 0.668475 | 128 |
| 6 | 1 | 1.38 | 2.797582 | 120 |
| 10 | 1 | 1.72 | 4.710569 | 131 |
| 100 | 1 | 2.98 | 9.484325 | 172 |
| 500 | 1 | 3.02 | 9.600139 | 178 |
| 1k | 1 | 3.02 | 9.600139 | 179 |
| 5k | 1 | 3.04 | 9.657472 | 180 |
| 10k | 1 | 3.06 | 9.714429 | 180 |
| 50k | 1 | 3.22 | 10.15712 | 180 |
| 100k | 1 | 3 | 9.542425 | 171 |
| 1M | 1 | 3.12 | 9.883092 | 195 |
| 5M | 1 | 2.04 | 6.192603 | 243 |
| 10M | 1 | 1.27 | 2.076074 | 266 |

Mindband gain = 10 dB

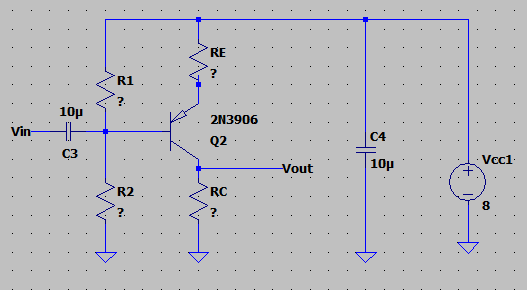
F3dB low = 6 Hz

F3dB high = 10 MHz

Mindband Gain (@10 kHz) = -0.283 dB

Max ppk @ 1 KHz 🡺 1.9 Vpp

1. Why do we *need* C1/C3 between the function generator and the base bias resistors?



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