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Date Submitted: _____01-25-2024_____ Time Submitted _____4:16_pm_____

CSE 3341 Digital Logic Design II

CSE 5357 Advanced Digital Logic Design

Spring Semester 2024

Lab Assignment #1 – Knight Rider Flasher

Due Date – January 25, 2024 (11:59 PM)

Submit on Canvas Assignments

DESIGN REQUIREMENTS

Design in SystemVerilog, implement on the DE10-Lite, and demonstrate a sequential machine that flashes the red LEDs on the DE10-Lite in a continuous back and forth pattern reminiscent of the action lights on the Knight Rider's Firebird Trans Am, KITT. Once you complete this assignment, you will have demonstrated an ability to design and model sequential logic circuits in SystemVerilog that meet specified requirements and to implement the design using a Field Programmable Gate Array (FPGA) employing the following features.

- Clock_50 50-MHz clock
- On/Off toggle
- Clock divider
- Up/Down counter
- Binary to 7-segment decoder
- Module instantiation
- Pin assignment

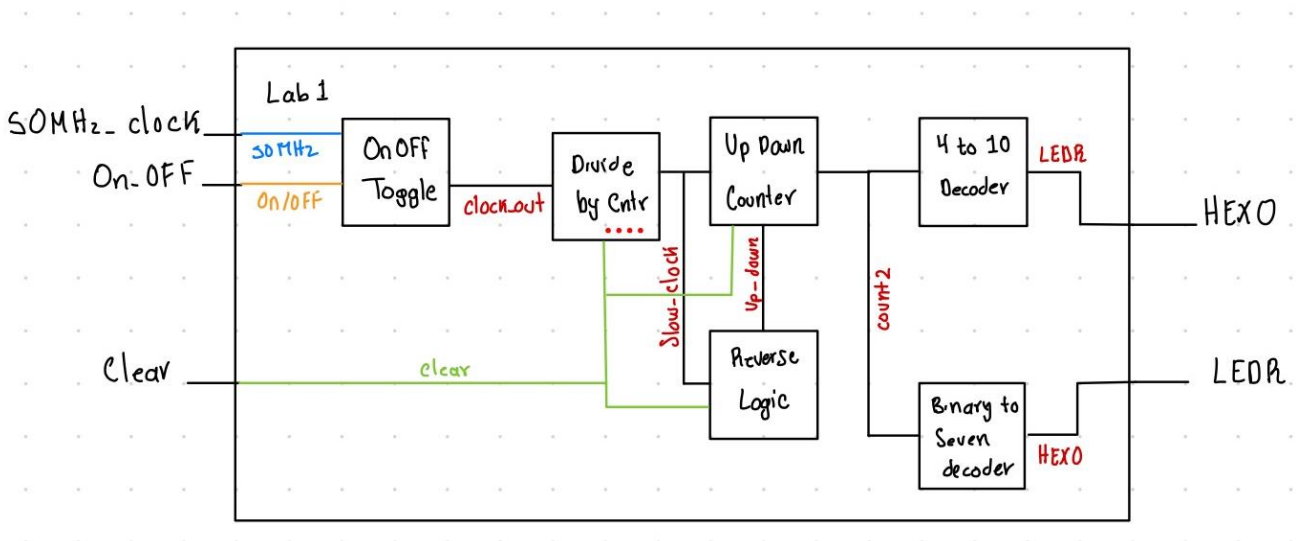
The DE10-Lite board provides a 50-MHz clock (CLOCK_50) that can be used as the time-based for the Flasher. You will need to design a clock divider to provide an appropriate frequency for the machine. The LEDs should flash in a continuous back and forth pattern, reversing direction about once per second, twice per second, and once every two seconds. An up/down counter can be used to realize the LED output pattern. Employ an on/off toggle for your On/Off switch.

Design, implement, and demonstrate the sequential machine described above. Your design must employ a top-down approach and include the following modules.

- Top level
- On/off toggle
- Clock divider
- Up/down counter
- Seven-segment decoder

Lower-level modules should be instantiated in the top-level module.

HIERARCHY DIAGRAM



SYSTEM VERILOG CODE FOR ALL MODULE

- Top Module

```
1  module Lab1
2  (
3      input CLK, ON_OFF, CLEAR,
4      output [9:0] LEDR,
5      output [0:6] HEX0
6  );
7
8      logic clock_out;
9
10     OnOffToggle toggle
11     (
12         .OnOff(ON_OFF),
13         .IN(CLK),
14         .OUT(clock_out)
15     );
16
17     logic slow_clock, up_down;
18     logic [3:0] count1, count2;
19
20     // 5000000 --> Once every sec
21     // 2500000 --> Twice every sec
22     // 10000000 --> Once every 2 sec
23
24     divideXN #(5000000, 32) divByCntr
25     (
26         .CLK(clock_out),
27         .CLEAR(CLEAR),
28         .COUNT(count1),
29         .OUT(slow_clock)
30     );
31
32     reverseLogic RvrsLgd
33     (
34         .CLK(slow_clock),
35         .CLEAR(CLEAR),
36         .UP_DOWN(up_down)
37     );
38
39     decadeUpDownCounter UpDwnCntr
40     (
41         .CLK(slow_clock),
42         .CLEAR(CLEAR),
43         .UP(up_down),
44         .COUNT(count2)
45     );
46
47     four2ten fourDecoder
48     (
49         .BIN(count2),
50         .OUT(LEDR)
51     );
52
53     binary2seven B2Sev
54     (
55         .BIN(count2),
56         .SEV(HEX0)
57     );
58
59 endmodule
```

- On and Off Toggle Module

```

1 module OnOffToggle
2   (
3     input OnOff, IN,
4     output OUT
5   );
6   reg state, nextstate;
7   parameter ON = 1'b1, OFF = 1'b0;
8   always @ (negedge OnOff)
9     state <= nextstate;
10  always @ (state)
11    case(state)
12      OFF: nextstate = ON;
13      ON: nextstate = OFF;
14    endcase
15  assign OUT = state*IN;
16 endmodule

```

- Divide By Counter Module

```

1 module divideXN #(parameter N = 10, parameter M = 4) // 5,000,000 for 1 sec
2   (
3     input CLK, CLEAR,
4     output logic [M-1:0] COUNT, // COUNT is defined as a M-bit register
5     output logic OUT
6   );
7   always_ff @ (negedge CLK, negedge CLEAR)
8     if (CLEAR == 1'b0) COUNT <= 0; // COUNT is loaded with all 0's
9   else
10    begin
11      if (COUNT == N-2'd2) begin OUT <= 1'b1; COUNT <= N-1'd1; end // Once COUNT = N-2 OUT = 1
12    else
13      if (COUNT == N-1'd1) begin OUT <= 1'b0; COUNT <= 0; end // Once COUNT = N-1 OUT=0
14      else begin OUT <= 1'b0; COUNT <= COUNT + 1'b1; end // COUNT is incremented
15    end
16 endmodule

```

- Reverse Logic

```

1 // Toggle output every 10 clock cycles
2
3 module reverseLogic
4   (
5     input CLK, CLEAR,
6     output logic UP_DOWN
7   );
8   logic [3:0] counter = 4'b0;
9
10  always_ff @(negedge CLK, negedge CLEAR) begin
11    if(CLEAR == 1'b0) begin
12      counter <= 4'b0;
13      UP_DOWN <= 1'b0;
14    end else begin
15      counter <= counter + 4'b1;
16
17      if(counter == 4'd8) begin // 9 does one more cylce than require
18        UP_DOWN <= ~UP_DOWN; // so had to go w 8
19        counter <= 4'b0;
20      end
21    end
22  end
23 end
24
25 endmodule

```

- Up Down Counter Module

```

1 module decadeUpDownCounter
2   (
3     input CLK, CLEAR, UP,
4     output logic [3:0] COUNT
5   );
6
7   always_ff @ (negedge CLK, negedge CLEAR)
8   if (CLEAR == 1'b0) begin
9     COUNT <= 4'b0;
10  end else begin
11    if (UP == 0)
12      COUNT <= COUNT + 1'b1;    // if UP increment by 1
13    else
14      COUNT <= COUNT - 1'b1;    // else, decrease by 1
15  end
16 endmodule

```

- Decoder (4-10) Module

```

1 module four2ten
2   (
3     input [3:0] BIN,
4     output logic [9:0] OUT
5   );
6   always_comb
7   case ({BIN[3:0]})
8     4'b0000: {OUT[9:0]} = 10'b0000000001;
9     4'b0001: {OUT[9:0]} = 10'b0000000010;
10    4'b0010: {OUT[9:0]} = 10'b0000000100;
11    4'b0011: {OUT[9:0]} = 10'b0000001000;
12    4'b0100: {OUT[9:0]} = 10'b0000010000;
13    4'b0101: {OUT[9:0]} = 10'b0000100000;
14    4'b0110: {OUT[9:0]} = 10'b0001000000;
15    4'b0111: {OUT[9:0]} = 10'b0010000000;
16    4'b1000: {OUT[9:0]} = 10'b0100000000;
17    4'b1001: {OUT[9:0]} = 10'b1000000000;
18    default: {OUT[9:0]} = 10'b0000000000;
19  endcase
20 endmodule

```





















- Decoder (10-7 seg) Module

```

1 module binary2seven
2   (
3     input [3:0] BIN,
4     output logic [0:6] SEV
5   );
6   always_comb
7   case ({BIN[3:0]})
8     4'b0000: {SEV[0:6]} = 7'b0000001;    //0
9     4'b0001: {SEV[0:6]} = 7'b1001111;    //1
10    4'b0010: {SEV[0:6]} = 7'b0010010;    //2
11    4'b0011: {SEV[0:6]} = 7'b0000110;    //3
12    4'b0100: {SEV[0:6]} = 7'b1001100;    //4
13    4'b0101: {SEV[0:6]} = 7'b0100100;    //5
14    4'b0110: {SEV[0:6]} = 7'b0100000;    //6
15    4'b0111: {SEV[0:6]} = 7'b0001111;    //7
16    4'b1000: {SEV[0:6]} = 7'b0000000;    //8
17    4'b1001: {SEV[0:6]} = 7'b0001100;    //9
18    4'b1010: {SEV[0:6]} = 7'b0001000;    //A
19    4'b1011: {SEV[0:6]} = 7'b1100000;    //b
20    4'b1100: {SEV[0:6]} = 7'b0110001;    //C
21    4'b1101: {SEV[0:6]} = 7'b1000010;    //d
22    4'b1110: {SEV[0:6]} = 7'b0110000;    //E
23    4'b1111: {SEV[0:6]} = 7'b0111000;    //F
24  endcase
25 endmodule

```

DE-10 PIN ASSIGNMENT

| | tatu | From | To | Assignment Name | Value | Enabled | Entity | Comment | Tag |
|----|------|---------|---|-----------------|---------|---------|--------|---------|-----|
| 1 | ✓ | |  CLK | Location | PIN_P11 | Yes | | | |
| 2 | ✓ | |  ON_OFF | Location | PIN_B8 | Yes | | | |
| 3 | ✓ | |  HEX0[0] | Location | PIN_C14 | Yes | | | |
| 4 | ✓ | |  HEX0[1] | Location | PIN_E15 | Yes | | | |
| 5 | ✓ | |  HEX0[2] | Location | PIN_C15 | Yes | | | |
| 6 | ✓ | |  HEX0[3] | Location | PIN_C16 | Yes | | | |
| 7 | ✓ | |  HEX0[4] | Location | PIN_E16 | Yes | | | |
| 8 | ✓ | |  HEX0[5] | Location | PIN_D17 | Yes | | | |
| 9 | ✓ | |  HEX0[6] | Location | PIN_C17 | Yes | | | |
| 10 | ✓ | |  LEDR[0] | Location | PIN_A8 | Yes | | | |
| 11 | ✓ | |  LEDR[1] | Location | PIN_A9 | Yes | | | |
| 12 | ✓ | |  LEDR[2] | Location | PIN_A10 | Yes | | | |
| 13 | ✓ | |  LEDR[3] | Location | PIN_B10 | Yes | | | |
| 14 | ✓ | |  LEDR[4] | Location | PIN_D13 | Yes | | | |
| 15 | ✓ | |  LEDR[5] | Location | PIN_C13 | Yes | | | |
| 16 | ✓ | |  LEDR[6] | Location | PIN_E14 | Yes | | | |
| 17 | ✓ | |  LEDR[7] | Location | PIN_D14 | Yes | | | |
| 18 | ✓ | |  LEDR[8] | Location | PIN_A11 | Yes | | | |
| 19 | ✓ | |  LEDR[9] | Location | PIN_B11 | Yes | | | |
| 20 | ✓ | |  CLEAR | Location | PIN_A7 | Yes | | | |
| 21 | | <<new>> | <<new>> | <<new>> | | | | | |

DEMOED IN PERSON

Demoed on 01/24/2024

To: TA (Madison)