A screenshot of a computer program

Description automatically generated

**(a) Minimum Data Required Time (DRT)**  
MinDRT = Period + CLKtoNOT + NOTdelay + NOTtoCLK – SETUP  
 = 20ns + 1ns + 4ns + 1ns – 4ns = 22ns  
**(b) Maximum Data Arrival Time (DAT)**  
MaxDAT = ClocktoCLK + CLKtoQ + REGtoAdder + AddTime + AddertoReg  
 = 2ns + 8ns + 2ns + 20ns + 2ns = 34ns  
**(c) Setup Slack**  
SetupSlack = MinDRT – MaxDAT

= 22ns – 34ns = -12ns  
**(d) Maximum Clock Frequency**  
Tmin = Period – SetupSlack

= 20ns – (-12ns) = 20ns + 12ns = 32ns  
Fmax = 1/Tmin

= 1/32ns = 31.25MHz

A diagram of a circuit

Description automatically generated

A diagram of a block diagram

Description automatically generated

Add time = 2tg + 2tg + 4\*2tg = 12tg

CLA add time = 2tg + 2tg + 4tg = 8tg

A diagram of a number of numbers

Description automatically generated with medium confidence

A diagram of a block diagram

Description automatically generated

A diagram of a flowchart

Description automatically generated

A diagram of a flowchart

Description automatically generated

One clock cycle where tCYCLE = 2tMUX and tMUX is the propagation delay of a multiplexer (2x1)

A diagram of a flowchart

Description automatically generated

A number is normalized when the integer portion of the mantissa is 1.

+ infinity = 0 | 1111 1111 | 000 0000 0000 0000 0000 0000

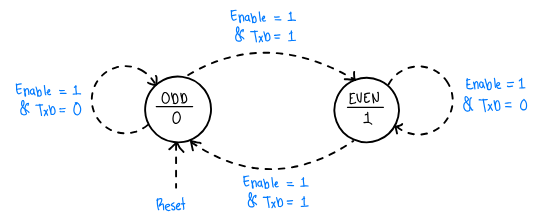
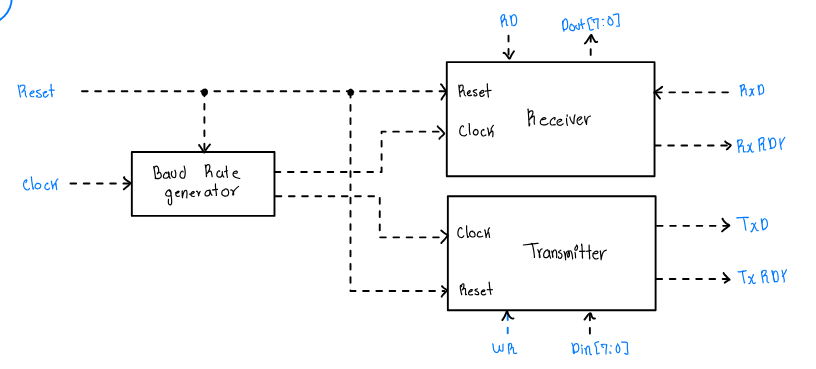
- infinity = 1 | 1111 1111 | 000 0000 0000 0000 0000 0000

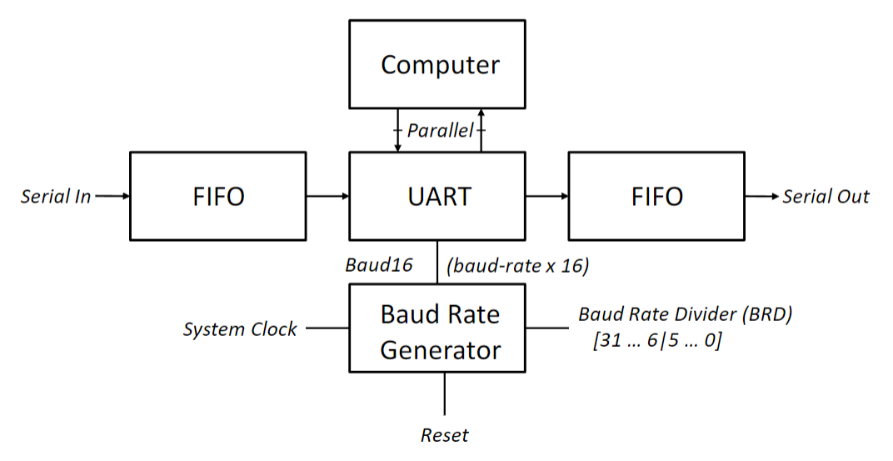
A screenshot of a computer program

Description automatically generated

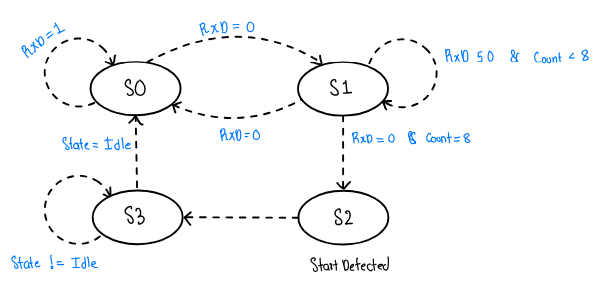
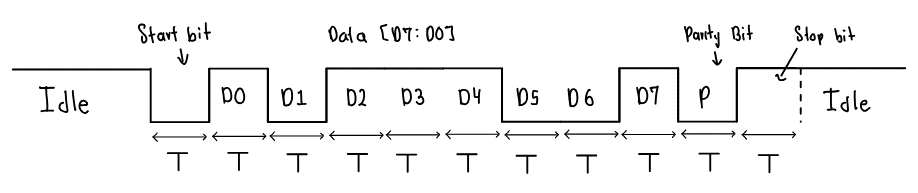
A diagram of a formula

Description automatically generated

A diagram of a data stack

Description automatically generatedA diagram of a computer component

Description automatically generatedA screenshot of a computer code

Description automatically generated

If both the Write and Read Pointer point to the bottom of the buffer (Address 0) it means that the buffer is EMPTY. Can be caused by a clear.

If the Write pointer points to the top of the buffer and the Read pointer points to the bottom, it means that the buffer is FULL.

**Data Organization FIFO Buffer**

**UART Diagram**

**Buffered UART Block Diagram**

Buffering a UART helps regulate the incoming and outgoing flow of data; ensures that bursts of data can be handled properly without any loss or overflow of it.

**Synchronous FIFO Buffer**

**Empty state** – PtrDiff = 0  
**Full state** – PtrDiff = StackHt  
**Overflow state** – PtrDiff > StackHt  
**Read state** – Read & PtrDiff > 0  
**Write state** – Write & PtrDiff < StackHt

**Receiver Controller SystemVerilog Module**

T = 1/fBaud

**UART Serial Data Format**

**Sampling and Detecting Start-Bit State Diagram**

**Parity Generator State Diagram**

**Assuming ODD parity**