A diagram of a line graph

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Description automatically generatedA computer code with numbers and symbols

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Clock Ladder

Input Clock Frequency= ƑCLK

Ƒy0 =

Ƒy1 =

Ƒy2 = Ƒyn =

Ƒy3 =

CLA4 carry

c0 = cin

c1 = p0c0 + g0

c2 = p1c1 + g1

c3 = p2c2 + g2

c4 = p3c3 + g3

Sync a clock to an async input like a switch can lead to multiple reads per clock pulse, or unpredictable behavior by the switch. Solutions:

- Slow the clock speed to control unit

- Add transition states

- Use edge detection on switch

Multiplexed displays Advantages:

- fewer pin assignments required

- Simpler and shorter code

- easier to implement

- separate Anodes as supposed to single

- less wiring than non-multiplexed

- more efficient

Disadvantages:

- clock rate for cycling thru digits must be set, otherwise flickering

- dimmer than non-multiplexed displays

\* **Data Arrival Time** (**DAT**): the time it takes for the data to arrive at the destination register input.

- Max

- Min

\* **Clock Arrival Time** (**Tclk**) : the time it takes for the clock to arrive at the destination register

- Max

- Min

\* **Data Required Time** (**setup**) = Clock Arrival Time – Setup Time

- Max

- Min

\* **Data Required Time** (**hold**): = Clock Arrival Time + Hold Time

- Max

- Min

\* **Setup slack** = clock period + minimum data required time – max data arrival time

*Dependent on frequency!*

\* **Hold slack** = minimum data arrival time – max data required time

*NOT dependent on frequency!*

\* **Max clock frequency**

new period = clock period + |setup slack|

TMIN = DATMAX + Setup Time - TclkMIN

FMAX =

\* If setup slack < 0, then logic design is rather slow. Fix by increasing the period, or, in other words, decreasing frequency.

CLA Equations

S = A ⊕ B ⊕ Cin

Cout = a’bcin + b’acin + abcin’ + abcin

= (a’b + ab’)cin + ab(cin + cin’)

= (a ⊕ b)cin + ab

= pcin + g

p = a ⊕ b

g = ab

In a 4x4 keypad scanning algo. Upon pressing any of the buttons on a given row, this one will send a signal to the Keypad Scanner & Encoder. Then columns are scanned. Having both the row and column, the specific button that was pressed can be determined. Code corresponding to button is outputted, along w a signal that tell whether code is ready.

Overflow creates the wrong sign bit.

1. When adding two (+) numbers that yield a (-) number

2. When adding two (-) numbers that yield a (+) number

i.e. 7 + 7 ≠ -2 -8 + -8 ≠ 0

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For 4 chained CLAs

Add Time = 4tg + 4tg + 4tg + 4tg

One CLA4: takes 1tg to compute propagate and generate; takes 2tg to compute Cout (2 logic gates needed); and computing sum takes 1tg.

1 CLA4 Add Time = 4tg­

A screenshot of a computer code

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A screenshot of a computer program

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For an n-bit ripple carry adder, the add time is 2\*n\*tg

A screen shot of a computer code

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A computer screen shot of a computer code

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