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| Name: \_\_\_\_\_Servando\_Olvera\_\_\_\_\_\_\_\_ ID# \_\_\_\_\_\_\_\_1001909287\_\_\_\_\_\_\_    Date Submitted: \_\_\_\_\_02-06-2024\_\_\_\_ Time Submitted \_\_\_\_\_9:00\_pm\_\_\_\_\_\_    CSE 3341 Digital Logic Design II    CSE 5357 Advanced Digital Logic Design    Spring Semester 2024    **Lab 2 –Multiplexed Seven-Segment Displays**  Due Date – February 6, 2024, 11:59 PM    Submit on Canvas Assignments |

**DESIGN REQUIREMENTS**

Design a decoder/controller for the *HexBoard* four-digit multiplexed seven segment display. Capture your design using SystemVerilog. Realize your design on the DE10-Lite + HexBoard devices found in your ADL Lab Kit. In Part A, you will test your decoder/controller by displaying, in hexadecimal, the output of a 16-bit binary counter as shown in Figure 1. In Part B, you will use the *HexBoard* to display a crawling message. This can be realized by replacing the 16-bit counter with a circular buffer as shown in Figure 2.

* SystemVerilog must be used for coding the solutions.
* Structured design must be used and documented by a hierarchy diagram.
* Code must be commented.

## **Part A – Multiplexed seven-segment decoder/controller**

1. Design and implement the circuit in Figure 1.
2. Demonstrate that the counter counts and displays properly from 0000 to FFFF and repeats.
3. Demonstrate that the On/Off and Reset features work.
4. Mathematically derive the count rate and mux rate for the clock ladder settings in Figure 1.
5. Add a feature that allows the mux rate to be controlled from the DE10-Lite+HexBoard switches and pushbuttons.
6. Experimenally determine the slowest mux rate that does not produce flicker on the display.
7. Does speeding up the mux rate from this minimum improve the display?

## **Part B – Crawling message display**

1. Design and implement the circuit in Figure 2.
2. Demonstrate that it can continuously display the message *0123456789AbCdEF* in hex.
3. Increase the crawl rate by a factor of 4 and observe the effect on the display.
4. Reprogram your circular buffer to display the message HELLO 2 YOU.

**HIRERARCHY DIAGRAMS**

**Part A**

**A diagram of a computer

Description automatically generated**

**Part B**

**A diagram of a computer

Description automatically generated**

**SYSTEM-VERILOG CODE**

**Part A Top Module**

**A screenshot of a computer program

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**Part B Top Module**

**A screenshot of a computer program

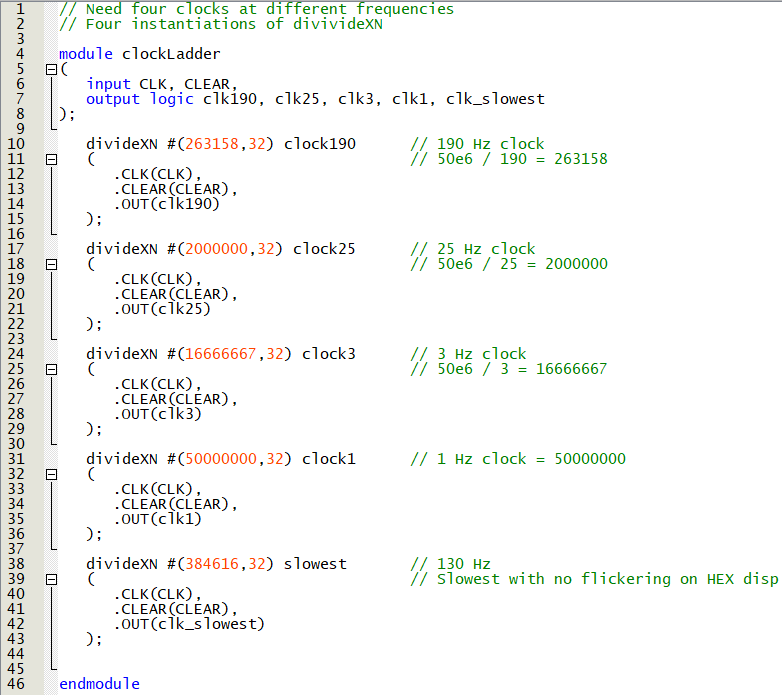
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**ON & OFF Toggle Module**

**A screenshot of a computer screen

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**Clock Ladder Module [Part A]**

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**Clock Ladder Module [Part B]**

**A screenshot of a computer program

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**Clock Rates Module**

**A computer screen shot of text

Description automatically generated**

**16-bit Binary Counter Module [Part A]**

**A screenshot of a computer program

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**Circular Buffer Module [Part B]**

A computer code on a white background

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**MUX Module**

**A screenshot of a computer program

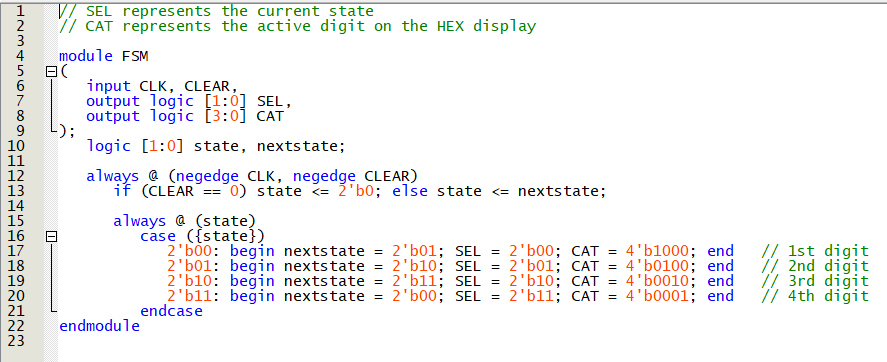
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**Four To One Module**

**A screenshot of a computer program

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**Finite State Machine Module**

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**Binary To 7-Hex & To Message Decoder**

**A screenshot of a computer

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**PIN ASSIGMENTS**

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**SW9 is for part B (I implemented A & B similarly)**

**DEMOED IN PERSON**

**Demoed on 02/05/2024**

**To: TA (Madison)**