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| Name: \_\_\_\_\_Servando\_Olvera\_\_\_\_\_\_\_\_ ID# \_\_\_\_\_\_\_\_1001909287\_\_\_\_\_\_\_    Date Submitted: \_\_\_\_\_03-19-2024\_\_\_\_ Time Submitted \_\_\_\_\_4:00\_pm\_\_\_\_\_\_    CSE 3341 Digital Logic Design II    CSE 5357 Advanced Digital Logic Design    Spring Semester 2024    **Lab 4 – Registered Eight x Eight Signed Multiplier**  **200 points**  Due Date – March 21, 2024, 11:59 PM    Submit on Canvas Assignments  ***Note – Late submissions will not be accepted!*** |

**DESIGN REQUIREMENTS – SIGNED VERSION**

Your assignment is to design a registered eight-by-eight signed multiplier by enhancing the four- by-four unsigned shift-and-add multiplier shown below and discussed in class.

***REQUIREMENTS:***

1. Registered 8 x 8 multiplier  
2. Signed numbers (use 2’s complement for negative numbers)  
3. SystemVerilog implementation  
4. Design verification (simulation)  
5. DE10-Lite realization

***DESIGN VERIFICATION (simulation)***

1. Simulate your designs to verify their correctness. Use the following values for M and Q in  
your simulations.

(a) 01111111 x 00000001  
(b) 00010101 x 00101010  
(b) 01111111 x 11111111  
(c) 10101010 x 00110011  
(d) 10101010 x 11111110  
(e) 11011101 x 11001101

2. Include a screen shot of your simulation waveforms in your report.  
3. Record the simulation results in a table for your report (use hexadecimal)  
4. How many clock cycles does it take for each case to complete?

***RTL ANALYSIS***

1. Generate RTL diagrams using the Quartus Prime Netlist Viewer for each version.  
2. Record the compilation summary for your report. How many ALM, registers, and pins does  
your design require?

***TIMING ANALYSIS***

1. Run a timing analysis on your signed multiplier and determine its maximum operating  
speed in GHz.

2. Capture a screen shot of your timing analysis waveform showing the fastest clock speed  
your design will accommodate.

***DE10-Lite IMPLEMENTATION (signed version only)***

1. Implement your signed multiplier on the DE10-Lite using the following inputs/outputs. Use

pin assignments of your choice

Inputs M, Q, InM, InQ,

Outputs Mout, Qout, Pout. Display in hexadecimal on the HEX displays.

2. Include a table of your pin assignments in your report.  
3. Program the DE10-Lite with your design.

**DATA PATH DIAGRAM**

**A diagram of a data flow

Description automatically generated**

**CONTROL PATH DIAGRAM**

**A diagram of a test

Description automatically generated**

**SYSTEM-VERILOG CODE**

**Top Module**

**A screenshot of a computer screen

Description automatically generated**

**A screenshot of a computer program

Description automatically generated**

**Register Module**

**A screenshot of a computer

Description automatically generated**

**Multiplier Module**

**A screenshot of a computer program

Description automatically generated**

**Multiplier Control Module**

**A computer screen shot of a computer program

Description automatically generated**

**MUX Controller Module**

**A screenshot of a computer program

Description automatically generated**

**Finite State Machine Module**

**A screenshot of a computer program

Description automatically generated**

**MUX/ Four to One Decoder Module**

**A screenshot of a computer program

Description automatically generated**

**Clock Ladder Module**

**A screenshot of a computer code

Description automatically generated**

**Binary to Seven-Seg Display Decoder Module**

**A screenshot of a computer

Description automatically generated**

**SIMULATION RESULTS WAVEFORM**

**A screenshot of a computer

Description automatically generated**

**A screenshot of a computer

Description automatically generated**

**PIN ASSIGMENTS**

**A screenshot of a computer

Description automatically generated**

**A screenshot of a computer

Description automatically generated**

**RTL DIAGRAMS**

**Top Module**

**A diagram of a computer

Description automatically generated**

**Registers A & B**

**A diagram of a computer program

Description automatically generated**

**Multiplier**

**A diagram of a circuit

Description automatically generated**

**Multiplier Control**

A computer diagram of a circuit board

Description automatically generated

**Clock Ladder**

**A computer screen shot of a computer

Description automatically generated**

**Product Register**

**A diagram of a computer

Description automatically generated**

**MUX/Controller**

**A computer screen shot of a computer

Description automatically generated**

**Four to One Decoder**

**A screenshot of a computer

Description automatically generated**

**Binary To Seven Segment Display Decoder (Product)**

**A screenshot of a computer

Description automatically generated**

**Finite State Machine**

**A diagram of a computer

Description automatically generated**

**Binary To Seven Segment Display Decoder**

**(Used 4 times to properly display Mout & Qout)A diagram of a circuit

Description automatically generated**

**Four to One Decoder**

**A screenshot of a computer

Description automatically generated**

# of ALMs = 165

# of REGISTERS = 92

# of PINS = 68

**TIMING ANALYSIS DIAGRAMS**

**A screenshot of a computer

Description automatically generated**

**Max Operating Speed:** ~ 0.19 GHz

**Fastest Clock Speed:** 5.3 ns

**TEST RESULTS**

**Signed Tests**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Test** | **M x Q (Binary)** | **M x Q**  **(Hex)** | **Product**  **(Hex)** | **Clock Cycles** |
| a) | 0111 1111 x 0000 0001 | 7F x 01 | 007F | 20 |
| b) | 0001 0101 x 0010 1010 | 15 x 2A | 0372 | 22 |
| c) | 0111 1111 x 1111 1111 | 7F x FF | FF81 | 27 |
| d) | 1010 1010 x 0011 0011 | AA x 33 | EEDE | 23 |
| e) | 1010 1010 x 1111 1110 | AA x FE | 00AC | 26 |
| f) | 1101 1101 x 1100 1101 | DD x CD | 06F9 | 24 |

**PHOTOS OF TEST RESULTS**

|  |  |
| --- | --- |
| **a)**    P  M  Q | **b)** |
| **c)** | **d)** |
| **e)** | **f)** |