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| Name: \_\_\_\_\_Servando\_Olvera\_\_\_\_\_\_\_\_ ID# \_\_\_\_\_\_\_\_1001909287\_\_\_\_\_\_\_    Date Submitted: \_\_\_\_\_03-21-2024\_\_\_\_ Time Submitted \_\_\_\_\_9:00\_pm\_\_\_\_\_\_    CSE 3341 Digital Logic Design II    CSE 5357 Advanced Digital Logic Design    Spring Semester 2024    **Lab 2 – Registered Eight x Eight Unsigned Multiplier**  **50 points**  Due Date – March 21, 2024, 11:59 PM    Submit on Canvas Assignments  ***Note – Late submissions will not be accepted!*** |

**DESIGN REQUIREMENTS**

Your assignment is to design a registered eight-by-eight unsigned multiplier by enhancing the four- by-four unsigned shift-and-add multiplier shown and discussed in class.

***REQUIREMENTS:***

1. Registered 8 x 8 multiplier  
2. Unsigned numbers  
3. SystemVerilog implementation  
4. Design verification (simulation)  
5. DE10-Lite realization

***DESIGN VERIFICATION (simulation)***

1. Simulate your designs to verify their correctness. Use the following values for M and Q in  
your simulations.

(a) 01111111 x 00000001  
(b) 00010101 x 00101010  
(b) 01111111 x 11111111  
(c) 10101010 x 00110011  
(d) 10101010 x 11111110  
(e) 11011101 x 11001101

2. Include a screen shot of your simulation waveforms in your report.  
3. Record the simulation results in a table for your report (use hexadecimal)  
4. How many clock cycles does it take for each case to complete?

***RTL ANALYSIS***

1. Generate RTL diagrams using the Quartus Prime Netlist Viewer for each version.  
2. Record the compilation summary for your report. How many ALM, registers, and pins does  
your design require?

***TIMING ANALYSIS***

1. Run a timing analysis on your signed multiplier and determine its maximum operating  
speed in GHz.  
2. Capture a screen shot of your timing analysis waveform showing the fastest clock speed  
your design will accommodate.

**DATA PATH DIAGRAM**

**A diagram of a product

Description automatically generated**

**CONTROL PATH DIAGRAM**

**A diagram of a test

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**SYSTEM-VERILOG CODE**

**Top Module**

**A screenshot of a computer program

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**Register Module**

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**Multiplier Module**

**A screenshot of a computer program

Description automatically generated**

**Multiplier Control Module**

**A computer screen shot of a program

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**MUX Controller Module**

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Description automatically generated**

**Finite State Machine Module**

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**Four to One Decoder Module**

**A screenshot of a computer program

Description automatically generated**

**Clock Ladder Module**

**A screenshot of a computer code

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**Binary to Seven-Seg Display Decoder Module**

**A screenshot of a computer

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**SIMULATION RESULTS WAVEFORM**

**A screenshot of a bar code

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**A screenshot of a barcode

Description automatically generated**

**PIN ASSIGMENTS**

**A screenshot of a computer

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**RTL DIAGRAMS**

**Top Module**

**A group of green squares with black lines

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**Multiplicand & Multiplier Registers**

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**Multiplier**

**A diagram of a computer

Description automatically generated**

**Multiplication Control Module**

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**Product Register**

**A diagram of a circuit

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**Clock Ladder A computer screen shot of a computer

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**MUX/Controller**

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**Four to One Decoder**

**A screenshot of a computer

Description automatically generated**

**Binary To Seven Segment Display**

**A screenshot of a computer

Description automatically generated**

**Finite State Machine**

**A diagram of a computer

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**Compilation Summary**

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# of ALMs = 107

# of REGISTERS = 85

# of PINS = 40

**TIMING ANALYSIS DIAGRAM**

**A screenshot of a computer

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**Max Operating Speed:** ~ 0.34 GHz

**Fastest Clock Speed:** 3.0 ns

**TEST RESULTS**

**Usigned Tests**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Test** | **M x Q (Binary)** | **M x Q**  **(Hex)** | **Product**  **(Hex)** | **Clock Cycles** |
| a) | 0111 1111 x 0000 0001 | 7F x 01 | 007F | 22 |
| b) | 0001 0101 x 0010 1010 | 15 x 2A | 0372 | 24 |
| c) | 0111 1111 x 1111 1111 | 7F x FF | 7E81 | 29 |
| d) | 1010 1010 x 0011 0011 | AA x 33 | 21DE | 25 |
| e) | 1010 1010 x 1111 1110 | AA x FE | A8AC | 28 |
| f) | 1101 1101 x 1100 1101 | DD x CD | B0F9 | 26 |

**PHOTOS OF TEST RESULTS**

|  |  |
| --- | --- |
| **a)** | **b)** |
| **c)** | **d)** |
| **e)** | **f)** |