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| Name: \_\_\_\_\_Servando\_Olvera\_\_\_\_\_\_\_\_ ID# \_\_\_\_\_\_\_\_1001909287\_\_\_\_\_\_\_    Date Submitted: \_\_\_\_\_04-27-2024\_\_\_\_ Time Submitted \_\_\_\_\_4:00\_pm\_\_\_\_\_\_    CSE 3341 Digital Logic Design II    CSE 5357 Advanced Digital Logic Design    Spring Semester 2024    **Eight-Bit, Four Function Calculator**  **250+ points**  Due Date – April 30, 2024, 11:59 PM    Submit on Canvas Assignments |

**DESIGN REQUIREMENTS**

**PURPOSE/OUTCOMES**  
To design, implement on the DE10-Lite + KeyPad + HexBoard, and test an eight-bit, four-function (ADD, SUBTRACT, MULTIPLY, DIVIDE) calculator. The calculator can be partitioned in to four components as illustrated in Figure 1. You will perform this project by designing the Control Unit (CU) and integrating it with the Arithmetic Unit (AU), Output Unit (OU), and Input Unit (IU) designed in previous assignments. By successfully completing this project, you will have demonstrated an ability to design, implement, and test a machine that incorporates combinational and sequential logic circuits implemented with field programmable logic arrays (FPGAs) and designed with the SystemVerilog hardware description language (HDL).

**REQUIREMENTS**  
To successfully complete the term project, you must design the CU and integrate it with the IU, AU, and OU and demonstrate it’s functionality with the test inputs specified below.

a. 74 + 35  
b. 74 – 35  
c. –74 – 35  
d. 127 + 6  
e. 10 x 15  
f. 127 x 2  
g. –1 x –1  
h. –127 x –127  
i. 10 ÷ 5  
j. 67 ÷ 32

**INPUT REQUIREMENTS**  
1. Operands must be entered in hexadecimal on the CSE KeyPad 4 x 4 keypad shown in Figure 2.  
2. Control and operations must be entered using pushbuttons as described below.

**NUMBER ENTRY AND OPERATIONS REQUIREMENTS**  
Inputs consist of a sign and up to three magnitude digits. Enter operands and perform operations as follows.

1. Clear the calculator – press Key0 (Clear All)  
2. Capture operand A using the KeyPad  
3. Enter operand Ahigh – press Key1  
4. Enter operand Alow – press Key1  
5. Capture operand B using the KeyPad  
6. Enter the operand B – press Key1  
7. Enter the operation to be performed – add (Key2), subtract (Key3), multiply (Key4), divide (Key5)

**DISPLAY REQUIREMENTS**  
1. Operands and results must be displayed in hexadecimal on the HexBoard.  
2. Results must be displayed in decimal sign-magnitude on the DE10 seven-segment displays after  
calculations are complete.  
3. Operations that produce an oveflow must light LEDR9.  
4. Operations that produce a zero (0) result must light LEDR8.

**CONTROL UNIT REQUIREMENTS**  
The control-path, data-path interface is shown in Figure 3. The control signals are produced by a finite state machine described in Figure 4.

**DESCRIPTION OF ADDED FEATURES**

**N/A**

**No added features.**

**ORGANIZATION DIAGRAM**

**A diagram of a diagram

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**CONTROL UNIT**

**Inputs/Output**

**A diagram of a control unit

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**State Diagram**

A diagram of a computer system

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**TEST RESULTS**

**Summary**

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| Test Case | Inputs  (Decimal) | Expected Result (Decimal) | Expected Result (Hex) | Actual Inputs  (Hex) | Actual  Result | OVR | ZERO |
| a. | 74 + 35 | 109 | 006D | 4A + 23 | 006D | 0 | 0 |
| b. | 74 - 35 | 39 | 0027 | 4A - 23 | 0027 | 0 | 0 |
| c. | -74 - 35 | -109 | FF93 | B6 - 23 | FF93 | 0 | 0 |
| d. | 127 + 6 | 133 | 0085 | 7F + 06 | FF85 | 1 | 0 |
| e. | 10 x 15 | 150 | 0096 | 0A x 0F | 0096 | 0 | 0 |
| f. | 127 x 2 | 254 | 00FE | 7F x 02 | 00FE | 0 | 0 |
| g. | -1 x -1 | 1 | 0001 | FF x FF | 0001 | 0 | 0 |
| h. | -127 x -127 | 16,129 | 3F01 | 81 x 81 | 3F01 | 0 | 0 |
| i. | 10 ÷ 5 | 2|0 | 02|00 | 0A ÷ 05 | 02|00 | 0 | 0 |
| j. | 67 ÷ 32 | 2|3 | 02|03 | 43 ÷ 20 | 02|03 | 0 | 0 |

**Demonstration (Documented Pictures)**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Test Case** | **Input A** | **Input B** | **Op** | **Result** |
| a. |  |  | + |  |
| b. |  |  | - |  |
| c. |  |  | - |  |
| d. |  |  | - |  |
| **e.** |  |  | **+** |  |
| f. |  |  | x |  |
| g. |  |  | x |  |
| h. |  |  | x |  |
| **i.** |  |  | **÷** |  |
| j. |  |  | ÷ |  |

**VERILOG CODE**

**Term Project/ Top Module**

**A screenshot of a computer program

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**Control Unit Module**

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**MUX**

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**Arithmetic Unit Module**

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**Arithmetic Unit Module**

**Clock Ladder Modified Module**

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**Edge Detect Module**

**A computer screen shot of a program

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