Chapter 4

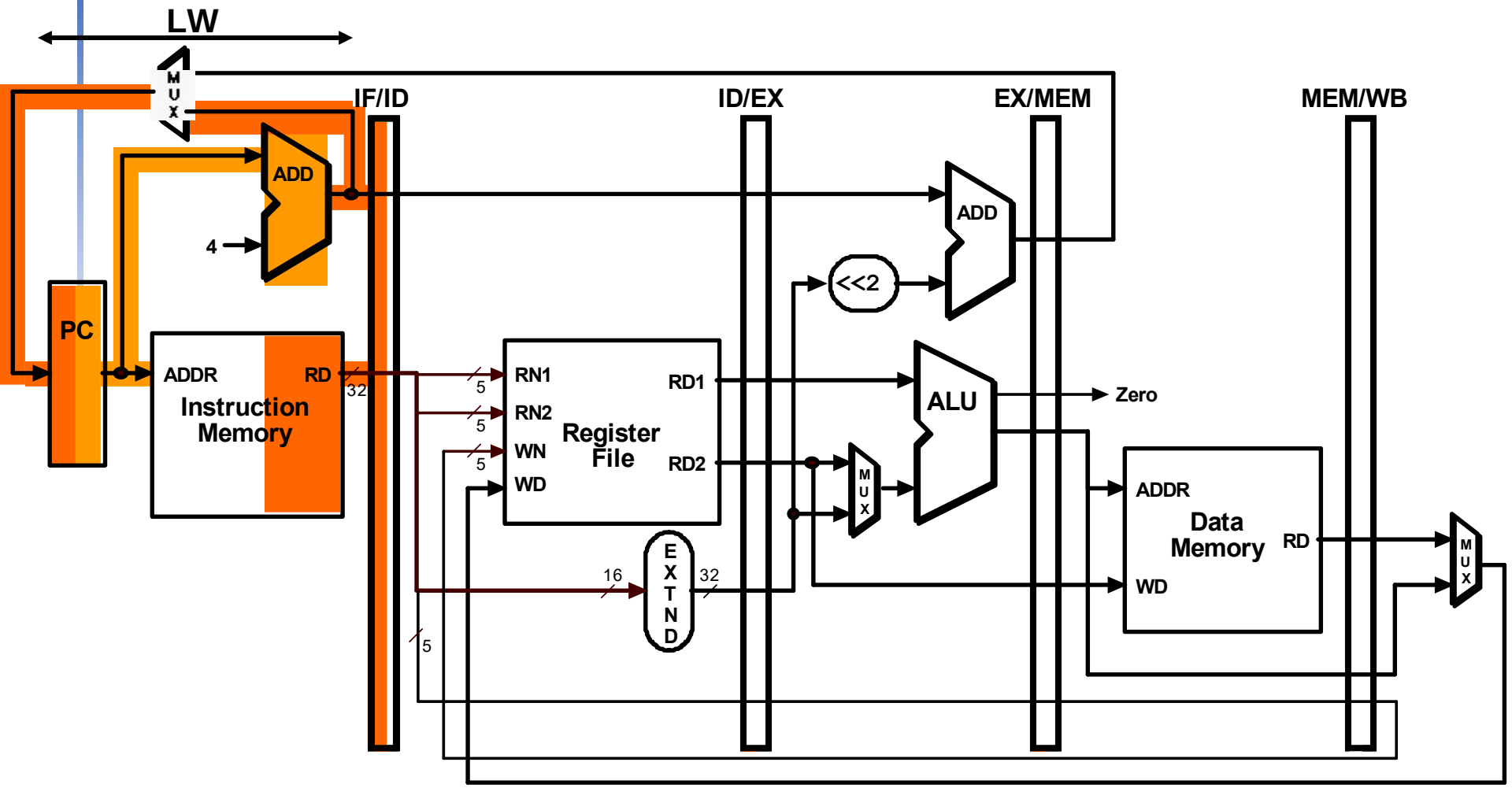
The Processor

Pipelined Example

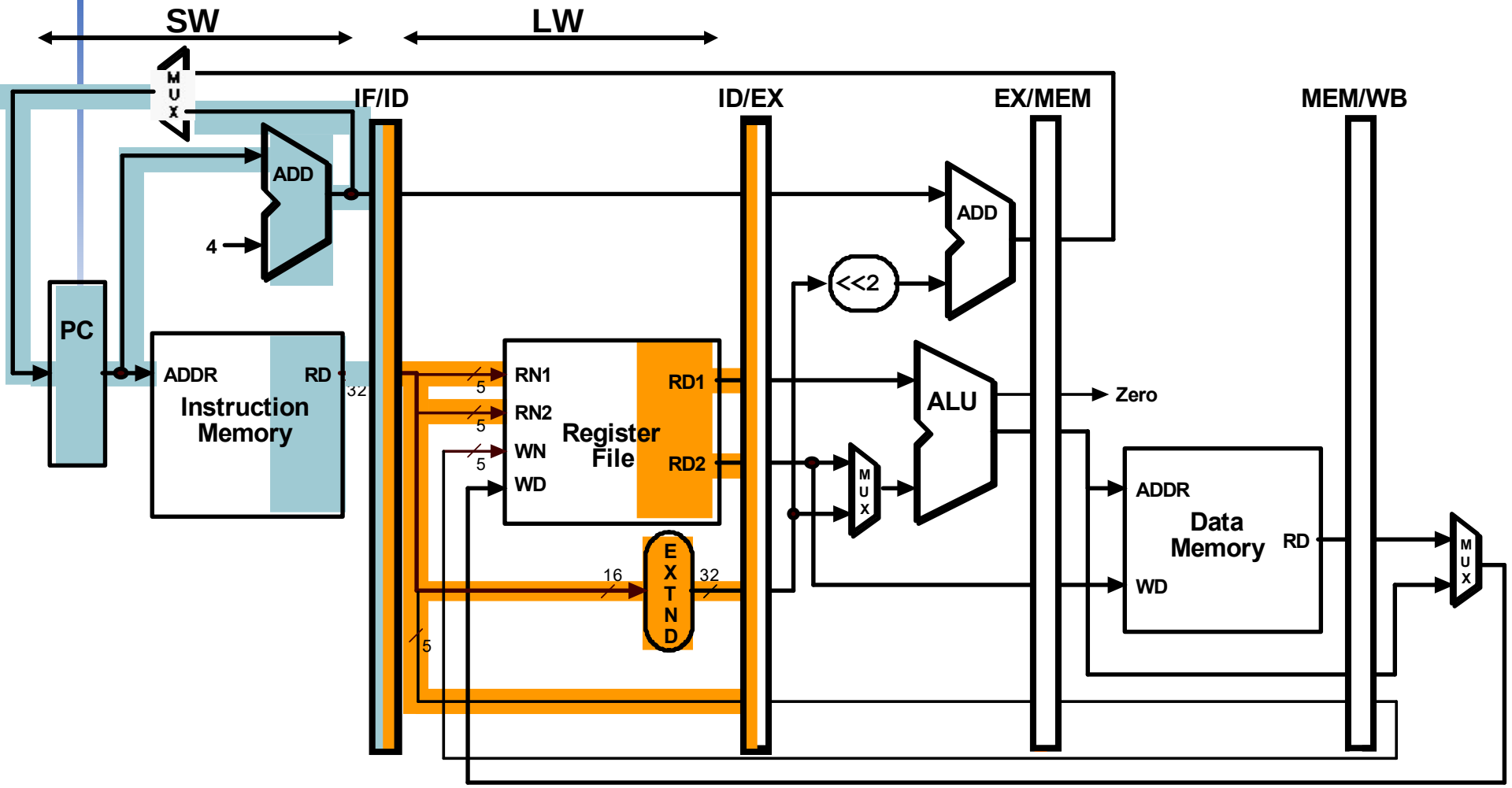
- Consider the following instruction sequence:

```
lw  $t0,  10($t1)
sw  $t3, 20($t4)
add $t5,  $t6,  $t7
sub $t8,  $t9,  $t10
```

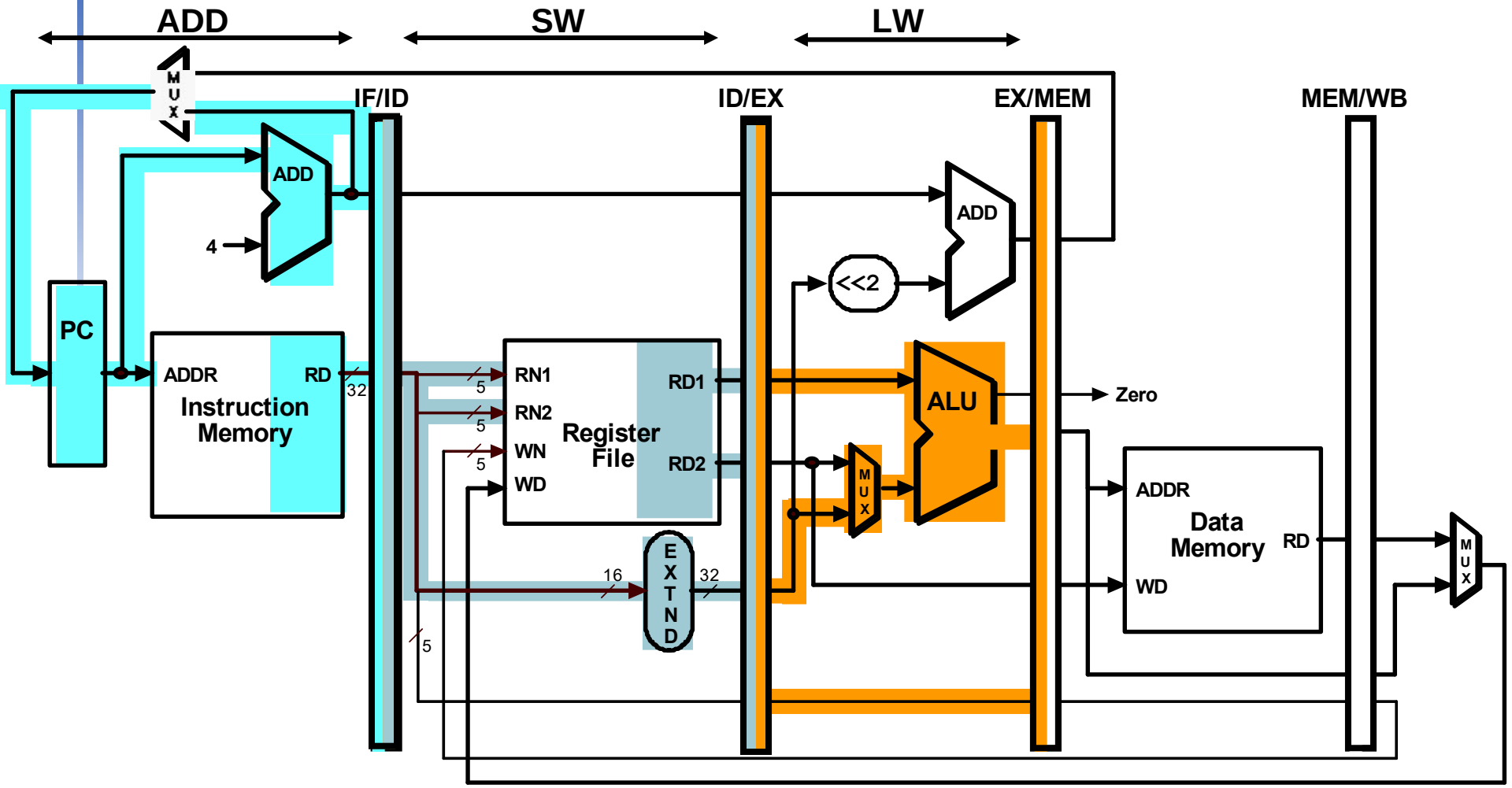
Clock Cycle 1



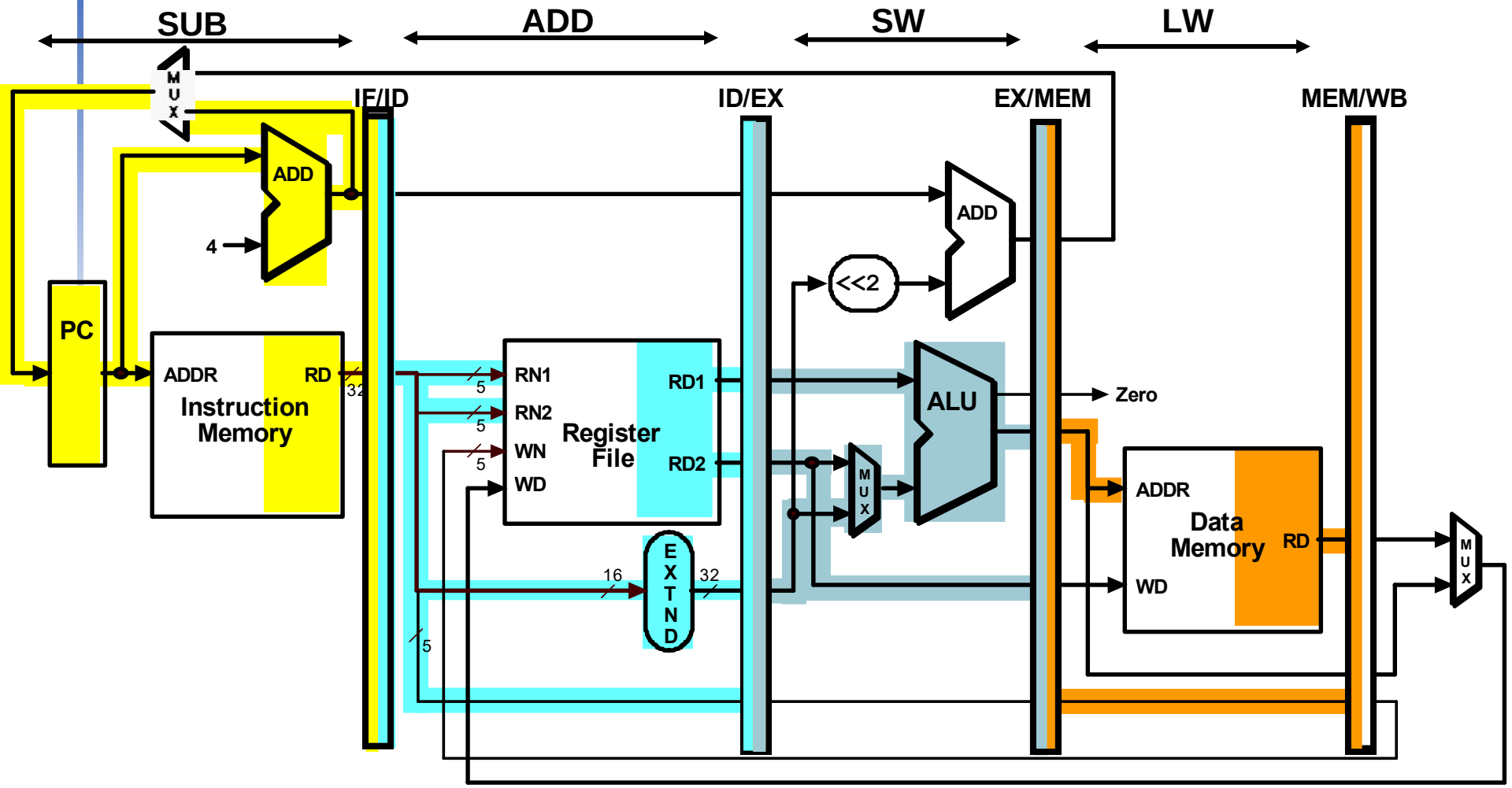
Clock Cycle 2



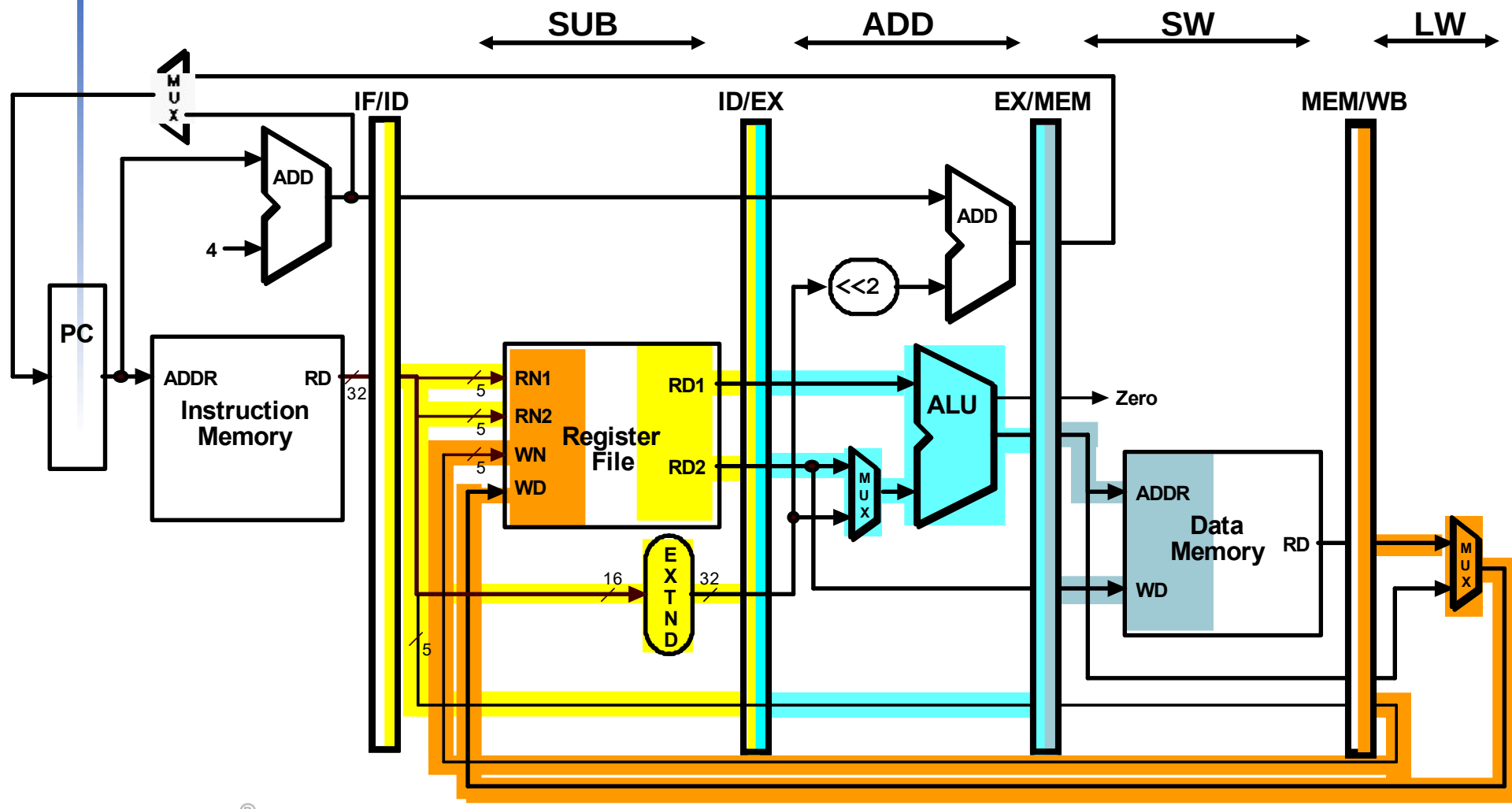
Single Clock Cycle Diagram: Clock Cycle 3



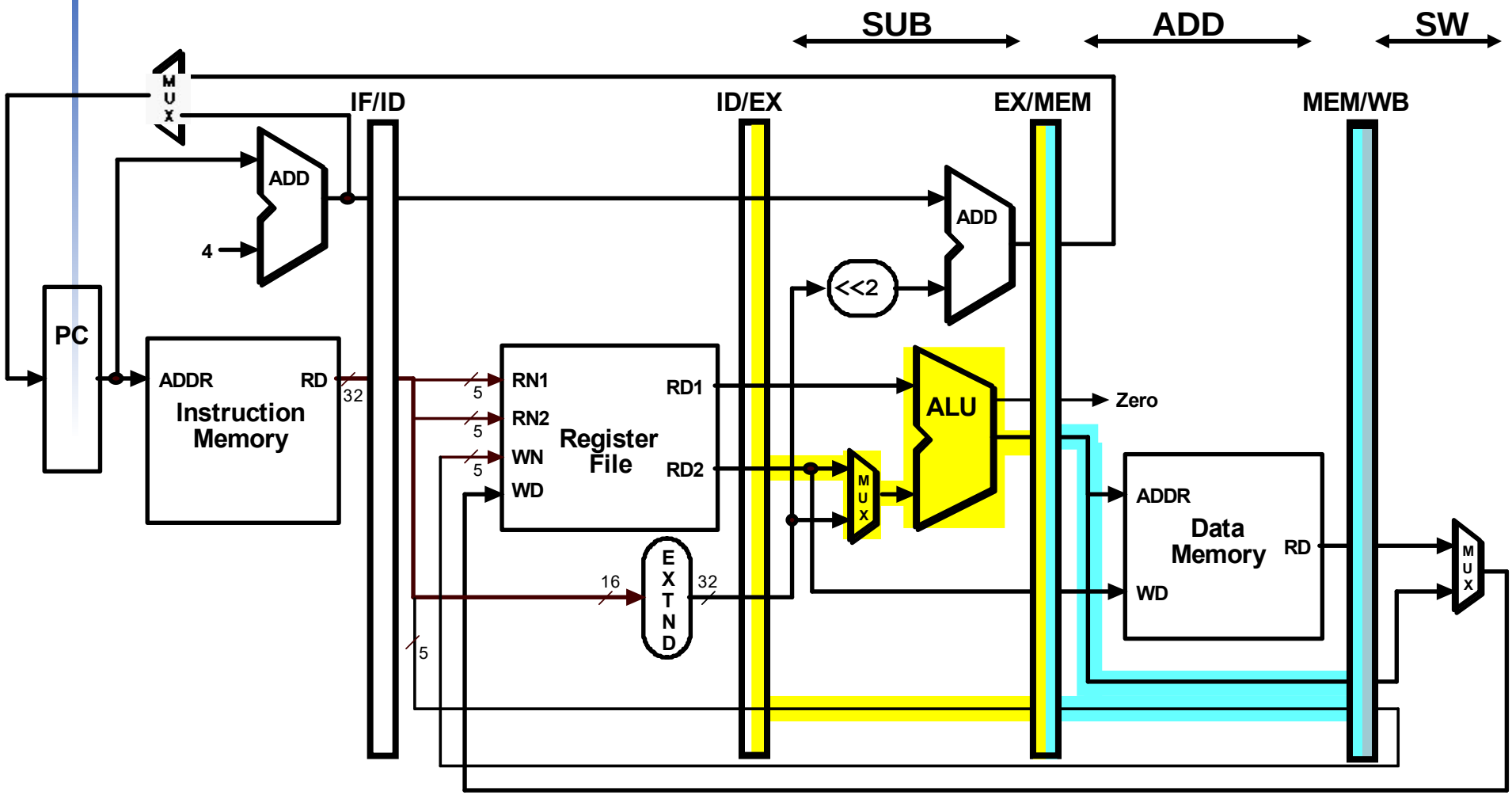
Single Clock Cycle Diagram: Clock Cycle 4



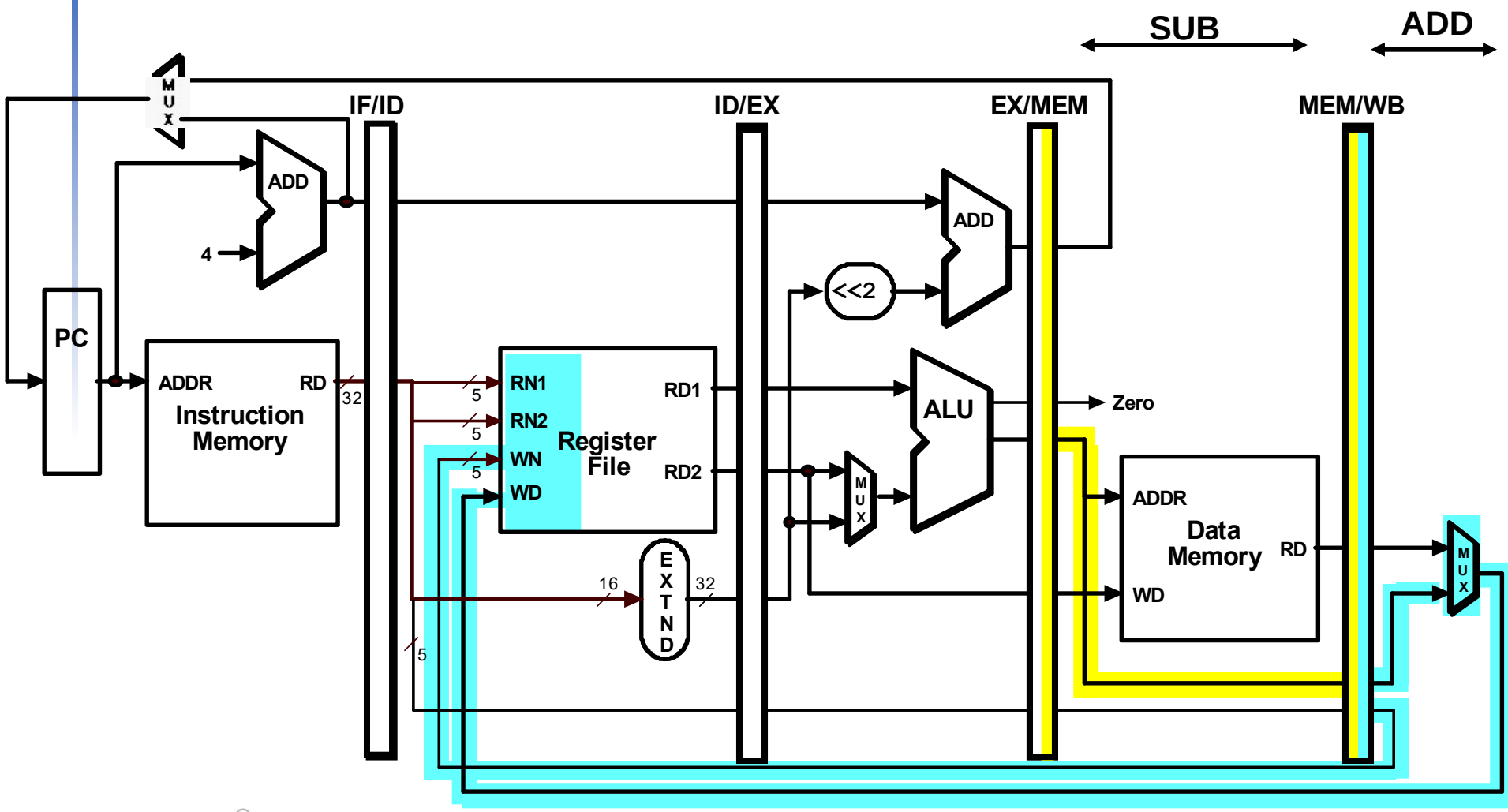
Single Clock Cycle Diagram: Clock Cycle 5



Single Clock Cycle Diagram: Clock Cycle 6



Single Clock Cycle Diagram: Clock Cycle 7



Clock Cycle 8