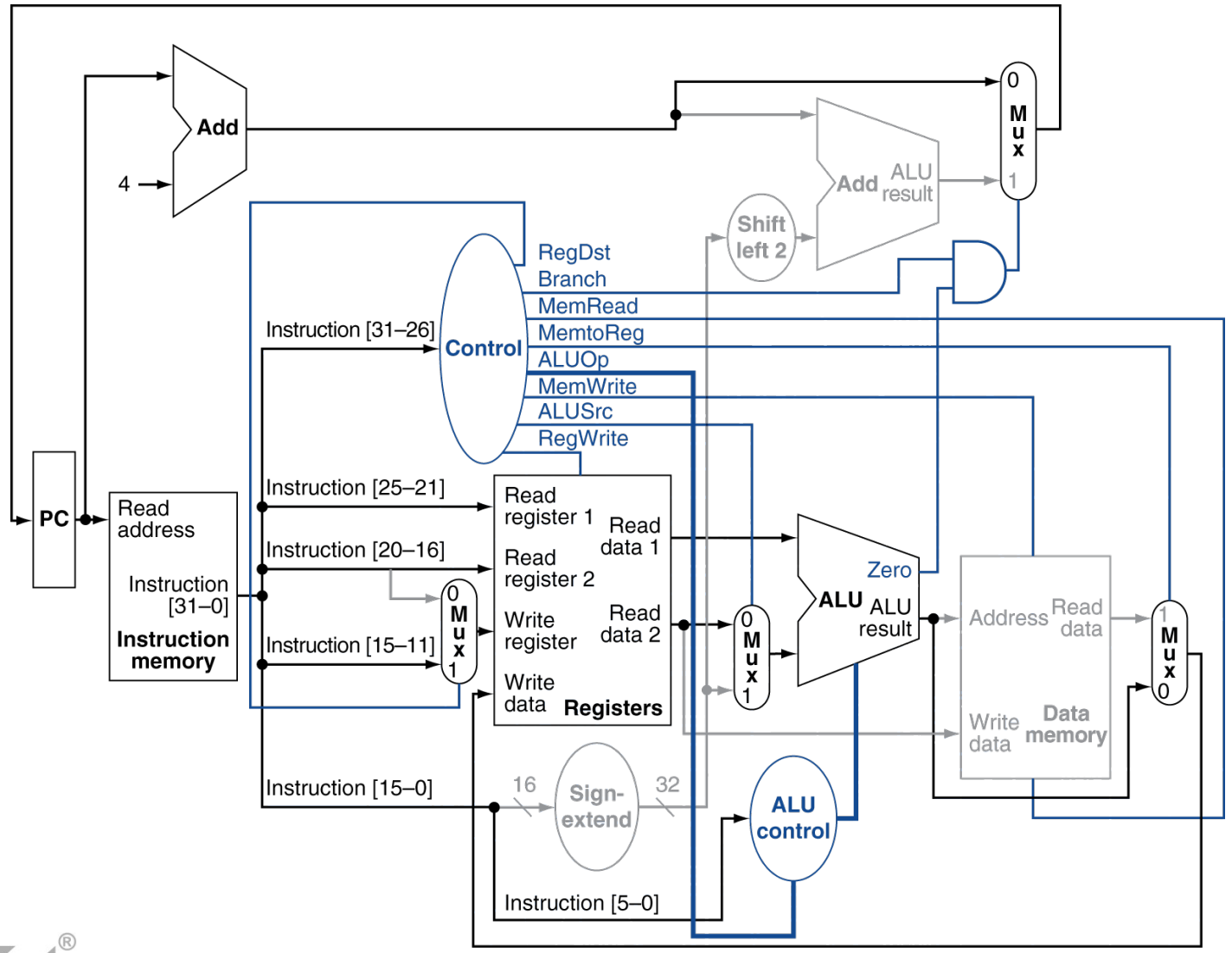
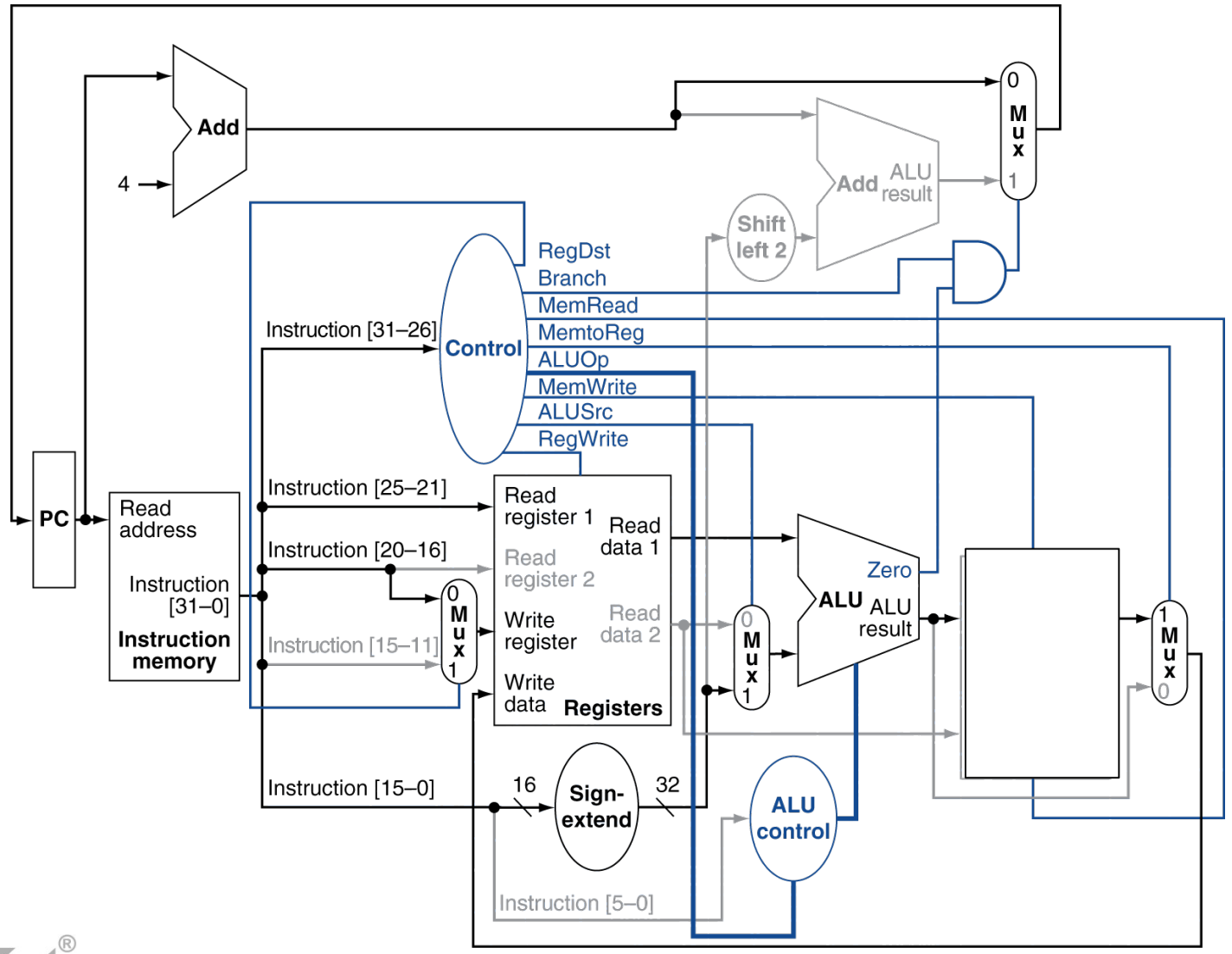
Chapter 4

The Processor

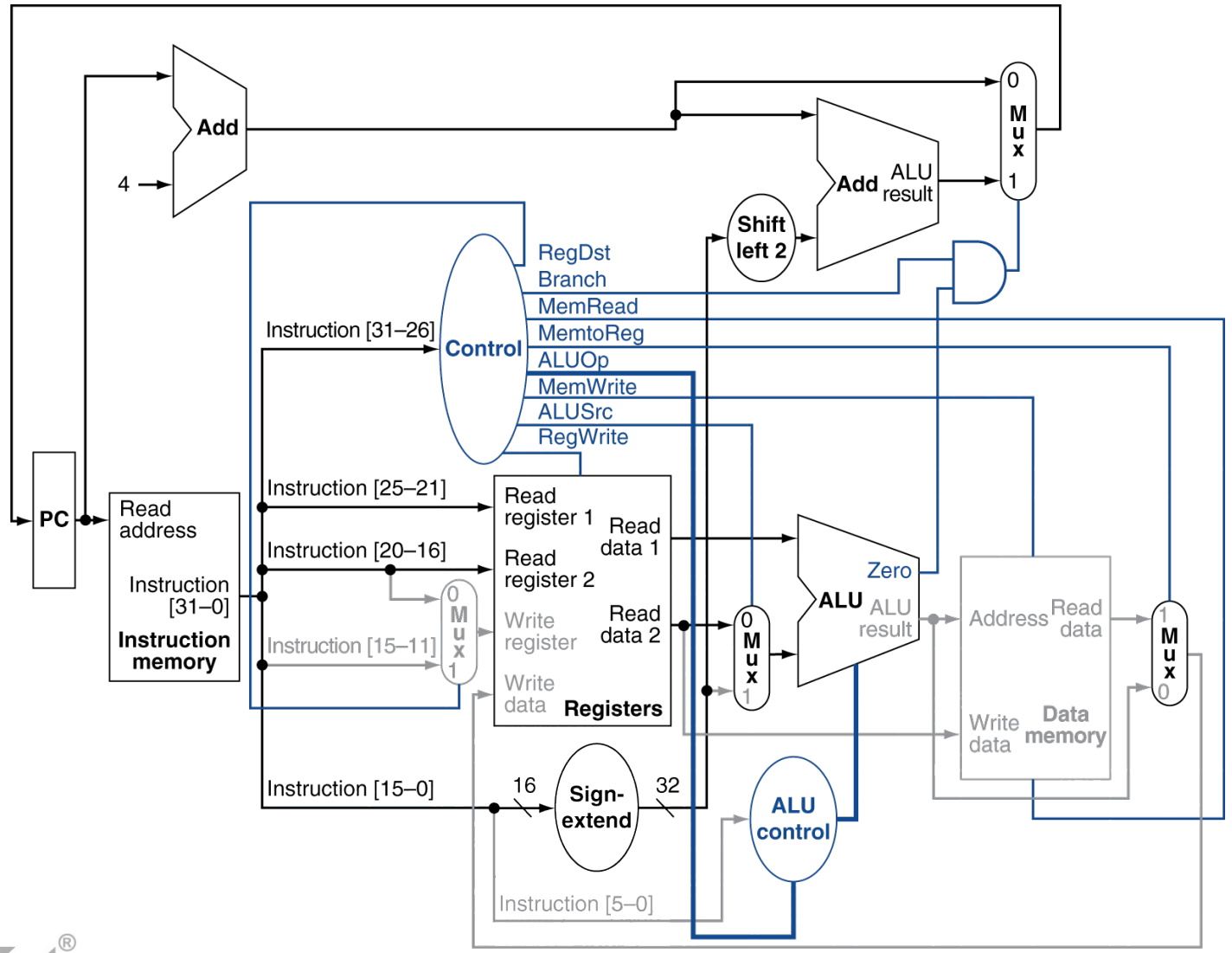
R-Type Instruction



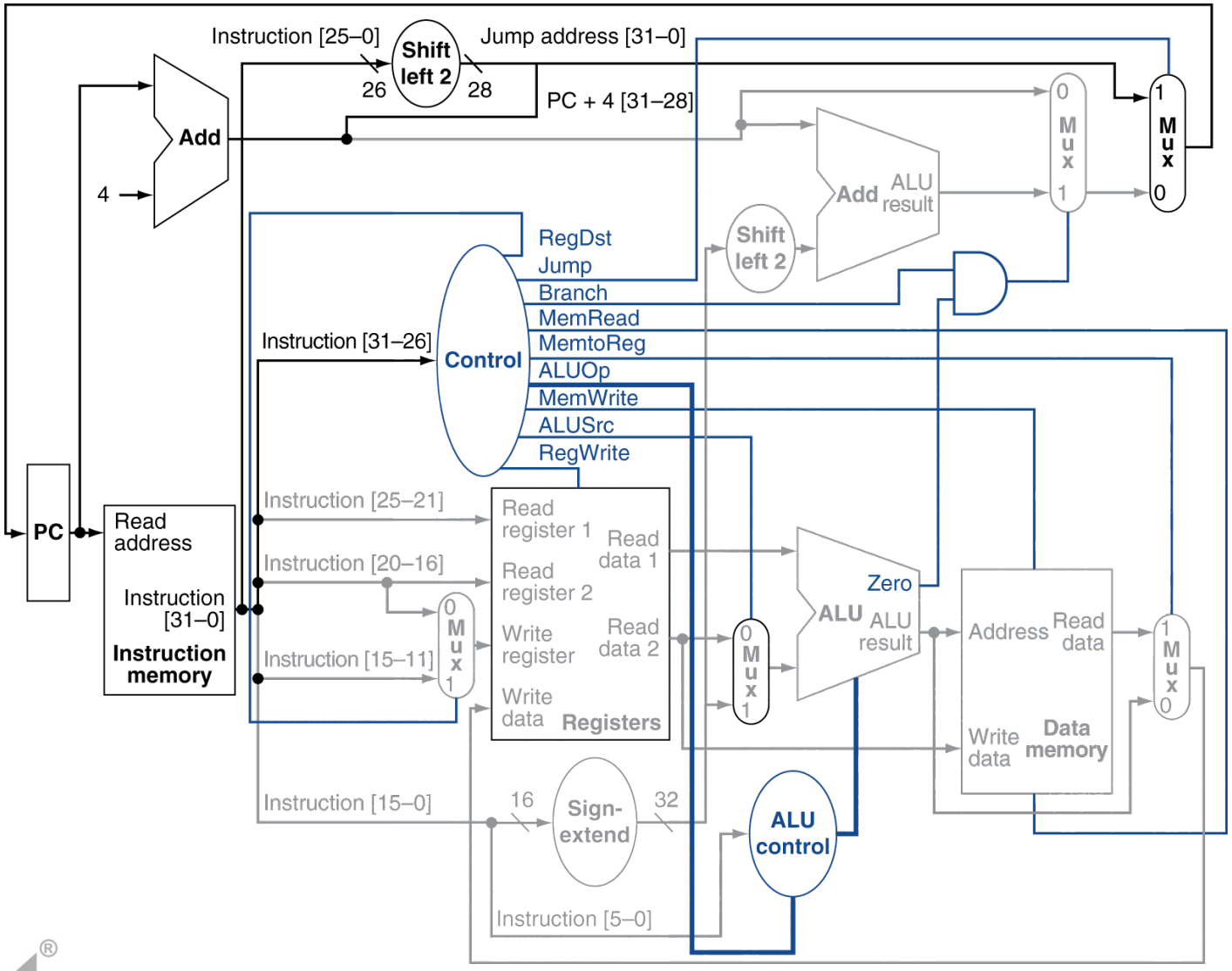
Load Instruction



Branch-on-Equal Instruction



Datapath With Jumps Added



Single Cycle Processor Implementation

Performance Issues

- The clock is determined by the longest possible path in the processor
  - Critical path: load instruction
  - Instruction memory → register file → ALU → data memory → register file
- Not feasible to vary period for different instructions
  - Clock cycle is the worst case delay for all instructions

Clock cycle time

- Assume time for stages is
  - 100ps for register read or write
  - 200ps for other stages

Instr	Instr fetch	Register read	ALU op	Memory access	Register write	Total time
lw	200ps	100 ps	200ps	200ps	100 ps	800ps
sw	200ps	100 ps	200ps	200ps		700ps
R-format	200ps	100 ps	200ps		100 ps	600ps
beq	200ps	100 ps	200ps			500ps