

# ASIC Design Laboratory

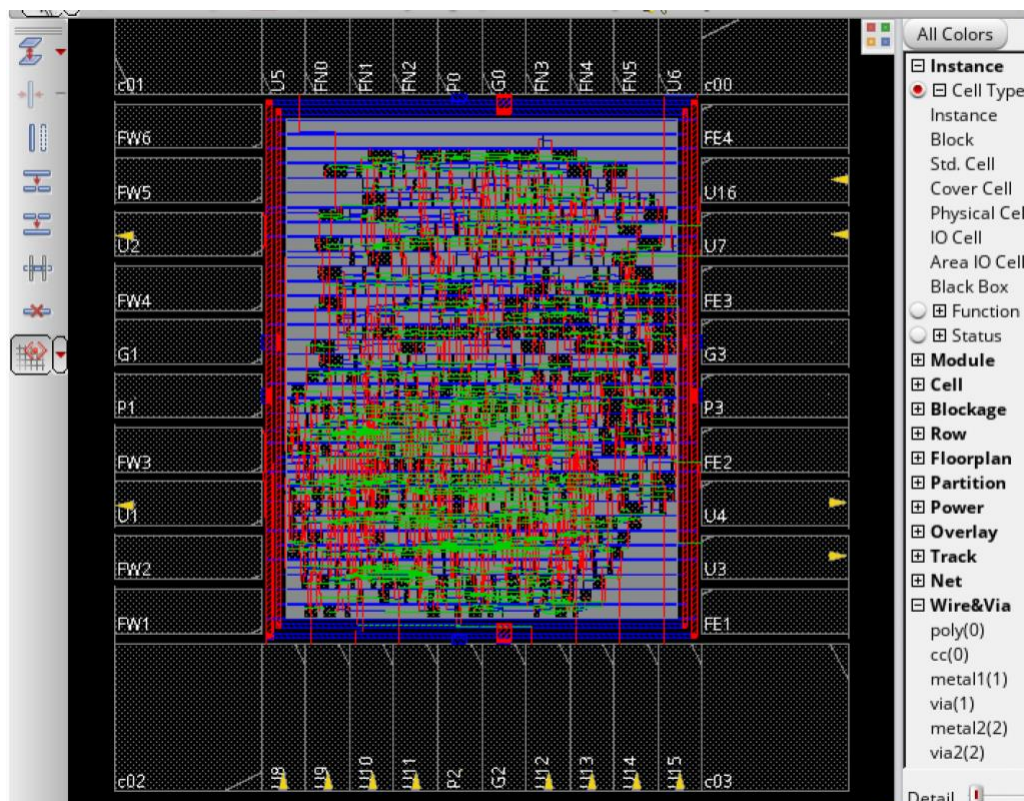
## Lab 10

### Evaluation Sheet

Spring 2020

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 Section: 1

Initial Full Layout	TA Initials	Date	Score
Error-Free Synthesis Run and Added Pads			____/0
Produced Layout			____/0
Connectivity Verified	_____	_____	____/6



What colors in the Innovus layout correspond to \_\_\_\_\_/2

METAL1? **Blue**

METAL2? **Red**

What are the coordinates of the Layout \_\_\_\_\_/2

Pad Frame Lower Left Corner X: **0** Y: **0**

Pad Frame Upper Right Corner X: **1500** Y: **1500**

What is the area of this layout of the design? \_\_\_\_\_/2

**2250000**

Altering the Aspect Ratio of the Layout

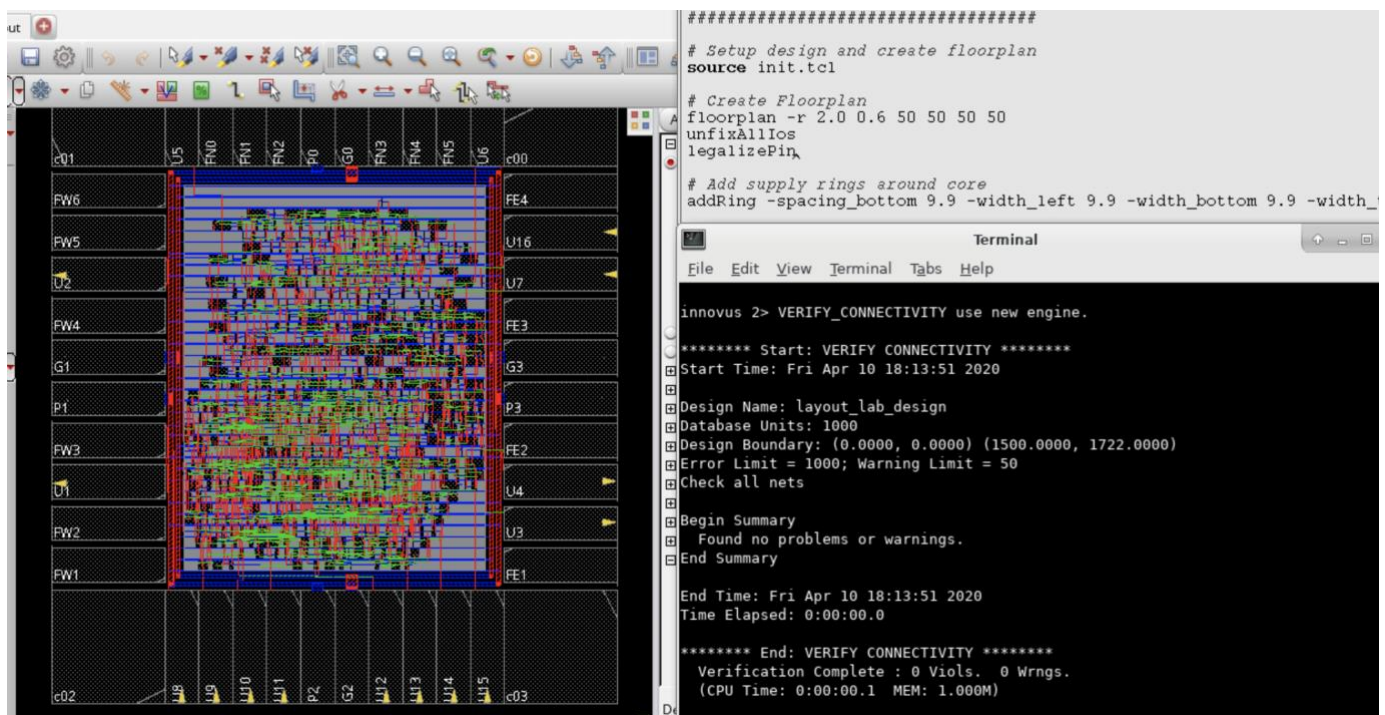
TA Initials

Date

Score

Produced Layout (Innovus only)

\_\_\_\_\_/3



The screenshot displays the Innovus layout tool interface. On the left, a hierarchical tree view shows the design structure with components like FW6, FW5, U2, FW4, G1, P1, FW3, U1, FW2, FW1, c02, U8, U9, U10, U11, P2, G2, U12, U13, U14, U15, c03, FE4, U16, U7, FE3, G3, P3, FE2, U4, U3, FE1, and U6. The main window shows a detailed layout of these components with various colored lines representing different metal layers. On the right, a terminal window shows the following text:

```
#####  
# Setup design and create floorplan  
source init.tcl  
  
# Create Floorplan  
floorplan -r 2.0 0.6 50 50 50 50  
unfixAllIos  
legalizePin  
  
# Add supply rings around core  
addRing -spacing_bottom 9.9 -width_left 9.9 -width_bottom 9.9 -width_  
  
Terminal  
File Edit View Terminal Tabs Help  
  
innovus 2> VERIFY_CONNECTIVITY use new engine.  
  
***** Start: VERIFY CONNECTIVITY *****  
Start Time: Fri Apr 10 18:13:51 2020  
Design Name: layout_lab_design  
Database Units: 1000  
Design Boundary: (0.0000, 0.0000) (1500.0000, 1722.0000)  
Error Limit = 1000; Warning Limit = 50  
Check all nets  
Begin Summary  
Found no problems or warnings.  
End Summary  
  
End Time: Fri Apr 10 18:13:51 2020  
Time Elapsed: 0:00:00.0  
  
***** End: VERIFY CONNECTIVITY *****  
Verification Complete : 0 Viols. 0 Wrngs.  
(CPU Time: 0:00:00.1 MEM: 1.000M)
```

What mathematical relationship can you derive for Aspect Ratio, and is used as more of a goal or requirement \_\_\_\_\_/2

**Goal.**

**the ratio of the width to height of the chip.**

**Height = aspect ratio \* width**

Altering the Row Utilization of the Layout

TA Initials

Date

Score

Produced Layout (Innovus only)

/3

```
# Create Floorplan
floorplan -r 1.0 0.4 100 50 100 50
unfixAllIos
legalizePin

# Add supply rings around core
addRing -spacing_bottom 9.9 -width_left 9.9 -width_
```

Terminal

File Edit View Terminal Tabs Help

innovus 2> VERIFY\_CONNECTIVITY use new engine.

\*\*\*\*\* Start: VERIFY CONNECTIVITY \*\*\*\*\*

Start Time: Fri Apr 10 17:55:30 2020

Design Name: layout\_lab\_design

Database Units: 1000

Design Boundary: (0.0000, 0.0000) (1713.6000, 1572.0000)

Error Limit = 1000; Warning Limit = 50

Check all nets

Begin Summary

Found no problems or warnings.

End Summary

End Time: Fri Apr 10 17:55:30 2020

Time Elapsed: 0:00:00.0

\*\*\*\*\* End: VERIFY CONNECTIVITY \*\*\*\*\*

Verification Complete : 0 Viols. 0 Wrngs.

(CPU Time: 0:00:00.0 MEM: 0.000M)

What are the coordinates of the Layout

/2

Pad Frame Lower Left Corner X: 0 Y: 0Pad Frame Upper Right Corner X: 1713.6 Y: 1572

What is the area of this layout of the design

/1

2693779.2

/2

How does this new area compare with the area that was previously calculated in the initial layout, and does this make sense given the two values for Row Utilization?

The area is greater. It does make sense because after changing the row utilization, each unit takes more space.

Why or why not is it possible to generate a layout for the USB that has 100% Row Utilization, not just a design goal of 100%?

/2

It's impossible to generate a layout for the USB that has 100% Row Utilization since if so, the interconnect in it would be too complicated in three metal layers.

Last Steps

TA Initials

Date

Score

Metal fill added with no max density violations

/2

```
79 addMetalFill -layer "1 2 3"

PROBLEMS OUTPUT DEBUG CONSOLE TERMINAL 1: verilog

innovus 2> setMetalFill -layer metal1 -windowSize 100.000 100.000 -windowStep 50.000 50.000 -minDensity 20.000 -maxDensity 80.000
setMetalFill -layer metal2 -windowSize 100.000 100.000 -windowStep 50.000 50.000 -minDensity 20.000 -maxDensity 80.000
setMetalFill -layer metal3 -windowSize 100.000 100.000 -windowStep 50.000 50.000 -minDensity 20.000 -maxDensity 80.000

***** Start: VERIFY DENSITY *****
Density calculation ..... Slot : 1 of 4
Density calculation ..... Slot : 2 of 4
Density calculation ..... Slot : 3 of 4
Density calculation ..... Slot : 4 of 4

No density violations were found.

***** End: VERIFY DENSITY *****
VMD: elapsed time: 1.00
(CPU Time: 0:00:00.1 MEM: 1.000M)
```

Why do you think that companies do not employ a fully  
Standard Cell, Place and Route approach to their  
high-performance microprocessor designs

\_\_\_\_/2

Unlike Fully custom design, fully Standard Cell  
cannot reach high performance

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Total points for lab

\_\_\_\_/30