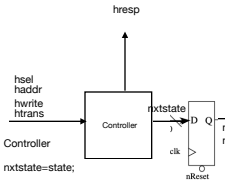



Controller

nxtstate=state;

IDLE:
if (hwrite&hsel)
    nxtstate = W
else if (!hwrite&hsel)
    nxtstate = R
else if (hsel & ((haddr==(0 | 1 | 2 | 3 | 15) & hwrite) | (haddr==(15) & !hwrite))
    hresp = 1;

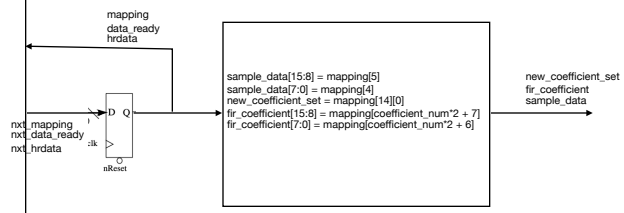
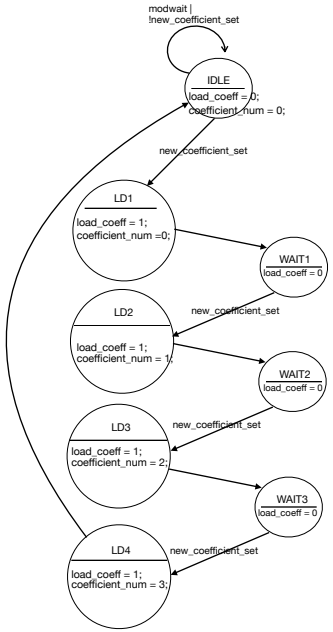
W:
if (!hwrite&hsel)
    nxtstate = R
else if (hsel & ((haddr==(0 | 1 | 2 | 3 | 15) & hwrite) | (haddr==(15) & !hwrite))
    hresp = 1;
else if (!hsel)
    nxtstate = IDLE

R:
if (hwrite&hsel)
    nxtstate = W
else if (hsel & ((haddr==(0 | 1 | 2 | 3 | 15) & hwrite) | (haddr==(15) & !hwrite))
    hresp = 1;
else if (!hsel)
    nxtstate = IDLE

OUT_LOGIC
default all value!!!!!
nxt_hsize = 0
nxt_haddr = 0
nxt_data_ready = 0
nxt_mapping = mapping
nxt_mapping[3] = fir_out[15:8]
nxt_mapping[2] = fir_out[7:0]
nxt_mapping[0][0] = modwait
nxt_mapping[0][7] = err

IDLE:
    nxt_mapping = 8'b0

W:
    if (nxt_haddr ==4 | 5)
        nxt_data_ready = 1;
    if (nxt_hsize==0)
        if (nxt_haddr % 2 == 0)
            nxt_mapping[nxt_haddr] = hwdata[7:0]
        else if (nxt_haddr % 2 == 1)
            nxt_mapping[nxt_haddr] = hwdata[15:8]

    else if (nxt_hsize == 1)
        if (nxt_haddr == 14 | 15)
            nxt_mapping[14] = hwdata[7:0]
        else if (nxt_haddr %2 == 0)
            nxt_mapping[nxt_haddr +1] = hwdata[15:8]
            nxt_mapping[nxt_haddr] = hwdata[7:0]
        else if (nxt_haddr %2 == 1)
            nxt_mapping[nxt_haddr] = hwdata[15:8]

R:
    if nxt_hsize==0
        if (nxt_haddr % 2 == 0)
            hrdata = {8'b0, mapping[nxt_haddr]}
        else if (nxt_haddr % 2 == 1)
            hrdata = {mapping[nxt_haddr], 8'b0}
    else if nxt_hsize==1
        if (nxt_haddr == 14 | 15)
            hrdata = {8'b0, mapping[14]}
        else if (nxt_haddr %2 == 0)
            hrdata = {mapping[nxt_haddr +1], mapping[nxt_haddr]}
        else if (nxt_haddr %2 == 1)
            hrdata = {mapping[nxt_haddr ], mapping[nxt_haddr-1]}