ASIC Design Laboratory
Lab 11
Evaluation Sheet

Spring 2020

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Section: 1

Lab Setup	TA Initials	Date	Score
Lab 11 folder and provided files in Git			/1

Layout Process Analysis	TA Initials	Date	Score
What layers are used for supply ring bars			/1

Horizontal? √ Vertical? _____

What are the widths of the supply ring bars and their spacing: /1

Bar Width? 9.9 Bar Spacing? 9.9

What is the spacing between the inner supply ring and the core area, and which prior command controls this /1

"addRing" command in "supply_rings.tcl"

How did the design change after running 'place_cells.tcl' /1

The cells were added to the core

What is a rough estimate for the core utilization /1

50.91%

What changed after running 'sroute' /1

The blue lines are connected to every row

In what ways are the three metal layers typically used in the routing /1

All the metal3 and metal1 are horizontal, and most of the metal2 are vertical. Metal1 connect with metal2 in the left and right side, and metal3 only connect to metal2.

What percentage of the core appears to be filled with cells after running 'final_route.tcl' /1

100%

And which command do you think primarily resulted in the change /1

"globalDetailRoute"

Performing Layout Timing Analysis TA Initials Date Score

What are the starting and ending gate-level components of the critical path /1

PADINC DFFPOSX1

How many combinational logic cells are in between /1

7

What are the starting and ending blocks (design modules) of the critical path /1

DFFSR DFFPOSX1

Is the synthesis critical path similar to the layout one? What are their respective delays /1

synthesis: 0.18

layout: -1.257

Pad/Pin Placement based Timing Adjustment TA Initials Date Score

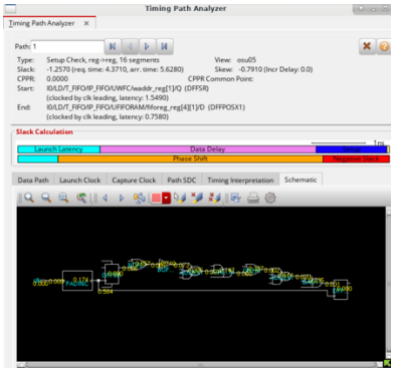
Reduced negative slack after IO-frame adjustment _____ _____ /4

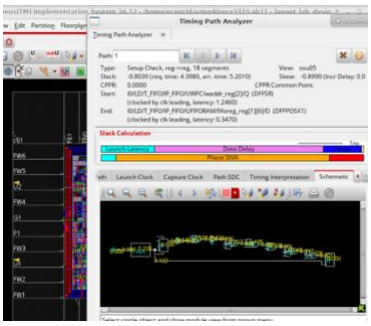
layout: -0.803

What change(s) were made and why do you think they resulted in the reduction /2

I switched the position of pad U5 and pad FE.

Because when I looked the path in the graph, I found that the wires are all connected to upper left corner, U5, which is too far way. Thus, I moved U5 to lower right corner. This change successfully reduced the delay since it reduced the path between where the pads been used and where the pads get their inputs.





Total points for lab /2