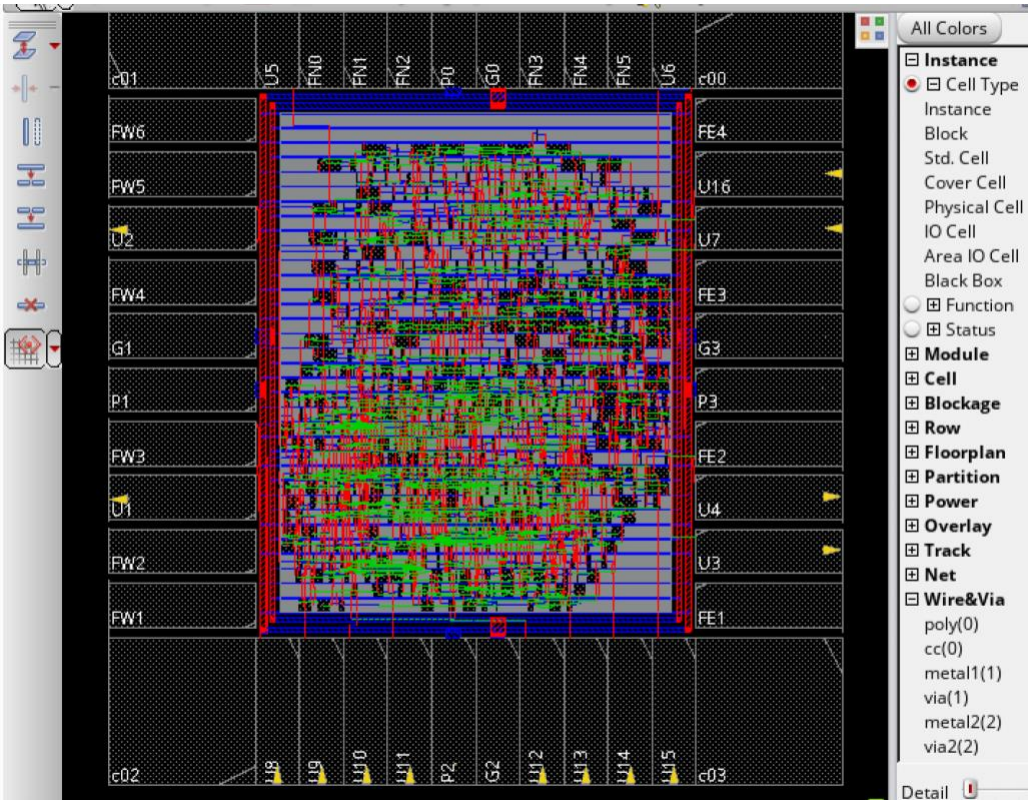
# ASIC Design Laboratory
# Lab 10
# Evaluation Sheet

Spring 2020

Student Name: Xiangyu Zhang
Mg Account: mg40
Section: 1

| | TA Initials | Date | Score |
|---|---|---|---|
| Initial Full Layout | | | |
| Error-Free Synthesis Run and Added Pads | | | /0 |
| Produced Layout | | | /0 |
| Connectivity Verified | | | /6 |



What colors in the Innovus layout correspond to /2

METAL1? Blue

METAL2? Red

What are the coordinates of the Layout /2

Pad Frame Lower Left Corner X: 0 Y: 0

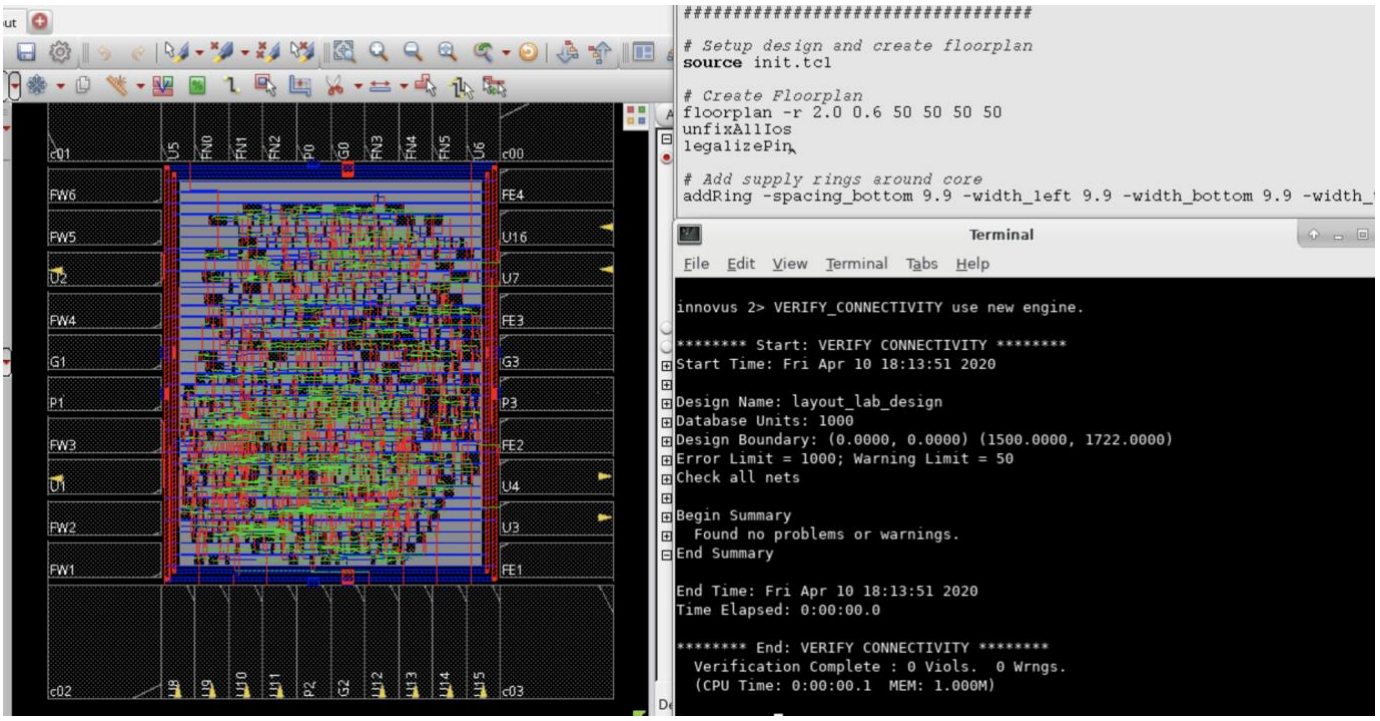
Pad Frame Upper Right Corner X: 1500 Y: 1500

What is the area of this layout of the design? /2

2250000

Altering the Aspect Ratio of the Layout TA Initials Date Score

Produced Layout (Innovus only) /3

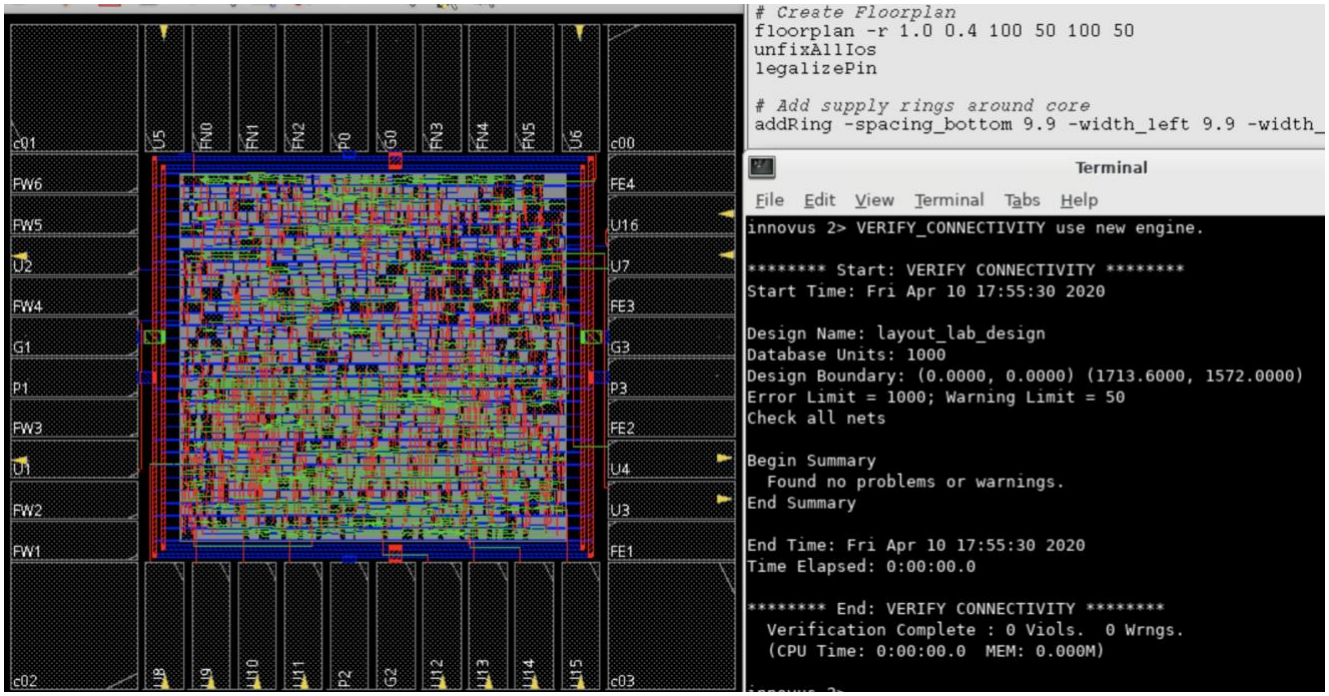



What mathematical relationship can you derive for Aspect Ratio, and is used as more of a goal or requirement /2

Goal.
the ratio of the width to height of the chip.
Height = aspect ratio * width

Altering the Row Utilization of the Layout TA Initials Date Score

Produced Layout (Innovus only) _____ _____ ____/3




What are the coordinates of the Layout ____/2

Pad Frame Lower Left Corner X: 0 Y: 0

Pad Frame Upper Right Corner X: 1713.6 Y: 1572

What is the area of this layout of the design ____/1

2693779.2

____/2

How does this new area compare with the area that was previously calculated in the initial layout, and does this make sense given the two values for Row Utilization?

The area is greater. It does make sense because after changing the row utilization, each unit takes more space.

Why or why not is it possible to generate a layout for the USB that has 100% Row Utilization, not just a design goal of 100%? ____/2

It's impossible to generate a layout for the USB that has 100% Row Utilization since if so, the interconnect in it would be too complicated in three metal layers.

Last Steps TA Initials Date Score

Metal fill added with no max density violations _____ _____ ____/2

```
79    addMetalFill -layer "1 2 3"
```

PROBLEMS OUTPUT DEBUG CONSOLE TERMINAL 1: verilog

```
innovus 2> setMetalFill -layer metal1 -windowSize 100.000 100.000 -windowStep 50.000 50.000 -minDensity 20.000 -maxDensity 80.000
setMetalFill -layer metal2 -windowSize 100.000 100.000 -windowStep 50.000 50.000 -minDensity 20.000 -maxDensity 80.000
setMetalFill -layer metal3 -windowSize 100.000 100.000 -windowStep 50.000 50.000 -minDensity 20.000 -maxDensity 80.000

******** Start: VERIFY DENSITY ********
Density calculation ...... Slot :   1 of   4
Density calculation ...... Slot :   2 of   4
Density calculation ...... Slot :   3 of   4
Density calculation ...... Slot :   4 of   4

No density violations were found.

******** End: VERIFY DENSITY ********
VMD: elapsed time: 1.00
     (CPU Time: 0:00:00.1  MEM: 1.000M)
```

Why do you think that companies do not employ a fully Standard Cell, Place and Route approach to their high-performance microprocessor designs _____/2

Unlike Fully custom design, fully Standard Cell cannot reach high performance

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Total points for lab _____/30