Engineering the Hardware/Software Interface for Robotic Platforms - A Comparison of Applied Model Checking with Prolog and Alloy

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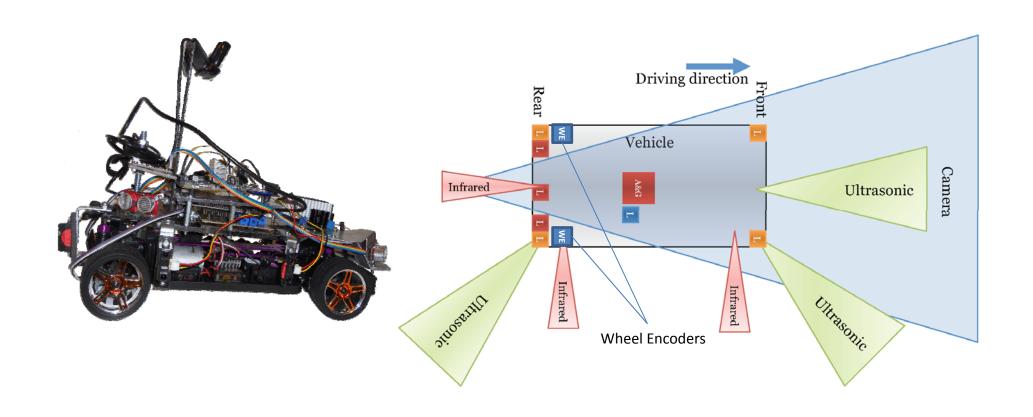
Division of Software Engineering
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Outline

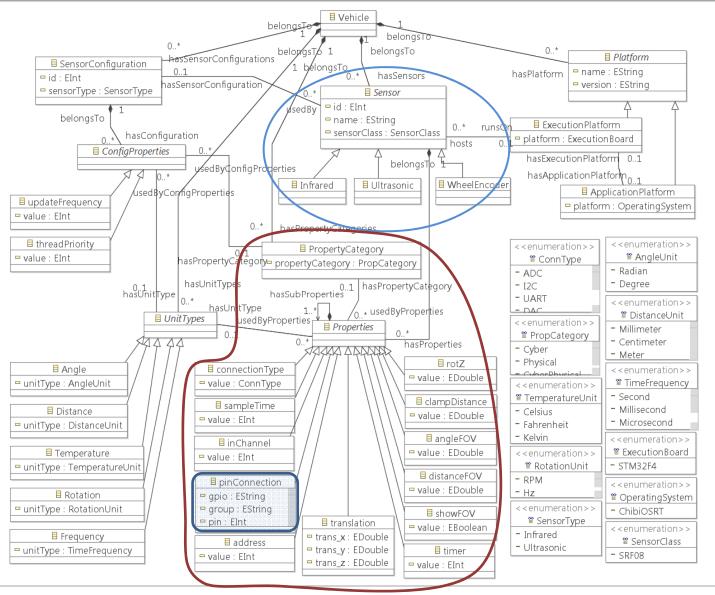
- Problem Domain
- Research Questions
- Overall Workflow
- Prolog Approach
- Alloy Approach
- Result
- Other Observations
- Future Work
- Summary & Conclusion

Problem Domain: Sensor Layout

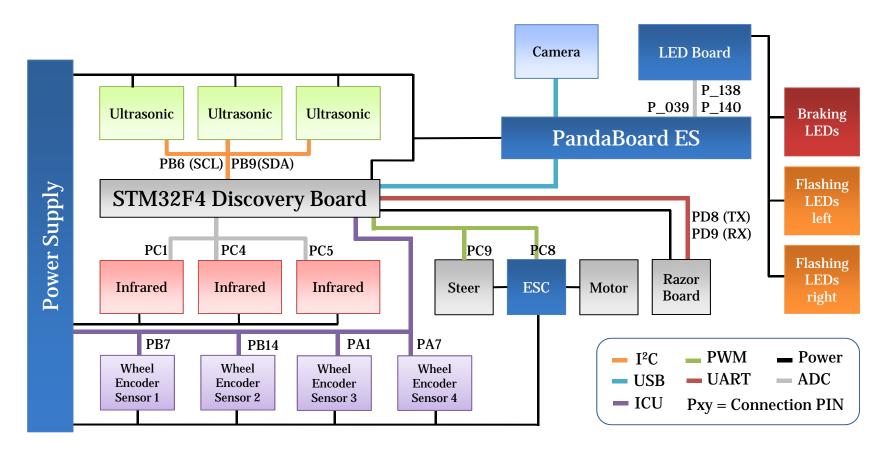


Problem Domain: DSL Meta-Model

- EMF ECORE Model
- Sensors
- SensorProperties
- ConfigurationProperties
- ExecutionPlatform
- ApplicationPlatform
- Unit Types
- Enumerations



Problem Domain: Solution for a Desired Configuration

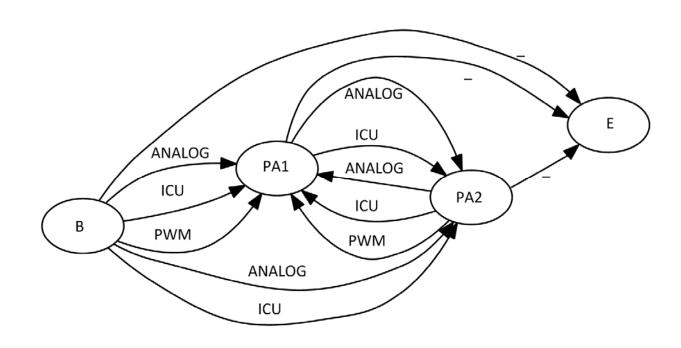


Schematic Hardware Architecture with assigned pinConnection

Problem Domain: Configuration Space

n	ADC1	I2C1	I2C2	12C3	UART1	UART2	UART3	UART4	UART5	UART6	CAN	ICU1	PWM1	ICU2	PWM2		PWM3	ICU4	PWM4	ICU5	PWM5	PWM6	ICU9	ICU10	ICU1
	ADC1-IN2					UART2-TX									TIM2_CH		1				TIM5_CH3		TIM9_CH		
_	ADC1-IN3					UART2-RX									TIM2_CH	4					TIM5_CH4		TIM9_CH2	-	
	ADC1-IN1													TIM2_CH2	2					TIM5_CH2					
88											CAN1-RX								TIM4_CH3					TIM10_CH1	1
11			I2C2-SDA				UART3-RX								TIM2_CH	4									
:6										UART6-TX	<						TIM3_CH					TIM8_CH3			
:9				I2C3-SDA													TIM3_CH	4				TIM8_CH4			
18				12C3-SCL								TIM1_CH	1												
30	ADC1-IN8																TIM3_CH	3							
31 .	ADC1-IN9																TIM3_CH	4							
36		12C1-SCL			UART1-TX																				
37					UART1-RX													TIM4 CH2	2						
39		I2C1-SDA									CAN1-TX							 							
10			12C2-SCL				UART3-TX																		
10								UART4-TX																	
:11								UART4-RX																	
	ADC1-IN4		200	Page Lagren	LIKER CHAR	22 9090122	UNI NO	DALLI 4-ITA	DCI ADCI	Do DMC Do	N31	NVI.	De DEI	DC2 DC1	Do MAIL	UANTZ PROFES	DAVIS	DATE DATE	Do 800	On DOM	Pos LCO	Touch I'els ISSE	2 NOCAMO	Cerere bitternel	CAN
	ADC1-IN4 ADC1-IN5		PAI	0 Button				PAG ADDINO AD	SHIND ADCSHIND	PAG PAG PAG PAG PAG	500		PA0 PA1		PAG PA1		UART+TX UART+RX		Pa	PAD PA1	PAI LCD		-		
			PAC PAC	Per SAGREEN				PAG AGC1 AGC1465 AGC	DINESOA DINES	PAZ PAZ PAZ PAZ			Phis EXC1 PAC PA		PM UARTT PA2 PA2 PA3 PA4 PA4	UARTS-TX UARTS-RX			PM 5300 F PA0 F PA1 F PA2 F PA3 F PA4 F	1A2 1A3	PA2 PA3 PA4	Pail		ETHRISOLK ETHNOID	Second Se
	ADC1-IN6		PA:		1253-F 5911-CUK	15		PAS ADDITION AD	200	PAS DACI PAS	\$91-500 \$91-450 \$91-400		PAS PAS		PAS PAS PAS				PAS P	NA DOVIJHSYNC	PAS PAS			HSYNC	
	ADC1-IN7		PA:		SPINISO SPINIOS			PAT ADDING AD	24NF	PAS PAS	SPI-MISO SPI-MIOSI		PAT		PAT				PAT P	TAT .	PAT			POJK STHING	
9			PAI	Fee .			abveus .	PAS PAS		PAS PAS			PAS PAS	1203-50.	PAT PAS UARTI-TX PA10 UARTI-RX PA11			\rightarrow	PAS P	NAS DOVI_DD	PAS PAS PA10 PA11				
.10			PAT	11			10 OH OP	PA11 PA12		PA10 PA10 PA11 PA11 PA12 PA12		_	PA11		PA11				PA11 P	A10 00VI_D1	PA11 PA12				
15			PAT	13			SWOO	PA13		PA13 PA13 PA14 PA14		_	PAT PAS PAS PAID PAID PAID PAID PAID PAID PAID PAID		PA12 PA13 PA14			-	PAT P PAS C	A13	PA13 PA14				_
34			PA1	IS Free				PA15		DAIS DAIS		_	PA15		PAIS					H15	PA15	DigSel.			_
35			Pa	Free				P80 ADC14NS AD 981 ADC14NS AD	3/16 3/16	Page			PEC PE1		Pac				P20 P	Page 1	PEO Zeckight PEI	0007			_
14			PE:	2 Free			SNO	PB2 PB2		P82 P82 P83 P83	SPIT-SOC SPIT-MSO SPIT-MOSI	SPI3-SOX	P82		PR2 PR3				P82 P	182	PB2 PB3				
15			PE-	fra Fra	12014			PEA PES PES		PEA PEA	SPIT-MOSI	SPISHOSI	PEA PES		PD4 PD5 PDF UADTATX				PEA P	184	PEA PES PER	DIN DIN		Di	
:0	ADC1-IN10		Par Par		1201-5	10.		PRF		P26 P26 P27 P27 P25 P25			PACS PA		PES UARTITY PET UARTITY PES				PRT P	705 00W_D8 00W_D	PET PES			VSYNC SCL	
	ADC1-IN11		PE		1201-5	DA .		PES		PES PES PES PES	\$92.50		PES ISCHSON	G-50.	PES PESO	UARTS T			PES SCIOLOS P	es conjus	PES PESO			SOA	GANI-TX
	ADC1-IN12		PG*	II free			-	9810 P811 P812 P813 P815 P815 P815 P815 P815 P815 P816 P8		Per			PB11 12	CD-SOA	PB12 PB12 PB13	UARTSR		\rightarrow	PRY PRS SCIC_DA P PRS SCIC_DA P PRS SCIC_DO P PRSI SCIC_DO P PRII P P P P P P P P P P P P P P P P P P P	911 912	PB11 PB12			ETHM ETHM	
	ADC1-IN13		PS1	Tree				PB13		PB11	\$P3-90 \$P3-00	K .	PB13		PB13				PB13 P	011 012 013 014	P013			ETHN	
	ADC1-IN14		PET	Tree				Pars Dec		P015 P015	\$9540	,	PRIS Dis		P214 P215			-	PEIS P	215	P214 P215 Pin	PEN			_
			PC PC	t Free			PowerCn	Pina	3-IN10 ADCS-IN10 3-IN11 ADCS-IN11	P00 P00 P01 P01			PCO		PCI PCI				PC1 P	No.	PCD PCD		50-Detect	ETHNOC	_
	ADC1-IN15		PC PC	2 Fee		DOUT		PEZ ADCI-INIZ ADC PEZ ADCI-INIZ ADC	2-IN12 ADC3-IN12 3-IN13 ADC3-IN13	PC2 PC3	\$P(2-01) \$P(3-02)	9	PC2 PC3 PC3 PC4		PCI PCI PCI PCI				PC2 PC3 PC4	C2	PC2 PC3	BUSY			
7			PO PO	Free				PES ADDITION ADD PES ADDITION ADD PES	3-IN15	PC4 PC4 PC5 PC5 PC5 PC5			PCS PCS		PCS PCS			_	PCS P	104	PCS PCS			ETH no.	_
12			PO PO	E Free	1000								POS Mur					UARTSTX UARTSHA	POS SOIO_OS P	00 00VI_00	PCS PU/			D0	
)2			PO		1253-5	DK .	\rightarrow	PCS PCS PC10	\rightarrow	PCS PCS PCS PCS PC10 PC10		SPISSON	PCS PCS PCS PC10 PC10 PC11 PC11	1203-50A	PCS PCS PC10	UARTST	E UARTATX		PCS SDC_CS P	00/1_02 00/1_02	PCS PCS PCS		\$0,0_00 \$0,0_01 TX \$0,0_02	00	+
)5			PC1	Free	12534			PC11		PCII PCII		SPIS-MISO SPIS-MOSI	PC11	_	PC11		C LINETA DV	TSTX	PC11 5010_03 P	C11	PCII PCI2	R5223-	RX 50/0_03 50/0_0X		+
96			PCI PCI PCI					PC13 PC14 PC15		PC13 PC13 PC14 PC14			PC13 PC14 PC15		PCIS PCIS PCIS PCIS PCIS					C13 C14 C15	PC14				
8			PCI	S Frai				Pos Pos Pos		PCIS PCIS The The FOO FOO			Pois De		Pois Dis				Po I	no no	PCIS Pins POD FSMC_D2				
9			Po Po Po	t Frei				PDI		P01 P01			Pol 902 903		P01				#00 # P01 P #02 \$00_010 # P02 P	100	P00 F5WC_00 P01 F5WC_00				
5			PO:	Free	Rem			POZ POS		P01 P01 P02 P02 P03 P03			P01		P01 P02 P03			rsax	P02 500_0/0 P	103	POS PSHC_NOS		\$010_010		
6			PO		See		ED OVCUM	POA POS		POA POA POS POS POS POS POT POT			POS		POS POS POT	UARTSTX UARTSRX			POA POS	104 105 106 107	POS FSUC_NIVE				
9			FO 90	E Fra			-	POS POS	_	POS POX		-	POS POS		POF	UARTST:		-	P05 0	101	PDF F5WC_NE1 PDF F5WC_D13				
11			POI	5 Frei 10 Frei 11 Frei		_	-	PO10	_	P06 P08 P09 P09 P010 P010		_	POID POID		POID POID	UARTER		$\overline{}$	P010 P	108 010	POS FSVC_DIA		-		-
13			PO!	11 Frei 12 LEO green				P011		PO11 PO11 PO12 PO12			P011 P012		P011 P012				P011 P	011 00VI_04 012	P011 P012				
14			P01	12 LEO green 13 LEO mange 14 LEO med				P06 P09 P010 P011 P011 P011 P011 P012 P013 P014		POS			P013 P014		908 909 9010 9011 9012 9012 9014				P013 P	005 005 001 001 001 001 002 003	PD13 PSMC_00				
14			POT	S LEO bue				Pois Pin		POIS POIS			PDIS The						POIS P		POIS FSVC_DI				
			PS:	1	N(T1 N(T2		_	PE0 PE1		Pos PG0 PG1 PG1			PE1		Pin PE1				PE1 P	150 00VI_02	PE1				
			PE	2 Free	Olese			PEZ PEZ		962 962 963 963 964 964 966 966 967 967			PE2 PE3		PE2 PE3				PE2 P	162	PE2 FSVC_A19			-	
			PE-	4 Frei 5 Frei 6 Frei				PES DES		PE4 PE5			PES DES		PES DOS				PES P	924 00/1_04 925 00/1_06	PSA PSS			04 08 07	
			000 000 000 000 000 000 000 000 000 00	Total			-	924 925 927 927 928 929 9210 9211 9212				_	504 504		952 953 954 955 965 967 967 963 963 9610 9611		+		2000 P	NAME SCOTT DOWN_DD	PET FSWC_D4 PES FSWC_DS			J	+
			PE	7 Feet				PE9 PE10		PE9 PE9 PE10 PE10			PES PESO		PES PEIO				PE9 P	129 1210	PE9 F5VC_06 PE10 F5VC_07				
			PE	II Free			-	PE11		PES PES PETO		-	PE11		PE11		+	-	PE11 P	E11	PEH FSMC_08		_		+
			PE	13 Frei 14 Frei 15 Frei				PE13 PE14 PE15		PE13 PE13 PE14 PE15 PE15 PE15			PE12		PE13 PE14 PE15				PE13 P	E12	PE12 F5MC_010 PE13 F5MC_010 PE14 F5MC_011 PE15 F5MC_012				

Basic Representation Model



Visualization of the graph $G = \{N, E, A\}$

A concrete configuration is represented by a path P from n_B to n_E with |P| < |N|

Problem Domain: Complexity

$$C_{|M|=1}^{|N|} = \sum_{k=1}^{L} \binom{|N|}{k} = \sum_{k=1}^{L} \frac{|N|!}{(|N|-k)!k!}$$

$$K(n,m) = \begin{cases} 1 + \sum_{p=1}^{n} *K(p,m-1) & \text{if } m > 1, \\ 1 & \text{otherwise} \end{cases}$$

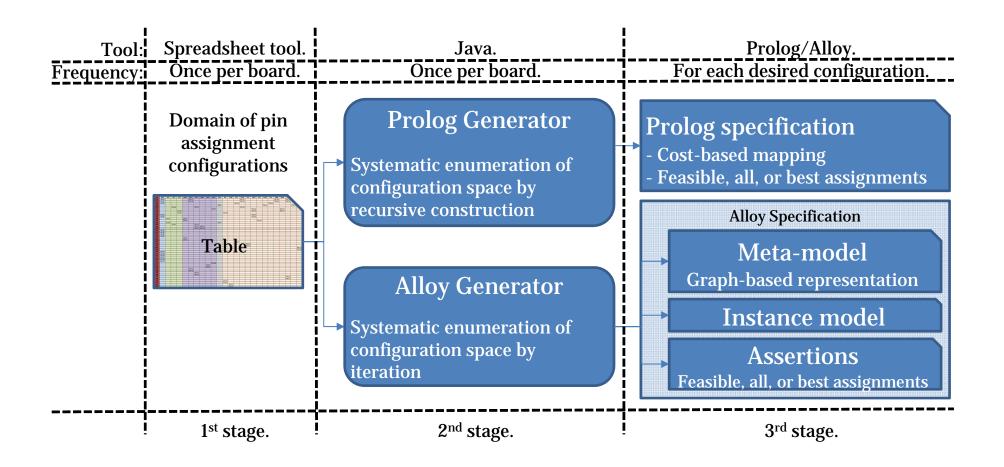
$$C_{|M|}^{|N|} = \sum_{k=1}^{L} \binom{|N|}{k} *K(k,|M|)$$

- ✓ Total 1,099,126,862,792 configuration possibilities (considering all pins)
- ✓ Total 14,689,111 configuration possibilities (considering pins with multiple usage)

Research Questions

- To determine a feasible, all possible, and the best configuration assignment:
 - How can Prolog be used to apply model checking on instances of the domain of possible pin assignment configurations?
 - How can Alloy be used to apply model checking on instances of the domain of possible pin assignment configurations?
- Which approach performs quicker compared to the other for the particular use cases?

Overall Workflow



Prolog Approach

- Consists of two parts
 - Facts (generated)

```
config([analog,analog],[[pa1,pa2],7])
```

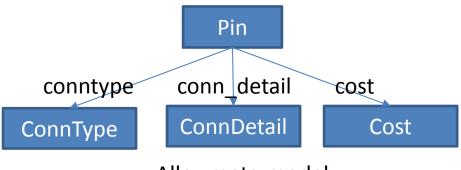


```
getConfig(RequiredConfiguration, Pair) :-
    msort(RequiredConfiguration, S),
    config(S, Pair).

allConfigs(RequiredConfiguration, Set) :-
    setof([Pins,Costs],
        getConfig(RequiredConfiguration,
        [Pins,Costs]), Set).

cheapestConfig(R, Pins, Costs) :-
    setof([Pins,Costs],
        getConfig(R, [Pins,Costs]), Set), Set = [_|_],
    minimal(Set, [Pins,Costs]).
```

Alloy Approach



Alloy meta-model

• Instance specification for a pin

```
one sig PA2 extends Pin {} {
conntype = ANALOG + SERIAL_TX + ICU + ICU
conn_detail = ADC1_IN2 + UART2_TX + TIM2_CH3 + TIM5_CH3
cost = 4}
```

Generated negated assertion for the desired configuration "ANALOG, ANALOG".

```
assert ANALOG_ANALOG {
all disj p1, p2:Pin |
not (
ANALOG in p1.conntype &&
ANALOG in p2.conntype &&
p1.cost.add[p2.cost] < = 3
)}
check ANALOG_ANALOG</pre>
```

Result

	Length	Costs for feasible assignment	Computation time for feasible configuration	Computation time for impossible configuration		
	1	3	0s	Os		
	2	7	0s	Os		
	3	11	0s	Os		
ρū	4	13	Os	0.01s		
Prolog	5	15	0.03s	0.02s		
Pr	6	17	0.11s	0.10s		
	7	19	0.29s	0.30s		
	8	21	0.78s	0.64s		
	9	23	1.06s	1.06s		
	10	26	2.47s	1.36s		
			$\emptyset = 0.474s$	$\emptyset = 0.349s$		
			± 0.79s	± 0.50s		

	Length	Number of all possible assignments	Costs for best assignment	Prolog computation time (all/best)		
	1	5	2	0s/0s		
	2	10	4	0s/0s		
	3	10	7	0s/0s		
6 0	4	24	9	0.01s/0.01s		
Prolog	5	11	13	0.06s/0.03s		
Pr	6	2	17	0.22s/0.11s		
	7	8	19	0.61s/0.30s		
	8	20	21	1.40s/0.64s		
	9	20	23	2.42s/1.08s		
	10	32	26	4.06s/1.38s		
				$\varnothing_{all} = 0.878s \pm 1.375s \\ \varnothing_{best} = 0.355s \pm 0.51s$		

	Length	Costs for the first feasible as- signment	Computation time for feasible configuration	Computation time for impossible configuration		
	1	3	0.53s	-		
	2	7	0.52s	0.52s		
>	3	11	0.56s	0.53s		
Alloy	4	13	0.54s	0.53s		
⋖	5	15	0.56s	0.53s		
	6	17	0.57s	0.64s		
	7	19	0.62s	0.62s		
	8	22	0.63s	0.56s		
	9	23	0.65s	0.67s		
	10	26	0.67s	0.68s		
			$\emptyset = 0.58s \pm 0.05s$	$\emptyset = 0.59s \pm 0.06s$		

	Length	Number of all possible assignments	Costs for best assignment	Alloy computation time (all/best)		
	1	5	2	0.07s/0.53s		
	2	20	4	0.24s/0.63s		
	3	60	7	0.59s/0.67s		
>	4	480	9	1.57s/1.63s		
Alloy	5	840	13	2.27s/1.20s		
⋖	6	720	17	2.16s/1.17s		
	7	2760	19	4.68s/1.09s		
	8	7320	21	10.43s/3.25s		
	9	7320	23	9.27s/2.88s		
	10	9960	26	14.12s/3.38s		
				$\varnothing_{all} = 4.58s \pm 5.02s$		
				\varnothing_{best} = 1.64s \pm 1.11s		

Other Observation

Generated specification size

Prolog	Alloy
1.7GB	100KB

Time to generate specification

Prolog	Alloy
2102s (~35min)	Less than 1s

Time to load specification

Prolog	Alloy
347s (~6min)	Less than 1s

Future Work

Optimization
Algorithm

VS. Model Checker
with Higher Order
Quantification

VS. Alloy/Prolog

- Extend the work with other available COTS interface boards (Odroid, Rapsberry, Arduino, etc.)
- How good are the tools wrt. longer configuration length and more pins?

Summary & Conclusion

- ✓ Prolog performs up to more than 3-times faster to find all possible and best solution
- ✓ Alloy performs up to more than 3-times faster to find feasible solution and reporting insolvable configurations
- ✓ Alloy does not directly support higher order quantification but workaround solution is possible
- ✓ With the considered total number of pins (16) and configuration length (10) both Prolog and Alloy offers practicable solution.

Thank You