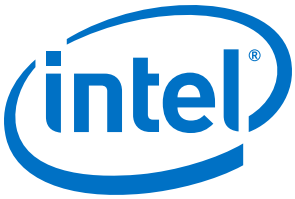


Quick-Start for Intel® Quartus® Prime Pro Edition Software

Updated for Intel® Quartus® Prime Design Suite: **17.1**


Subscribe


Send Feedback

MNL-1093 | 2018.10.22

Latest document on the web: **PDF** | **HTML**

Contents

MNL-1093 | 2018.10.22

Send Feedback

Quick-Start for Intel® Quartus® Prime Pro Edition Software

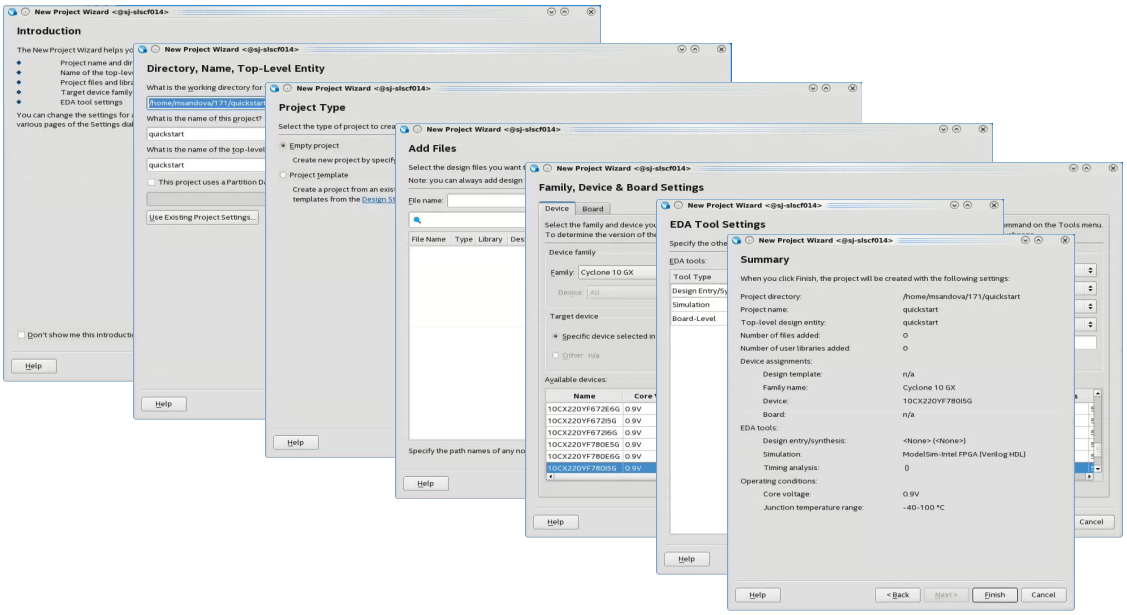
This document demonstrates how to set up an Intel® Quartus® Prime Pro Edition project, compile, perform a timing analysis, and program the generated files into an Intel FPGA device.

The following steps describe the flow:

Step 1: Create your Design

The Intel Quartus Prime software organizes and manages the elements of your design within a *project*. The project encapsulates information about your design hierarchy, libraries, constraints, and project settings. The **New Project Wizard** helps you to quickly setup and create a new design project.

Figure 1. New Project Wizard



To create a project with the **New Project Wizard**:

1. In the Intel Quartus Prime Pro Edition main window, click **File ➤ New Project Wizard**.
2. Specify project directory, name, and top-level entity.
3. Add design files and libraries.
4. Specify Intel FPGA device or Intel FPGA Development Kit/Board.
5. Specify Design Entry/Synthesis, simulation, and board-level tools.
   - For Intel Quartus Prime Synthesis, select **<None>**.
6. Review project settings and click **Finish**.

After the **New Project Wizard** generates the project, you can create design files using the full-featured schematic and text editors that the Intel Quartus Prime software provides. In addition, you can combine your logic design files with Intel and third-party IP core design files, including combining components into a Platform Designer system (`.qsys`).

Related Information

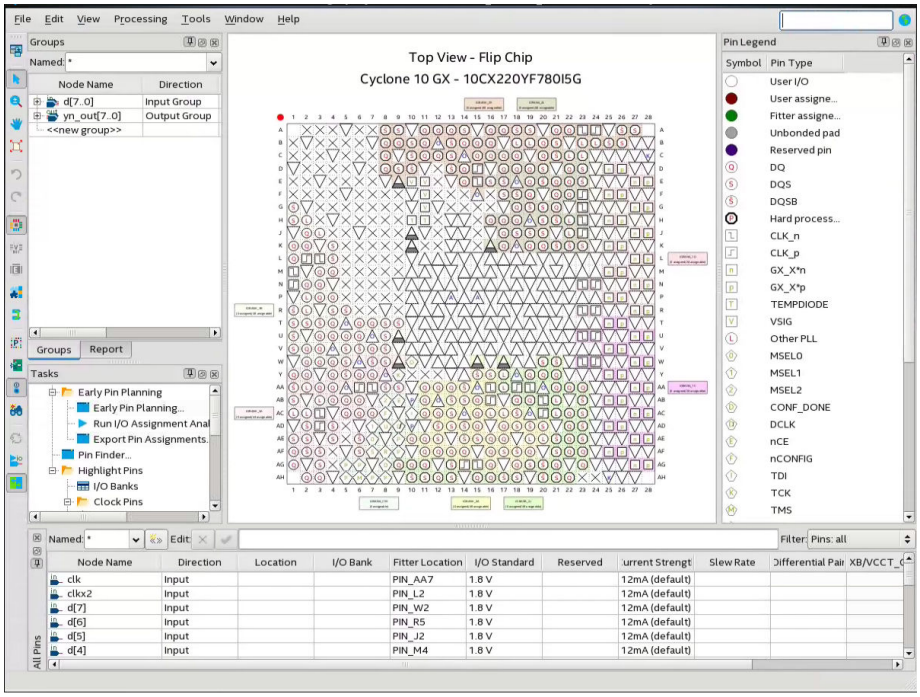
- Intel Quartus Prime Pro Edition User Guide: Getting Started
- Creating a New Project with Intel Quartus Prime

Step 2: Constrain your Design

After adding design files to the project, you assign design elements to I/O pins, and apply appropriate timing constraints to correctly optimize fitting and analyze timing for the design.

1. Click **Processing ➤ Start ➤ Start Analysis and Synthesis** to Run Analysis and Synthesis in the project
2. Click **Assignments ➤ Pin Planner**.

Figure 2. Pin Planner Window



3. In the **Pin Planner** window, specify pin location, I/O standard, current settings, and slew rate.
4. Create a timing constraints file by clicking **File ➤ New** and then clicking **Synopsys* Design Constraints File**.
5. Specify constraints for clock characteristics, timing exceptions, and external signal setup and hold times before running analysis.

In addition to device I/O pins and timing constraints, the Intel Quartus Prime Pro Edition software allows you to define placement and hierarchical constraints.

For more information, refer to the *Intel Quartus Prime Pro Edition User Guide: Design Constraints*.

Related Information

Intel Quartus Prime Pro Edition User Guide: Design Constraints

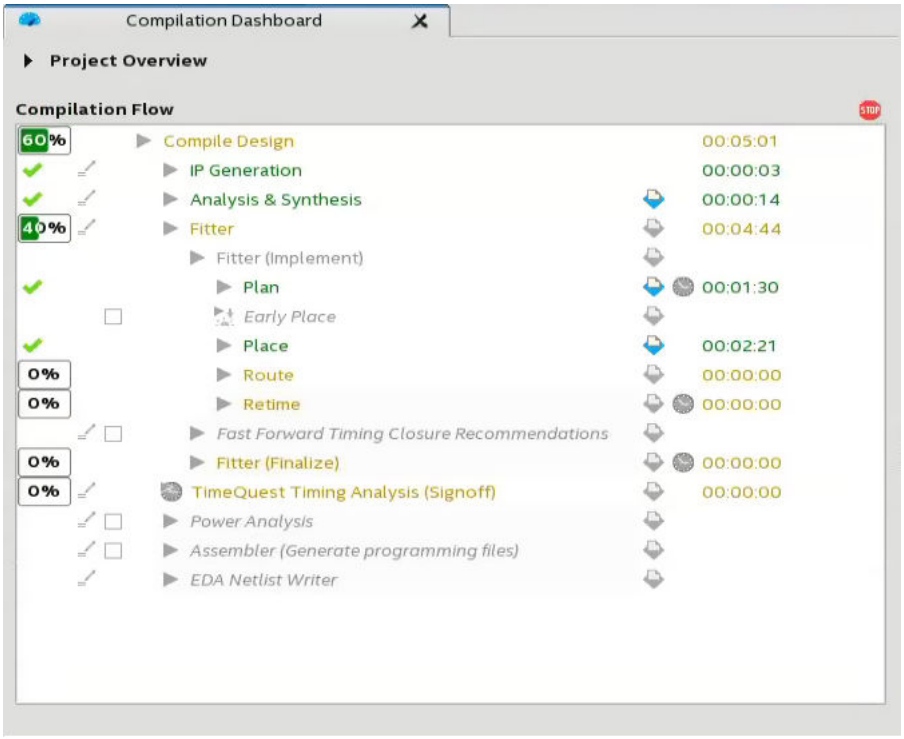
Step 3: Compile your Design

The Compiler synthesizes logic design files considering the device characteristics and design constraints.

1. Run a full design compilation by clicking **Processing ➤ Start Compilation**.

   Intel Quartus Prime Pro Edition displays the compilation stages and progress in the Compilation Dashboard.

Figure 3. Compilation Dashboard



   When the compilation finishes, modules that ran successfully show a green check image ✔.

2. Click **Processing ➤ Compilation Report** to view a report with detailed project information that helps you determine correct implementation.

   You can right-click report data to locate and edit the source in project files.

For more information, refer to the *Intel Quartus Prime Pro Edition User Guide: Design Compilation*.

Related Information

Intel Quartus Prime Pro Edition User Guide: Design Compilation

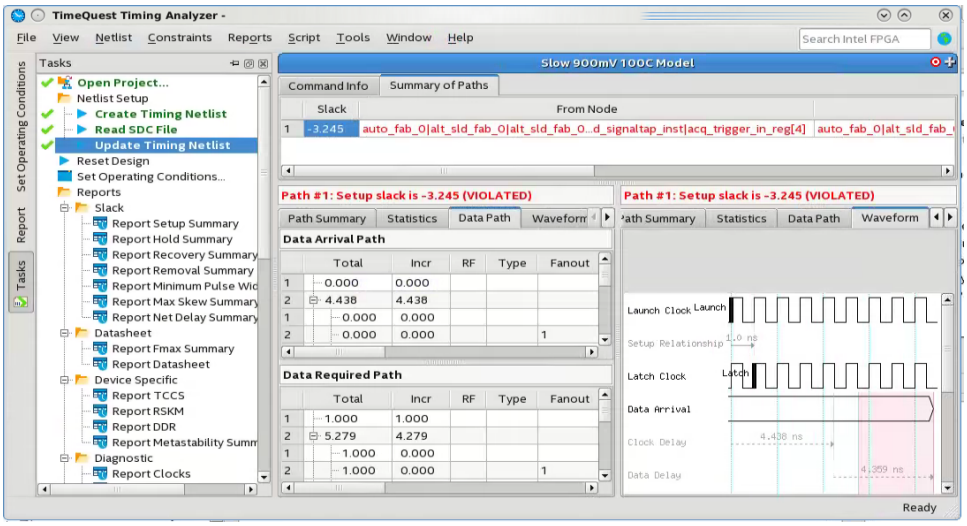
Step 4: Close Timing on your Design

The Timing Analyzer determines the timing relationships that the design must meet to function correctly and according to the timing specifications.

To perform timing analysis of a compiled design:

1. Click **Tools ➤ Timing Analyzer**.
2. In the **Tasks** window, double-click **Update Timing Netlist**.
   This action includes **Creating Timing Netlist** and **Read SDC File**.

Figure 4. Timing Report



By contrasting the timing results with the design requirements, you can determine whether the design needs further optimization, or you can continue with the next steps in the flow.

For more information, refer to *The Timing Analyzer* chapter in the *Intel Quartus Prime Pro Edition Handbook Volume 3*.

Related Information

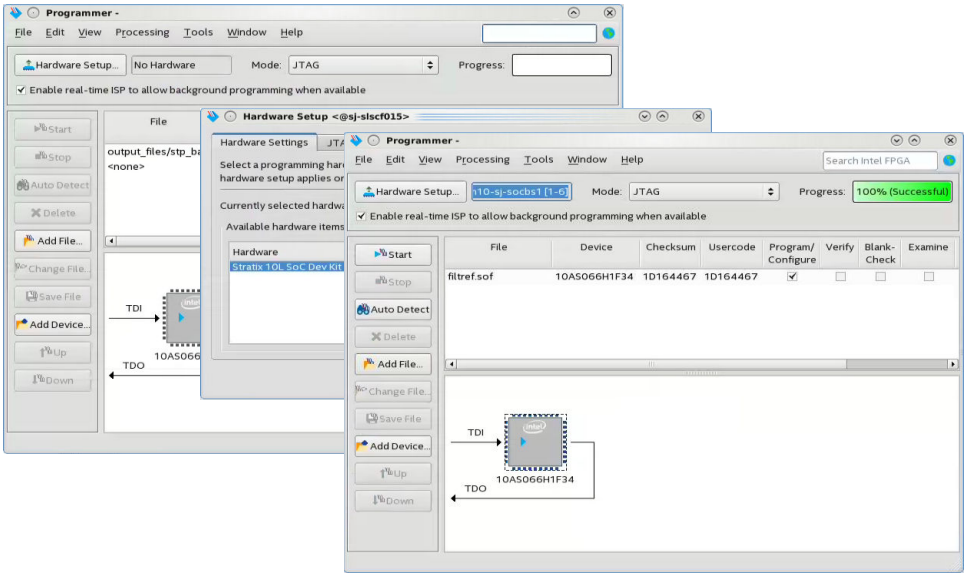
Intel Quartus Prime Pro Edition User Guide: Timing Analyzer

Step 5: Configure your Design on the Board

Once your design meets the specifications, you can create programming files and upload those files to the device.

Note: This stage assumes that you correctly connected the target device to the computer.

Figure 5. Intel Quartus Prime Programmer



1. In the Compilation Dashboard, run the Assembler stage to generate programming files.
2. Open the **Programmer** by clicking **Tools ➤ Programmer**.
3. In the **Programmer** window, click **Hardware Setup**.
4. Select the hardware for the device, and click **Close**.
5. Click **Auto Detect** to detect devices connected to the computer.
6. Click the target device in the device list.
7. Click the programming file that you want to upload to the device, and click **Start**. When the Programmer finishes, the Progress bar on the upper left corner of the window indicates the outcome.

For more information about programming devices, refer to *Programming Intel FPGA devices* chapter in the Intel Quartus Prime Pro Edition Handbook Volume 3.

Related Information

Intel Quartus Prime Pro Edition User Guide: Programmer

Document Revision History for Quick-Start for Intel Quartus Prime Pro Edition

This document has the following revision history.

Document Version	Intel Quartus Prime Version	Changes
2018.10.22	17.1.0	• Added Intel Quartus Prime version information to Revision History table. • Updated links to Intel Quartus Prime user guides.
2017.11.06	17.1.0	Initial release.