GDSC-1602AM

SPECIFICATIONS OF LCD MODULE

Ver 3.01

Features

1-1 Display type: Positive,Transmisstive,6o'clock

1-2 Driving Methed:4.85 v,1/18duty,1/5bias

1-3 Built-in controller:PCF2119

1-4 1.5-5.5V POWER SUPPLY (PCF2119)

Item	Standard Value	Unit
Module Dimension	35.0(W)*34.0(H)*2.1(T)	mm
Viewing Area	28.6(W)*19.8(H)	mm
Number of Characters	12 Characters *2Line	-
Characters Format	5*7 Dots with Icons	-
Characters Size	1.910(W)*3.915(H)	mm
Characters Pitch	2.26(W) *4.44(H)	mm
Dot Size	0.35(W) *0.525(H)	mm
Dot Pitch	0.39(W) *0.565(H)	mm
LCD Type	STN Gray,Reflective/Positive	-
Viewing Direction	6H	-
Duty	1/18	-
Bias	1/5	-
Controller	PCF2119	-
Approx Weight	5	g

Outline dimension

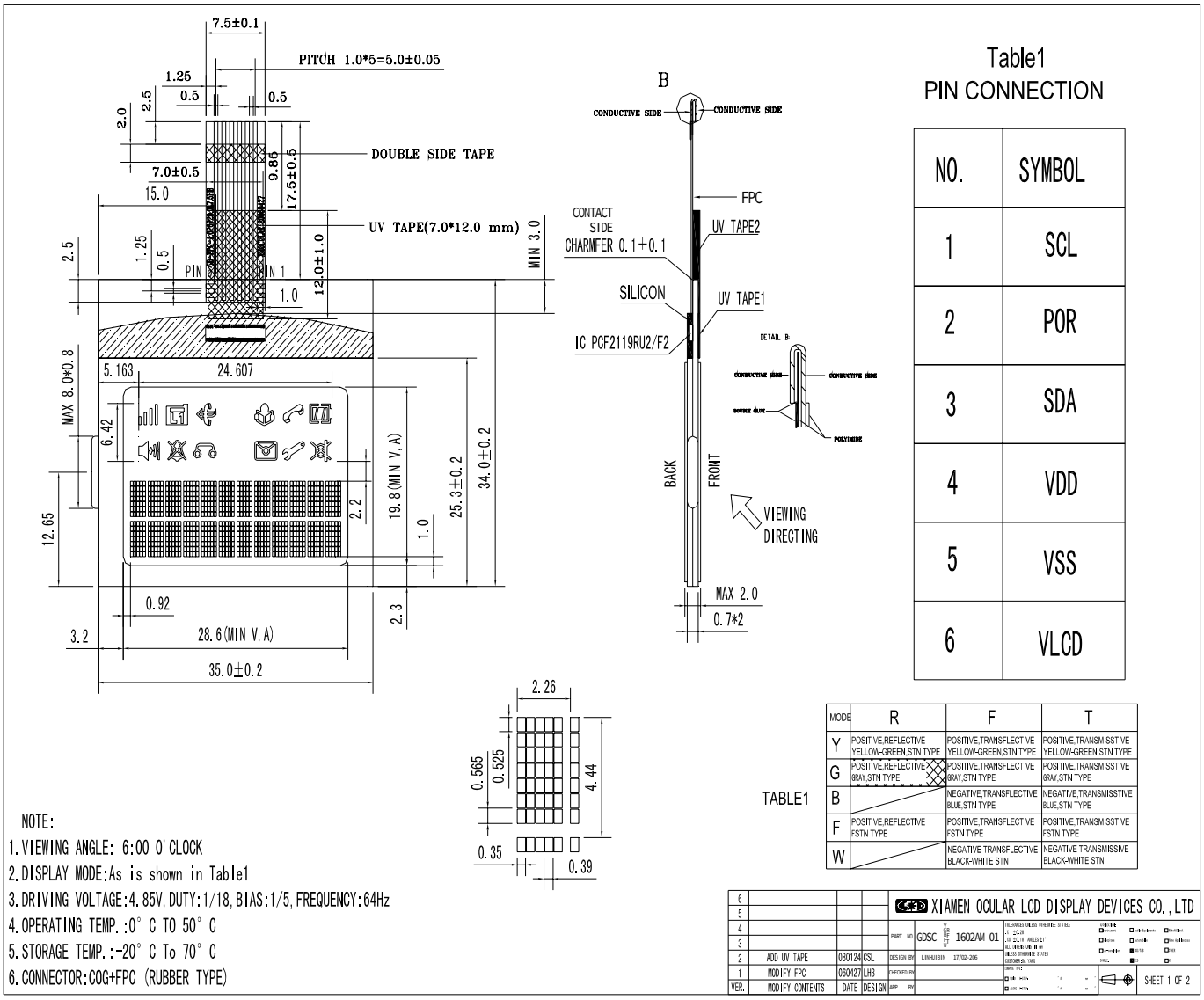


Table1
PIN CONNECTION

NO.	SYMBOL
1	SCL
2	POR
3	SDA
4	VDD
5	VSS
6	VLCD

TABLE1

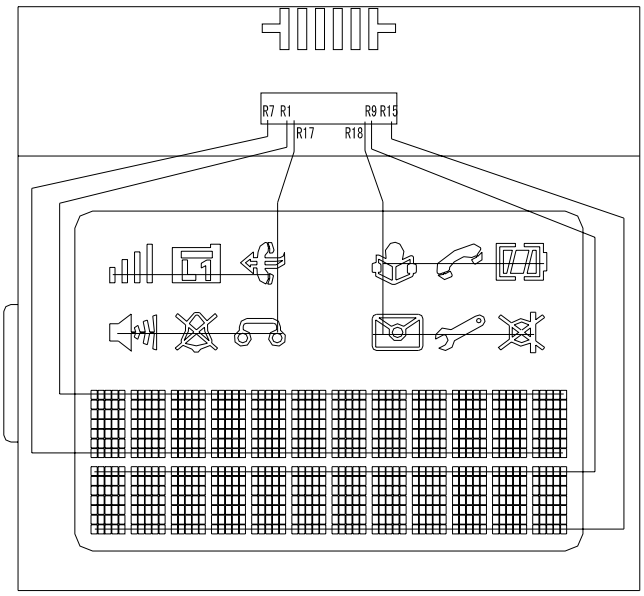
MODE	R	F	T
Y	POSITIVE,REFLECTIVE YELLOW-GREEN,STN TYPE	POSITIVE,TRANSFLECTIVE YELLOW-GREEN,STN TYPE	POSITIVE,TRANSMISSTIVE YELLOW-GREEN,STN TYPE
G	POSITIVE,REFLECTIVE GRAY,STN TYPE	POSITIVE,TRANSFLECTIVE GRAY,STN TYPE	POSITIVE,TRANSMISSTIVE GRAY,STN TYPE
B		NEGATIVE,TRANSFLECTIVE BLUE,STN TYPE	NEGATIVE,TRANSMISSTIVE BLUE,STN TYPE
F	POSITIVE,REFLECTIVE FSTN TYPE	POSITIVE,TRANSFLECTIVE FSTN TYPE	POSITIVE,TRANSMISSTIVE FSTN TYPE
W		NEGATIVE TRANSFLECTIVE BLACK-WHITE STN	NEGATIVE TRANSMISSIVE BLACK-WHITE STN

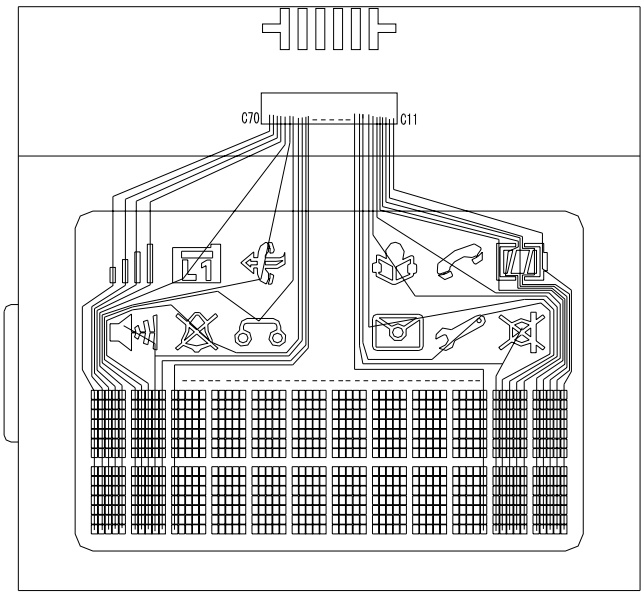
NOTE:
1. VIEWING ANGLE: 6:00 O'CLOCK
2. DISPLAY MODE:As is shown in Table1
3. DRIVING VOLTAGE:4.85V, DUTY:1/18, BIAS:1/5, FREQUENCY:64Hz
4. OPERATING TEMP.:0° C TO 50° C
5. STORAGE TEMP.:-20° C To 70° C
6. CONNECTOR:COG+FPC (RUBBER TYPE)

VER.	MODIFY CONTENTS	DATE	DESIGN
2	ADD UV TAPE	080124	CSL
1	MODIFY FPC	060427	LHB

XIAMEN OCULAR LCD DISPLAY DEVICES CO., LTD
PART NO. GDSC-1602AM-01
SHEET 1 OF 2

在 FPC 上多贴一 UV 遮光胶（尺寸为 7.0*12.0 mm）





6				XIAMEN OCULAR LCD DISPLAY DEVICES CO., LTD	
5					
4				PART NO. GDSC-1602AM-01	
3					
2				DESIGN BY LIHUIBIN 17/02-2006	
1	MODIFY FPC	060427	LHB	CHECKED BY	
VER.	MODIFY CONTENTS	DATE	DESIGN	APP BY	SHEET 2 OF 2

Absolute maximum ratings

Item	Symbol	Standard			Unit
Power supply voltage	V_{DD}-V_{SS}	0	-	5.5	V
Input voltage	VIN	VSS	-	VDD	
Operating temperature range	T_A	-20	-	+70	℃
Storage temperature range	T_{STO}	-30	-	+80	

*****Wide temperature range is available

Interface pin description

Pin No	Symbol	Level	Function
1	VLCD	-	POWER SUPPLY FOR LCD
2	VSS	-	GROUND
3	VDD	-	POWER SUPPLY FOR LOGIC
4	SDA	H/L	I2C-BUS SERIAL DATA INPUT/OUTPUT
5	POR	H/L	EXTERNAL POWER-ON RESET INPUT
6	SCL	H/L	I2C-BUS SERIAL CLOCK INPUT

Display Address:

Display Position	1	2	3	4	5	6	7	8	9	10	11	12
DD RAM Address	02	03	04	05	06	07	08	09	0A	0B	0C	0D
DD RAM Address	42	43	44	45	46	47	48	49	4A	4B	4C	4D

Optical characteristics

STN type display module (Ta=25℃, VDD=5.5V)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Viewing angle	θ	$C_r \geq 2$	-60	-	35	deg
	Φ		-40	-	40	
Contrast ratio	C_r		-	6	-	-
Response time (rise)	T_r	-	-	150	250	ms
Response time (fall)	T_r	-	-	150	250	

Electrical characteristics

DC characteristics

V_{DD1} = 1.5 to 5.5 V; V_{DD2} = V_{DD3} = 2.2 to 4.0 V; V_{SS} = 0 V; V_{LCD} = 2.2 to 6.5 V; T_{amb} = −40 to +85 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_{DD1}	logic supply voltage		1.5	–	5.5	V
V_{DD2}, V_{DD3}	high voltage generator supply voltage	internal V_{LCD} generation (V_{DD2} = V_{DD3} < V_{LCD})	2.2	–	4.0	V
V_{LCD}	LCD supply voltage		2.2	–	6.5	V
GROUND SUPPLY CURRENT (I_{SS}); EXTERNAL V_{LCD}; note 1						
I_{SS1}	ground supply current 1		–	70	120	µA
I_{SS3}	ground supply current 3	V_{DD} = 3 V; V_{LCD} = 5 V; note 2	–	35	80	µA
I_{SS4}	ground supply current 4	icon mode; V_{DD} = 3 V; V_{LCD} = 2.5 V; note 2	–	25	45	µA
I_{SS5}	ground supply current 5	power-down mode; V_{DD} = 3 V; V_{LCD} = 2.5 V; DB7 to DB0, RS and R/$\overline{W}$ = 1; OSC = 0; PD = 1	–	0.5	5	µA
GROUND SUPPLY CURRENT (I_{SS}); INTERNAL V_{LCD}; notes 1 and 3						
I_{SS6}	ground supply current 6		–	190	400	µA
I_{SS8}	ground supply current 8	V_{DD} = 3 V; V_{LCD} = 5 V; note 2	–	135	400	µA
I_{SS9}	ground supply current 9	icon mode; V_{DD} = 2.5 V; V_{LCD} = 2.5 V; note 2	–	85	–	µA
Logic						
V_{IL}	LOW-level input voltage		V_{SS1}	–	$0.3V_{DD1}$	V
V_{IH}	HIGH-level input voltage		$0.7V_{DD1}$	–	V_{DD1}	V
$V_{IL(osc)}$	LOW-level input voltage pad OSC	V_{DD} = $V_{DD(min)}$, $V_{DD(max)}$	V_{SS1}	–	V_{DD1} − 1.2	V
$V_{IH(osc)}$	HIGH-level voltage pad OSC	V_{DD} = $V_{DD(min)}$, $V_{DD(max)}$	V_{DD1} − 0.1	–	V_{DD1}	V
$I_{OL(DB)}$	LOW-level output current pads DB7 to DB0	V_{OL} = 0.4 V; V_{DD1} = 5 V	1.6	4	–	mA
$I_{OH(DB)}$	HIGH-level output current pads DB7 to DB0	V_{OH} = 4 V; V_{DD1} = 5 V	−1	−8	–	mA
I_{pu}	pull-up current pads DB7 to DB0	V_I = V_{SS}, $V_{DD(min)}$, $V_{DD(max)}$	0.04	0.15	1	µA
I_L	leakage current	V_I = $V_{DD1,2,3}$ or $V_{SS1,2}$	−1	–	+1	µA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I²C-bus						
SDA AND SCL						
V_{IL2}	LOW-level input voltage		0	–	$0.3V_{DD}$	V
V_{IH2}	HIGH-level input voltage		$0.7V_{DD}$	–	5.5	V
I_{LI}	input leakage current	$V_I = V_{DD}$ or V_{SS}	−1	–	+1	μA
C_i	input capacitance		–	5	–	pF
$I_{OL(SDA)}$	LOW-level output current SDA	V_{OL} = 0.4 V; V_{DD} > 2 V	3	–	–	mA
		$V_{OL} = 0.2V_{DD}$; V_{DD} < 2 V	2	–	–	mA
LCD outputs						
$R_{O(ROW)}$	row output resistance pads R1 to R18	note 4	–	10	30	kΩ
$R_{O(COL)}$	column output resistance pads C1 to C80	note 4	–	15	40	kΩ
$V_{bias(tol)}$	bias tolerance pads R1 to R18 and C1 to C80	note 5	–	20	130	mV
$V_{LCD(tol)}$	V_{LCD} tolerance	T_{amb} = 25 °C; note 3				
		V_{LCD} < 3 V	–	–	160	mV
		V_{LCD} < 4 V	–	–	200	mV
		V_{LCD} < 5 V	–	–	260	mV
		V_{LCD} < 6 V	–	–	340	mV
TC0	V_{LCD} temperature coefficient 0		–	−0.16	–	%/K
TC1	V_{LCD} temperature coefficient 1		–	−0.18	–	%/K
TC2	V_{LCD} temperature coefficient 2		–	−0.21	–	%/K
TC3	V_{LCD} temperature coefficient 3		–	−0.24	–	%/K

Notes

1. LCD outputs are open-circuit; inputs at V_{DD} or V_{SS}; bus inactive.
2. T_{amb} = 25 °C; f_{OSC} = 200 kHz.
3. LCD outputs are open-circuit; HV generator is on; load current I_{LCD} = 5 μA.
4. Resistance of output terminals (R1 to R18 and C1 to C80) with a load current of 10 μA; outputs measured one at a time; external V_{LCD}; V_{LCD} = 3 V; $V_{DD1} = V_{DD2} = V_{DD3}$ = 3 V.
5. LCD outputs open-circuit; external V_{LCD}.

AC characteristics

V_{DD1} = 1.5 to 5.5 V; V_{DD2} = V_{DD3} = 2.2 to 4.0 V; V_{SS} = 0 V; V_{LCD} = 2.2 to 6.5 V; T_{amb} = −40 to +85 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
f_{FR}	LCD frame frequency (internal clock)	V_{DD} = 5.0 V	45	95	147	Hz
f_{OSC}	oscillator frequency (not available at any pad)		140	250	450	kHz
$f_{OSC(ext)}$	external clock frequency		140	–	450	kHz
t_{OSCST}	oscillator start-up time after power-down	note 1	–	200	300	µs
Bus timing characteristics: parallel interface; note 2						
WRITE OPERATION (WRITING DATA FROM MPU TO PCF2119X)						
$T_{cy(en)}$	enable cycle time		500	–	–	ns
$t_{W(en)}$	enable pulse width		220	–	–	ns
$t_{su(A)}$	address set-up time		50	–	–	ns
$t_{h(A)}$	address hold time		25	–	–	ns
$t_{su(D)}$	data set-up time		60	–	–	ns
$t_{h(D)}$	data hold time		25	–	–	ns
READ OPERATION (READING DATA FROM PCF2119X TO MPU)						
$T_{cy(en)}$	enable cycle time		500	–	–	ns
$t_{W(en)}$	enable pulse width		220	–	–	ns
$t_{su(A)}$	address set-up time		50	–	–	ns
$t_{h(A)}$	address hold time		25	–	–	ns
$t_{d(D)}$	data delay time	V_{DD1} > 2.2 V	–	–	150	ns
		V_{DD1} > 1.5 V	–	–	250	ns
$t_{h(D)}$	data hold time		20	–	100	ns
Timing characteristics: I^2C-bus interface; note 2						
f_{SCL}	SCL clock frequency		–	–	400	kHz
t_{LOW}	SCL clock low period		1.3	–	–	µs
t_{HIGH}	SCL clock high period		0.6	–	–	µs
$t_{SU;DAT}$	data set-up time		100	–	–	ns
$t_{HD;DAT}$	data hold time		0	–	–	ns
t_r	SCL, SDA rise time	notes 1 and 3	15 + 0.1C_B	–	300	ns
t_f	SCL, SDA fall time	notes 1 and 3	15 + 0.1C_B	–	300	ns
C_B	capacitive bus line load		–	–	400	pF
$t_{SU;STA}$	set-up time for a repeated START condition		0.6	–	–	µs
$t_{HD;STA}$	START condition hold time		0.6	–	–	µs
$t_{SU;STO}$	set-up time for STOP condition		0.6	–	–	µs
t_{SW}	tolerable spike width on bus		–	–	50	ns
t_{BUF}	bus free time between STOP and START condition		1.3	–	–	µs

Command Description

8.1 Clear display

'Clear display' writes character code 20H into all DDRAM addresses (the character pattern for character code 20H must be a blank pattern), sets the DDRAM address counter to logic 0 and returns the display to its original position, if it was shifted. Thus, the display disappears and the cursor or blink position goes to the left edge of the display. Sets entry mode I/D = 1 (increment mode). S of entry mode does not change.

The instruction 'clear display' requires extra execution time. This may be allowed by checking the Busy Flag (BF) or by waiting until the 165 clock cycles have elapsed. The latter must be applied where no read-back options are foreseen, as in some Chip-On-Glass (COG) applications.

8.2 Return home

'Return home' sets the DDRAM address counter to logic 0 and returns the display to its original position if it was shifted. DDRAM contents do not change. The cursor or blink position goes to the left of the first display line. I/D and S of entry mode do not change.

8.3 Entry mode set

8.3.1 I/D

When I/D = 1 (0) the DDRAM or CGRAM address increments (decrements) by 1 when data is written into or read from the DDRAM or CGRAM. The cursor or blink position moves to the right when incremented and to the left when decremented. The cursor underline and cursor character blink are inhibited when the CGRAM is accessed.

8.3.2 S

When S = 1, the entire display shifts either to the right (I/D = 0) or to the left (I/D = 1) during a DDRAM write. Thus it appears as if the cursor stands still and the display moves. The display does not shift when reading from the DDRAM, or when writing to or reading from the CGRAM. When S = 0, the display does not shift.

8.4 Display control (and partial power-down mode)

8.4.1 D

The display is on when D = 1 and off when D = 0. Display data in the DDRAM is not affected and can be displayed immediately by setting D to a logic 1.

When the display is off (D = 0) the chip is in partial power-down mode:

- The LCD outputs are connected to V_{SS}
- The LCD generator and bias generator are turned off.

Three oscillator cycles are required after sending the 'display off' instruction to ensure all outputs are at V_{SS}, afterwards OSC can be stopped. If the oscillator is running during partial power-down mode ('display off') the chip can still execute instructions. Even lower current consumption is obtained by inhibiting the oscillator (OSC = V_{SS}).

To ensure I_{DD} <1 μA, the parallel bus pads DB7 to DB0 should be connected to V_{DD}; RS and R/$\overline{W}$ to V_{DD} or left open-circuit and PD to V_{DD}. Recovery from power-down mode: PD back to logic 0, if necessary OSC back to V_{DD} and send a 'display control' instruction with D = 1.

8.4.2 C

The cursor is displayed when C = 1 and inhibited when C = 0. Even if the cursor disappears, the display functions I/D, etc. remain in operation during display data write. The cursor is displayed using 5 dots in the 8th line (see Fig.5).

8.4.3 B

The character indicated by the cursor blinks when B = 1. The cursor character blink is displayed by switching between display characters and all dots on with a period of approximately 1 second, with $f_{blink} = \frac{f_{OSC}}{52\,224}$

The cursor underline and the cursor character blink can be set to display simultaneously.

8.5 Cursor or display shift

'Cursor/display shift' moves the cursor position or the display to the right or left without writing or reading display data. This function is used to correct a character or move the cursor through the display. In 2-line displays, the cursor moves to the next line when it passes the last position (40) of the line.

When the displayed data is shifted repeatedly all lines shift at the same time; displayed characters do not shift into the next line.

The Address Counter (AC) content does not change if the only action performed is shift display, but increments or decrements with the 'cursor shift'.

8.6 Function set

8.6.1 DL (PARALLEL MODE ONLY)

Sets interface data width. Data is sent or received in bytes (DB7 to DB0) when DL = 1 or in two nibbles (DB7 to DB4) when DL = 0. When 4-bit width is selected, data is transmitted in two cycles using the parallel bus. In a 4-bit application DB3 to DB0 should be left open-circuit (internal pull-ups). Hence in the first 'function set' instruction after power-on, M, SL and H are set to logic 1. A second 'function set' must then be sent (2 nibbles) to set M, SL and H to their required values.

'Function set' from the I^2C-bus interface sets the DL bit to logic 1.

8.6.2 M

Selects either 1-line by 32 display (M = 0) or 2-line by 16 display (M = 1).

8.6.3 SL

Selects MUX 1 : 9, 1-line by 16 display (independent of M and L). Only rows 1 to 8 and 17 are to be used. All other rows must be left open-circuit. The DDRAM map is the same as in the 2-line by 16 display mode, however, the second line is not displayable.

8.6.4 H

When H = 0 the chip can be programmed via the standard 11 instruction codes used in the PCF2116 and other LCD controllers.

When H = 1 the extended range of instructions will be used. These are mainly for controlling the display configuration and the icons.

8.7 Set CGRAM address

'Set CGRAM address' sets bits 5 to 0 of the CGRAM address A_{CG} into the address counter (binary A5 to A0). Data can then be written to or read from the CGRAM.

Attention: the CGRAM address uses the same address register as the DDRAM address and consists of 7 bits (binary A6 to A0). With the 'set CGRAM address' command, only bits 5 to 0 are set. Bit 6 can be set using the 'set DDRAM address' command first, or by using the auto-increment feature during CGRAM write. All bits 6 to 0 can be read using the 'read busy flag' and 'read address' command.

When writing to the lower part of the CGRAM, ensure that bit 6 of the address is not set (e.g. by an earlier DDRAM write or read action).

8.8 Set DDRAM address

'Set DDRAM address' sets the DDRAM address A_{DD} into the address counter (binary A6 to A0). Data can then be written to or read from the DDRAM.

8.9 Read busy flag and read address

'Read busy flag' and 'read address' read the Busy Flag (BF) and Address Counter (AC). BF = 1 indicates that an internal operation is in progress. The next instruction will not be executed until BF = 0. It is recommended that the BF status is checked before the next write operation is executed.

At the same time, the value of the address counter expressed in binary A6 to A0 is read out. The address counter is used by both CGRAM and DDRAM, and its value is determined by the previous instruction.

8.10 Write data to CGRAM or DDRAM

'Write data' writes binary 8-bit data D7 to D0 to the CGRAM or the DDRAM.

Whether the CGRAM or DDRAM is to be written into is determined by the previous 'set CGRAM address' or 'set DDRAM address' command. After writing, the address automatically increments or decrements by 1, in accordance with the entry mode. Only bits D4 to D0 of CGRAM data are valid, bits D7 to D5 are 'don't care'.

8.11 Read data from CGRAM or DDRAM

'Read data' reads binary 8-bit data D7 to D0 from the CGRAM or DDRAM.

The most recent 'set address' command determines whether the CGRAM or DDRAM is to be read.

The 'read data' instruction gates the content of the Data Register (DR) to the bus while E is HIGH. After E goes LOW again, internal operation increments (or decrements) the AC and stores RAM data corresponding to the new AC into the DR.

There are only three instructions that update the data register:

- 'set CGRAM address'
- 'set DDRAM address'
- 'read data' from CGRAM or DDRAM.

Other instructions (e.g. 'write data', 'cursor/display shift', 'clear display' and 'return home') do not modify the data register content.

9 EXTENDED FUNCTION SET INSTRUCTIONS AND FEATURES

9.1 New instructions

H = 1, sets the chip into alternate instruction set mode.

9.2 Icon control

The PCF2119x can drive up to 160 icons. See Fig.19 for CGRAM to icon mapping.

9.3 IM

When IM = 0, the chip is in character mode. In the character mode characters and icons are driven (MUX 1 : 18). The V_{LCD} generator, if used, produces the V_{LCD} voltage programmed in register V_A.

When IM = 1, the chip is in icon mode. In the icon mode only the icons are driven (MUX 1 : 2) and the V_{LCD} voltage generator, if used, produces the V_{LCD} voltage as programmed in register V_B.

9.4 IB

Icon blink control is independent of the cursor/character blink function.

When IB = 0, icon blink is disabled. Icon data is stored in CGRAM character 0 to 3 ($4 \times 8 \times 5 = 160$ bits for 160 icons).

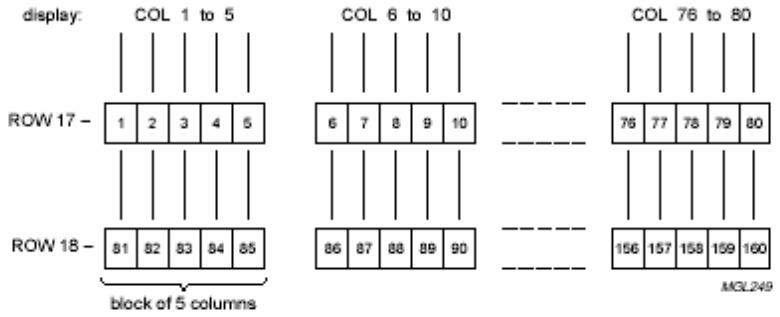
When IB = 1, icon blink is enabled. In this case each icon is controlled by two bits. Blink consists of two half phases (corresponding to the cursor on and off phases called even and odd phases hereafter).

Icon states for the even phase are stored in CGRAM characters 0 to 3 ($4 \times 8 \times 5 = 160$ bits for 160 icons). These bits also define the icon state when icon blink is not used.

Icon states for the odd phase are stored in CGRAM character 4 to 7 (another 160 bits for the 160 icons). When icon blink is disabled CGRAM characters 4 to 6 may be used as normal CGRAM characters.

Table 10 Blink effect for icons and cursor character blink

PARAMETER	EVEN PHASE	ODD PHASE
Cursor character blink	block (all on)	normal (display character)
Icons	state 1: CGRAM character 0 to 2	state 2: CGRAM character 4 to 6



icon no.	phase	ROW/COL	character codes	CGRAM address	CGRAM data	icon view
			7 6 5 4 3 2 1 0 MSB LSB	6 5 4 3 2 1 0 MSB LSB	4 3 2 1 0 MSB LSB	
1-5	even	17/1-5	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0	1 0 1 0 1	
6-10	even	17/6-10	0 0 0 0 0 0 0 0	0 0 0 0 0 0 1	0 1 0 1 0	
11-15	even	17/11-15	0 0 0 0 0 0 0 0	0 0 0 0 0 1 0	0 1 1 1 0	
⋮	⋮	⋮	⋮	⋮	⋮	⋮
76-80	even	17/76-80	0 0 0 0 0 0 0 1	0 0 0 1 1 1 1	1 1 1 1 1	
81-85	even	18/1-5	0 0 0 0 0 0 1 0	0 0 1 0 0 0 0	1 1 0 0 0	
⋮	⋮	⋮	⋮	⋮	⋮	⋮
156-160	even	18/76-80	0 0 0 0 0 0 1 1	0 0 1 1 1 1 1	1 1 1 0 1	
1-5	odd (blink)	17/1-5	0 0 0 0 0 1 0 0	0 1 0 0 0 0 0	0 0 0 0 0	
⋮	⋮	⋮	⋮	⋮	⋮	⋮
156-160	odd (blink)	18/76-80	0 0 0 0 0 1 1 1	0 1 1 1 1 1 1	0 0 1 1 0	

MGK999

CGRAM data bit = logic 1 turns the icon on, data bit = logic 0 turns the icon off.

Data in character codes 0 to 3 define the icon state when icon blink is disabled or during the even phase when icon blink is enabled.

Data in character codes 4 to 7 define the icon state during the odd phase when icon blink is enabled (not used for icons when icon blink is disabled).

Fig.19 CGRAM to icon mapping.

9.5 Normal/icon mode operation

IM	CONDITION	V_{LCD}
0	character mode	generates V_A
1	icon mode	generates V_B

9.6 Direct mode

When DM = 0, the chip is not in direct mode. Either the internal voltage generator or an external voltage may be used to achieve the necessary V_{LCD} value.

When DM = 1, the chip is in direct mode. The internal voltage generator is turned off and the V_{LCD} output is directly connected to the HVgen supply voltage V_{DD2}.

The direct mode can be used to reduce the current consumption when the required V_{LCD} output voltage is close to the V_{DD2} supply voltage. This can be the case in icon mode or in Mux 1 : 9 (depending on LCD liquid properties).

9.7 Voltage multiplier control

S[1:0]

A software configurable voltage multiplier is incorporated and can be set via 'Set HVgen stages' command.

The voltage multiplier control can be used to reduce current consumption by disconnecting internal voltage multiplier stages (depending on the required V_{LCD} output voltage).

9.8 Screen configuration

L: default is L = 0.

L = 0: the two halves of a split screen are connected in a standard way i.e. column 1/81, 2/82 to 80/160.

L = 1: the two halves of a split screen are connected in a mirrored way i.e. column 1/160, 2/159 to 80/81. This allows single layer PCB or glass layout.

9.9 Display configuration

P, Q: default is P, Q = 0.

P = 1: mirrors the column data.

Q = 1: mirrors the row data.

9.10 TC1 and TC2

Default is TC1 and TC2 = 0. This selects the default temperature coefficient for the internally generated V_{LCD}. TC1 and TC2 = 10, 01 and 11 selects alternative temperature coefficients 1, 2 and 3 respectively.

9.11 Set V_{LCD}

The V_{LCD} value is programmed by instruction. Two on-chip registers hold V_{LCD} values for the character mode and the icon mode respectively (V_A and V_B). The generated V_{LCD} value is independent of V_{DD}, allowing battery operation of the chip.

V_{LCD} programming:

1. Send 'function set' instruction with H = 1
2. Send 'set V_{LCD}' instruction to write to voltage register:
   a) DB7, DB6 = 10: DB5 to DB0 are V_{LCD} of character mode (V_A)
   b) DB7, DB6 = 11: DB5 to DB0 are V_{LCD} of icon mode (V_B)
   c) DB5 to DB0 = 000000 switches V_{LCD} generator off (when selected)
   d) During 'display off' and power-down the V_{LCD} generator is also disabled.
3. Send 'function set' instruction with H = 0 to resume normal programming.

9.12 Reducing current consumption

Reducing current consumption can be achieved by one of the options given in Table 11.

When V_{LCD} lies outside the V_{DD} range and must be generated, it is usually more efficient to use the on-chip generator than an external regulator.

Table 11 Reducing current consumption

ORIGINAL MODE	ALTERNATIVE MODE
Character mode	icon mode (control bit IM)
Display on	display off (control bit D)
HV generator operating	direct mode
Any mode	power-down (PD pad)

Table 12 Use of the V_A and V_B registers

MODE	V_A	V_B
Normal operation	V_{LCD} character mode	V_{LCD} icon mode

Table 17 Example of I²C-bus operation; 1-line display (using external reset, assuming SA0 = V_{SS}; note 1)

STEP	I²C BYTE									DISPLAY	OPERATION
1	I²C-bus start										initialized; no display appears
2	slave address for write										during the acknowledge cycle SDA will be pulled-down by the PCF2119x
	SA6	SA5	SA4	SA3	SA2	SA1	SA0	R/$\overline{W}$	Ack		
	0	1	1	1	0	1	0	0	1		
3	send a control byte for 'function set'										control byte sets RS for following data bytes
	Co	RS	0	0	0	0	0	0	Ack		
	0	0	0	0	0	0	0	0	1		
4	function set										selects 1-line display and $V_{LCD} = V_0$; SCL pulse during acknowledge cycle starts execution of instruction
	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Ack		
	0	0	1	X	0	0	0	0	1		
5	display on/off control									_	turns on display and cursor; entire display shows character 20H (blank in ASCII-like character sets)
	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Ack		
	0	0	0	0	1	1	1	0	1		
6	entry mode set									_	sets mode to increment the address by 1 and to shift the cursor to the right at the time of write to the DDRAM or CGRAM; display is not shifted
	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Ack		
	0	0	0	0	0	1	1	0	1		
7	I²C start									_	for writing data to DDRAM, RS must be set to 1; therefore a control byte is needed
8	slave address for write									_	
	SA6	SA5	SA4	SA3	SA2	SA1	SA0	R/$\overline{W}$	Ack		
	0	1	1	1	0	1	0	0	1		
9	send a control byte for 'write data'									_	
	Co	RS	0	0	0	0	0	0	Ack		
	0	1	0	0	0	0	0	0	1		
10	'write data' to DDRAM									**P**_	writes 'P'; the DDRAM has been selected at power-up; the cursor is incremented by 1 and shifted to the right
	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Ack		
	0	1	0	1	0	0	0	0	1		
11	'write data' to DDRAM									**PH**_	writes 'H'
	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Ack		
	0	1	0	0	1	0	0	0	1		

STEP	I²C BYTE	DISPLAY	OPERATION
12 to 15			
16	'write data' to DDRAM DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 Ack 0 1 0 1 0 0 1 1 1	**PHILIPS_**	writes 'S'
17	(optional I²C stop) I²C start + slave address for write (as step 8)	**PHILIPS_**	
18	control byte Co RS 0 0 0 0 0 0 Ack 1 0 0 0 0 0 0 0 1	**PHILIPS_**	
19	return home DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 Ack 0 0 0 0 0 0 1 0 1	**PHILIPS**	sets DDRAM address 0 in address counter (also returns shifted display to original position; DDRAM contents unchanged); this instruction does not update the Data Register (DR)
20	I²C start	**PHILIPS**	
21	slave address for read SA6 SA5 SA4 SA3 SA2 SA1 SA0 R/$\overline{W}$ Ack 0 1 1 1 0 1 0 1 1	**PHILIPS**	during the acknowledge cycle the content of the DR is loaded into the internal I²C-bus interface to be shifted out; in the previous instruction neither a 'set address' nor a 'read data' has been performed; therefore the content of the DR was unknown; the R/$\overline{W}$ has to be set to 1 while still in I²C-write mode
22	control byte for read Co RS 0 0 0 0 0 0 Ack 0 1 1 0 0 0 0 0 1	**PHILIPS**	DDRAM content will be read from following instructions
23	'read data': 8 × SCL + master acknowledge; note 2 DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 Ack X X X X X X X X 0	**PHILIPS**	8 × SCL; content loaded into interface during previous acknowledge cycle is shifted out over SDA; MSB is DB7; during master acknowledge content of DDRAM address 01 is loaded into the I²C-bus interface

STEP	I²C BYTE	DISPLAY	OPERATION
24	'read data': 8 × SCL + master acknowledge; note 2 DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 Ack 0 1 0 0 1 0 0 0 0	**PHILIPS**	8 × SCL; code of letter 'H' is read first; during master acknowledge code of 'I' is loaded into the I²C interface
25	'read data': 8 × SCL + no master acknowledge; note 2 DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 Ack 0 1 0 0 1 0 0 1 1	**PHILIPS**	no master acknowledge; after the content of the I²C-bus interface register is shifted out no internal action is performed; no new data is loaded to the interface register, data register is not updated, address counter is not incremented and cursor is not shifted
26	I²C stop	**PHILIPS**	

Notes

1. X = don't care.
2. SDA is left at high-impedance by the microcontroller during the read acknowledge.

Application

10 INTERFACES TO MPU

10.1 Parallel interface

The PCF2119x can send data in either two 4-bit operations or one 8-bit operation and can thus interface to 4-bit or 8-bit microcontrollers.

In 8-bit mode data is transferred as 8-bit bytes using the 8 data lines DB7 to DB0. Three further control lines E, RS and R/$\overline{W}$ are required; see Section 6.1.

In 4-bit mode data is transferred in two cycles of 4 bits each using pads DB7 to DB4 for the transaction. The higher order bits (corresponding to DB7 to DB4 in 8-bit mode) are sent in the first cycle and the lower order bits (DB3 to DB0 in 8-bit mode) in the second. Data transfer is complete after two 4-bit data transfers. It should be noted that two cycles are also required for the busy flag check. 4-bit operation is selected by instruction, see Figs 16 to 18 for examples of bus protocol.

In 4-bit mode, pads DB3 to DB0 must be left open-circuit. They are pulled up to V_{DD} internally.

10.2 I²C-bus interface

The I²C-bus is for bidirectional, two-line communication between different ICs or modules. The two lines are the Serial Data line (SDA) and the Serial Clock Line (SCL). Both lines must be connected to a positive supply via pull-up resistors. Data transfer may be initiated only when the bus is not busy.

Each byte of eight bits is followed by an acknowledge bit. The acknowledge bit is a HIGH level signal put on the bus by the transmitter during which time the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte.

Also a master receiver must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter.

The device that acknowledges must pull-down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse (set-up and hold times must be taken into consideration).

A master receiver must signal an end of data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a STOP condition.

10.2.1 I²C-BUS PROTOCOL

Before any data is transmitted on the I²C-bus, the device which should respond is addressed first. The addressing is always carried out with the first byte transmitted after the START procedure. The I²C-bus configuration for the different PCF2119x read and write cycles is shown in Figs 24 to 26. The slow down feature of the I²C-bus protocol (receiver holds SCL LOW during internal operations) is not used in the PCF2119x.

10.2.2 DEFINITIONS

- Transmitter: the device which sends the data to the bus
- Receiver: the device which receives the data from the bus
- Master: the device which initiates a transfer, generates clock signals and terminates a transfer
- Slave: the device addressed by a master
- Multi-master: more than one master can attempt to control the bus at the same time without corrupting the message
- Arbitration: procedure to ensure that, if more than one master simultaneously tries to control the bus, only one is allowed to do so and the message is not corrupted
- Synchronization: procedure to synchronize the clock signals of two or more devices.

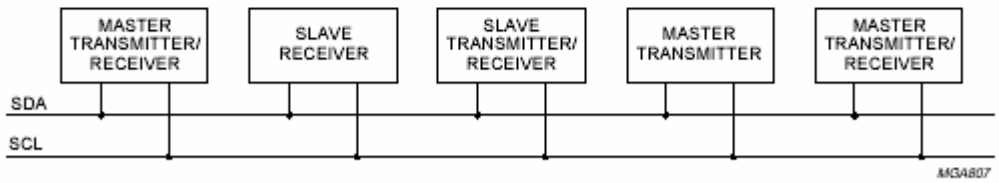


Fig.20 System configuration.

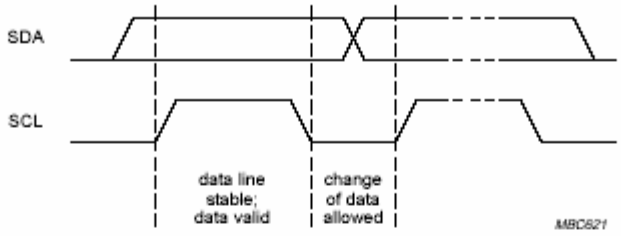


Fig.21 Bit transfer.

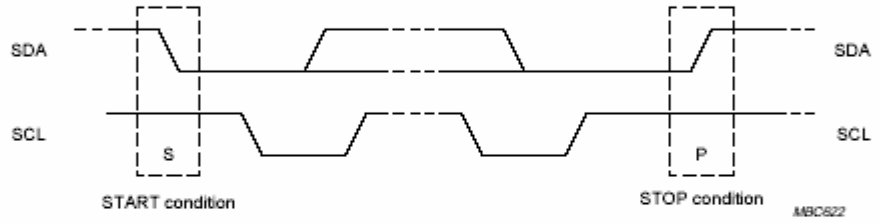


Fig.22 Definition of START and STOP conditions.

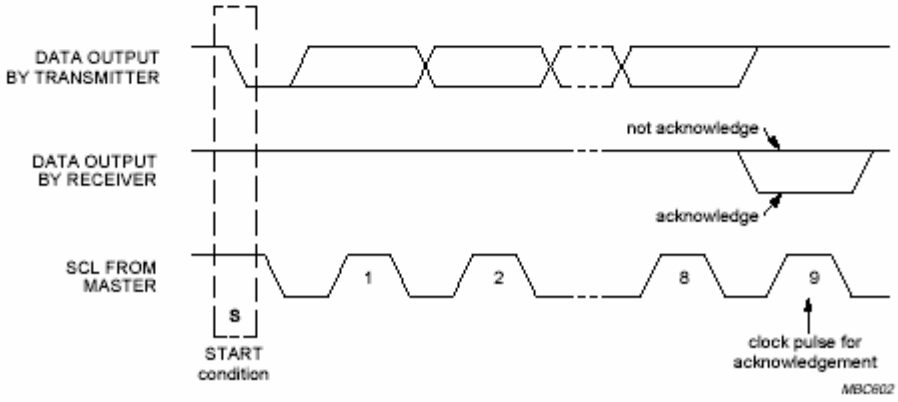


Fig.23 Acknowledgement on the I²C-bus.

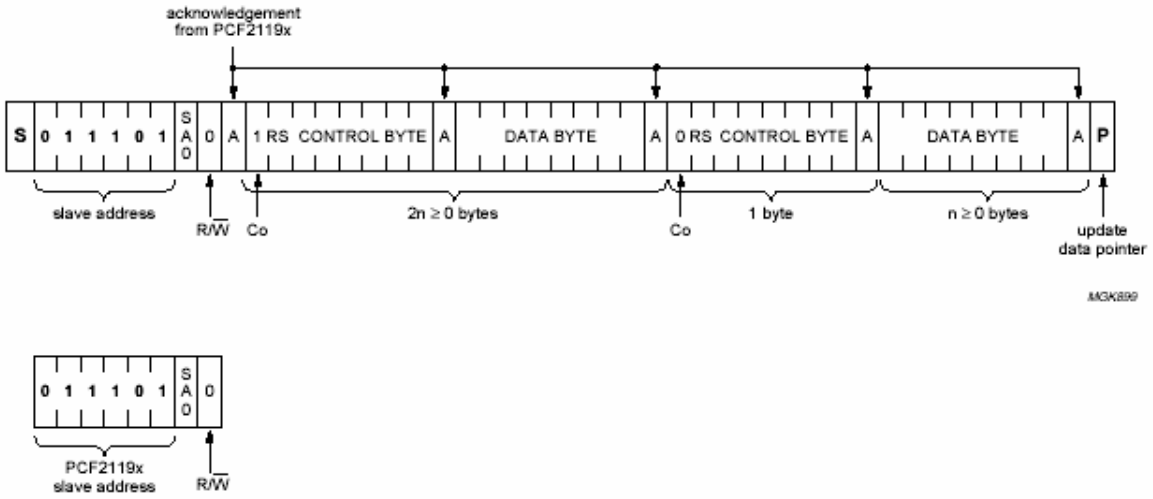
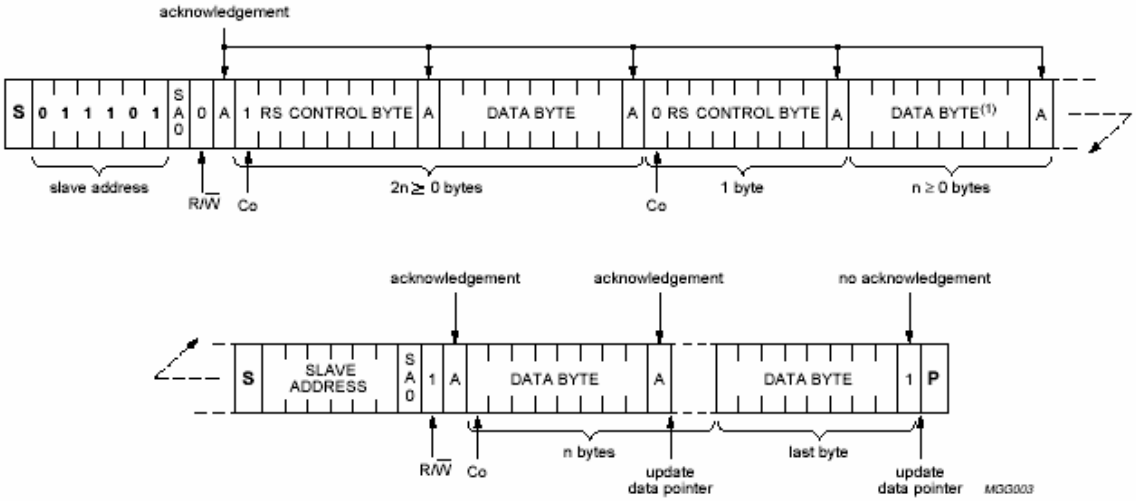


Fig.24 Master transmits to slave receiver; write mode.



(1) Last data byte is a dummy byte (may be omitted).

Fig.25 Master reads after setting word address; writes word address, set RS; 'read data'.

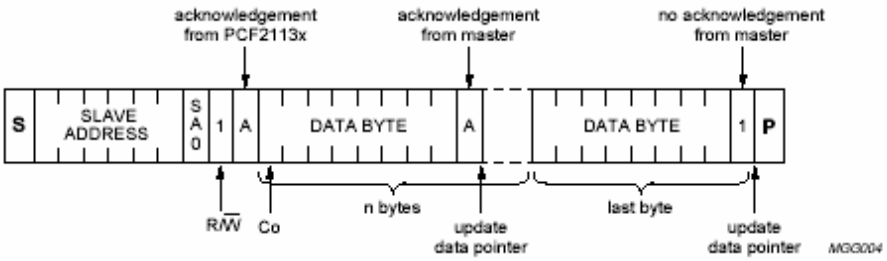


Fig.26 Master reads slave immediately after first byte; read mode (RS previously defined).

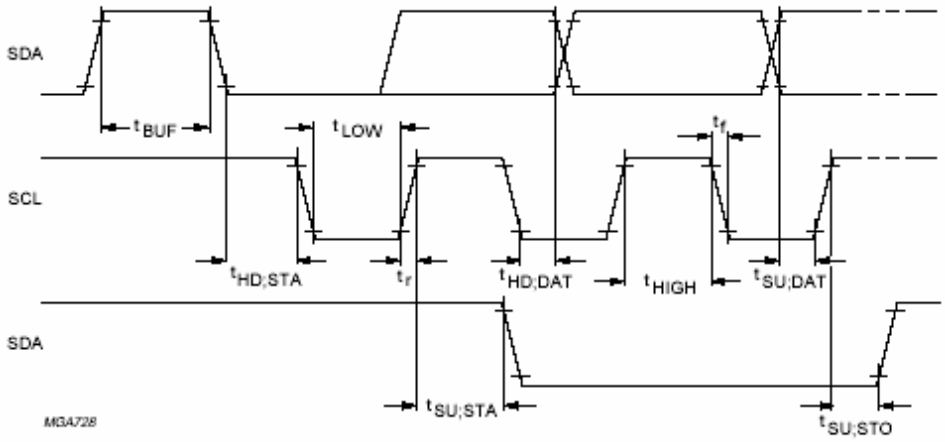


Fig.27 I²C-bus timing diagram.

COMPANY PROFILE

XIAMEN OCULAR LCD DEVIDES CO.,LTD. Was formed in 1992. Our company is a joint-venture specializing in manufacturing all kinds of Liquid Crystal Displays. We design and massproduce Touch Panel,LED,COG, the digital segment, dot matrix LCD panels, and modules in TN,HTN and STN types using the advanced and whole facilities and soft-ware technology.

Most of our products are customer_mode. Xiamen Ocular's LCDs now have a good sale not only in domextic China,but also in America,Europe and East_south Aisa.These LCDs were widely used in the display of instruments,clocks,telecommunication equipments,calcuators,air conditioner controllers and AV systems.

Based upon the reliable high quality, reasonable price and quick delivery, Xiamen Ocular will sever all customers wholeheartedly.

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